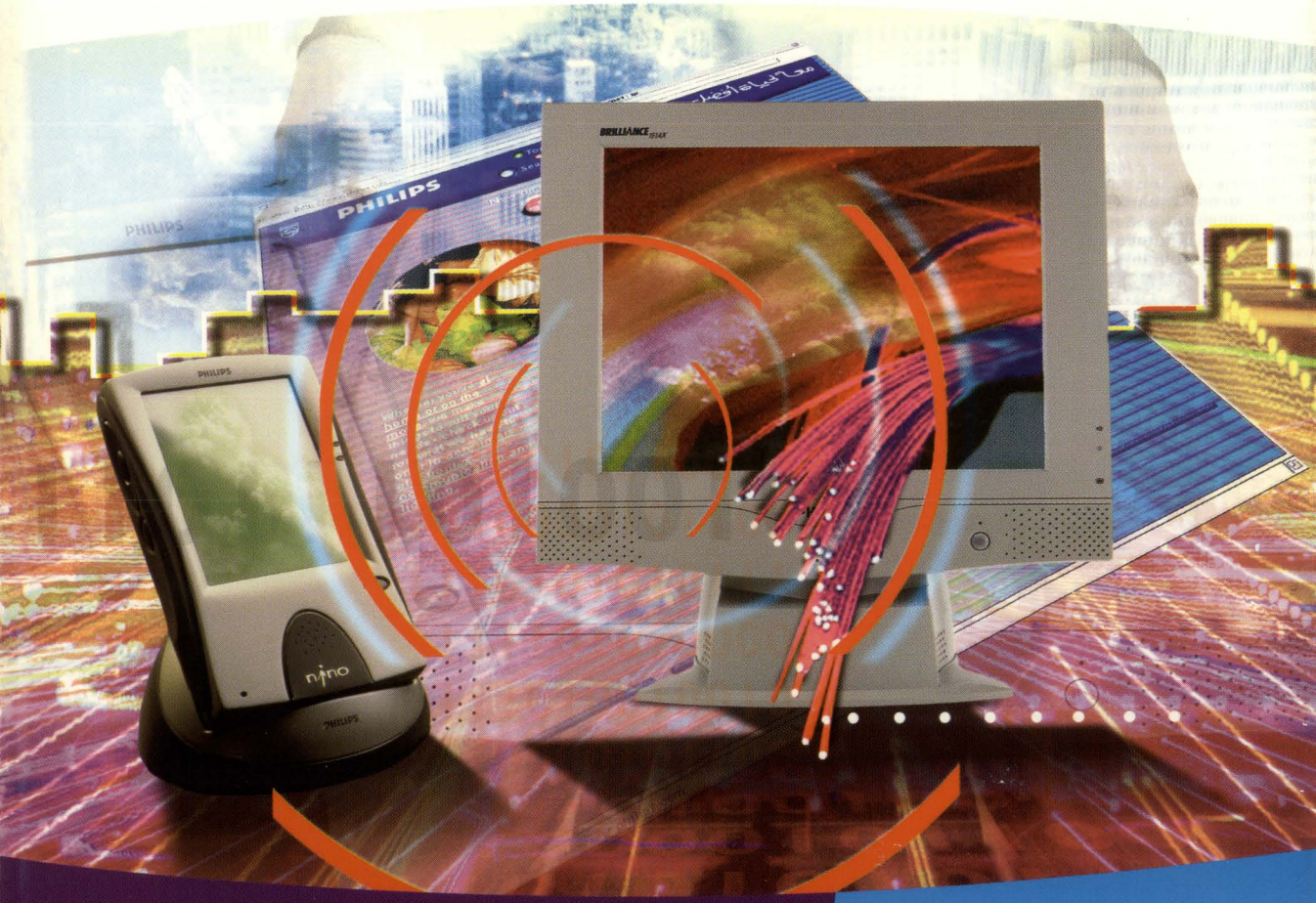
INTEGRATED CIRCUITS

ICs for Data Communications

Data Handbook IC19
CD-ROM included
1999



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PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

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DEFINITIONS

Data Sheet Identification	Product Status	Definition (Note)
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.
Short-form specification	—	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification

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These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such improper use or sale.

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NOTE: Always check with your local Philips Semiconductors Sales Office to be certain that you have the latest data sheet(s) before completing a design.

Preface

ICs for Data Communications

The Data Communications market is one of the fastest growing markets in electronics today. The desire to stay connected anywhere anytime is the fuel to this impressive development over the past decade. Philips Semiconductors has had a leading position for many years with products such as our UARTs and Serial Communications Controllers (DUSCC). The UART family has been expanded to include a number of 3.3 Volt CMOS products that supports low power consumption and multiple bus environments. New DataCom products are designed in the most advanced CMOS processes available.

The Trend to wireless data communication has manifested itself with the success of Wireless LAN solutions compliant to the IEEE 802.11 standard. Philips Semiconductors offers solutions the most competitive solutions for Frequency Hopping and Direct Sequence radios. Designed with the experience and technology of the world's leader in RF integrated circuits, our IC's offer the best performance for Wireless LAN radios on the market.

Philips Semiconductors has also expanded their commitment to the Network segment of the Data Communications market to support our customers in this high growth area. The Fiber Optic family (SA522X) for FDDI, SONET/SDH, Fiber Channel and the BTL family (FB20XX) for high–speed back planes are only a few examples out of the broad variety of networking products.

Philips Semiconductors commitment does not end with the product focus, but continues it to the highest levels of quality to insure our customers of cost effective ownership and world class reliability. In addition to the Data Communications product families, Philips offers a very extensive portfolio of semiconductor products, the details of which can be obtained from your local sales office.

As a result of innovating our product offering with new and enhanced data communication parts the data handbook grew thicker and thicker. Rather than splitting up the information of this handbook into several volumes, we took a different approach. To have the access to all the necessary information as easy as possible we created a CD–ROM, which will together with the Internet deliver the most comprehensive information of Philips Data Communication products. The printed Data Handbook companion will have included abstracts of all data sheets (features, pinout, block diagram, ordering information), selection guides, general descriptions of applications, abstracts of application notes and many more useful information to get an overview about the products and their applications. On the CD–ROM you'll find the complete versions of all documents included in the book. For the most complete and updated versions of our documentation visit our website at *http://www.semiconductors.philips.com* (see page 16 for specific information).

We hope that you'll find this method much more efficient and convenient for your daily work.

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ADDITIONAL MATERIAL ON ENCLOSED CD-ROM ONLY:

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CDUSCC Users Guide
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Wireless Business Line UARTs/DUSCCs Presentation
Demo board STM1/4/8, OC3, 12, 24, FC/GE (photo)
AN98090—Fiber optic transceiver board STM1/4/8, OC3, 12, 24, FC/GE
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TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through Failure Mode Effects Analysis (FMEA) the critical parameters are detected and measures taken to ensure good performance on these parameters. This method is also used to evaluate the capability of process steps.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, components reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the product reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action and continuous improvement.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

Replacement list

Discontinued Part	Package	Description	DO DN	last time buy	Replacement	Remarks
AM26LS31C	F	Quad high speed Line Driver	37	1/1/98	none	
AM26LS31C	D, D/T, N	Quad high speed Line Driver	36	6/30/97	none	
AM26LS31I	D, D/T, N	Quad high speed Differential Line Receiver	36	6/30/97	none	
AM26LS31M	F, N	Quad high speed Differential Line Receiver	36	6/30/97	none	
AM26LS32C	F	Quad high speed Differential Line Receiver	37	1/1/98	none	
AM26LS32C	D, D/T, N	Quad high speed Differential Line Receiver	36	6/30/97	none	
AM26LS32I	F	Quad high speed Differential Line Receiver	37	1/1/98	none	
AM26LS32I	D, D/T, N	Quad high speed Differential Line Receiver	36	6/30/97	none	
AM26LS32M	F, N	Quad high speed Differential Line Receiver	36	6/30/97	none	
AM26LS33C	D, D/T, N	Quad high speed Differential Line Receiver	36	6/30/97	none	
AM26LS33I	D, D/T, N	Quad high speed Differential Line Receiver	36	6/30/97	none	
FB2012A	A, A/T	Futurebus central arbitration controller	36	9/30/97	none	
NE5180	N	Octal receiver	38	6/30/98	NE5180A	
NE5180	A, A/T	Octal receiver	39	6/30/99	none	
NE5181	A, A/T, N	Octal Differential Receiver 10Mbit/s	36	12/31/97	none	
NE5211	D/T	Transimpedance amplifier (180MHz)	38	9/30/98	SA5211	
NE5212A	D, D/T, N	Transimpedance amplifier (140MHz)	37	1/1/98	SA5212A	
NE5212A	FE	Transimpedance amplifier (140MHz)	36	6/30/97	SA5212A	
NE5214	D/T	Post amplifier with link status indicator	38	9/30/98	SA5214	
NE5217	D, D/T	Post amplifier with link status indicator	39	6/30/99	SA5217	
NE5224	D, D/T	FDDI fiber optic post amplifier	39	6/30/99	SA5224	
NE8392C	A, A/T	Ethernet coaxial transceiver	39	12/31/98	NE83C92	
NE8392C–2	A, A/T, N	Coaxial transceiver interface for Ethernet	36	6/30/97	none	
NE83C92	N	Low–power coaxial Ethernet transceiver	38	6/30/98	NEC92A	
NE83Q92	N	Low–power coaxial Ethernet transceiver	38	12/31/98	NE83Q92A	
NE83Q93	N, D, D/T	Enhanced coaxial Ethernet transceiver	38	12/31/98	none	
NE86C92	D, D/T, N	10 BASE–T transceiver	36	6/30/97	none	
SA5212A	FE	Transimpedance amplifier (140MHz)	36	6/30/97	SA5212A	use different package
SA5222	D, D/T	Low–power FDDI transimpedance amplifier	38	9/30/98	SA5223	
SC26C562C1	N	CMOS dual universal serial communications controller (CDUSCC)	38	9/30/98	SC26C562C1A	Discontinued 48-pin DIP
SC68C562C1	N	CMOS dual universal serial communications controller (CDUSCC)	38	9/30/98	SC68C562C1A	Discontinued 48-pin DIP
SCC2692AC1	F40	Dual Asynchronous Receiver/Transmitter (DUART)	37	1/1/98	none	Discontinued ceramic package
SCC2692AE1	F40	Dual Asynchronous Receiver/Transmitter (DUART)	37	1/1/98	none	Discontinued ceramic package
SCC2698BC1	N64	Octal Asynchronous Receiver/Transmitter (OUART)	39	12/31/98	SCC2698BC1	Discontinued 64-pin DIP
SCC2698BE1	N64	Octal Asynchronous Receiver/Transmitter (OUART)	39	12/31/98	SCC2698BE1	Discontinued 64-pin DIP
SCN2641	A, A/T, F, N	Asynchronous communication interface	36	6/30/97	none	
SCN2652AC2	A44, A44/T	Multi–protocol communications controller (MPCC)	38	9/30/98	SCN2652AC2	Discontinued low-speed part
SCN26562C2	A52/T, N48	Dual universal serial communications controller (DUSCC)	38	9/30/98	SCN26562C4	Discontinued low-speed part
SCN26562C4	N48	Dual universal serial communications controller (DUSCC)	38	9/30/98	SCN26562C4	Discontinued 48-pin DIP
SCN2661AA	F28	Enhanced programmable communications interface (EPCI)	37	1/1/98	none	Discontinued ceramic package

Replacement list

SCN2681AE1	N24	Dual Asynchronous Receiver/Transmitter (DUART)	39	12/31/98	SCN2681C1	Discontinued 24-pin DIP
SCN2681TC1	N40	Dual Asynchronous Receiver/Transmitter (DUART)	38	XXX	SCN2681TC1	Discontinued 40-pin DIP
SCN68562C2	A52/T, A52, N48	Dual universal serial communications controller (DUSCC)	38	9/30/98	SCN68562C4	Discontinued low-speed part
SCN68681E1	F40	Dual Asynchronous Receiver/Transmitter (DUART)	37	9/30/97	none	Discontinued ceramic package

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To navigate to the *IC19–ICs for Data Communications* databook, follow the instructions below.

In the navigation bar in the browser, type the following:

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On this page, under the ICs folder, click on the folder **Communications**.

Then select **IC19–ICs for Data Communications** link. This will display the contents of the IC19 databook.

By clicking on the desired product type folder, a display of individual documents is returned. Click on the part number desired; a "Product Information Page" will be displayed, which provides a brief description of the product. Click **Datasheet**, then **Download PDF** to view, print, or save the complete document using Acrobat Reader.

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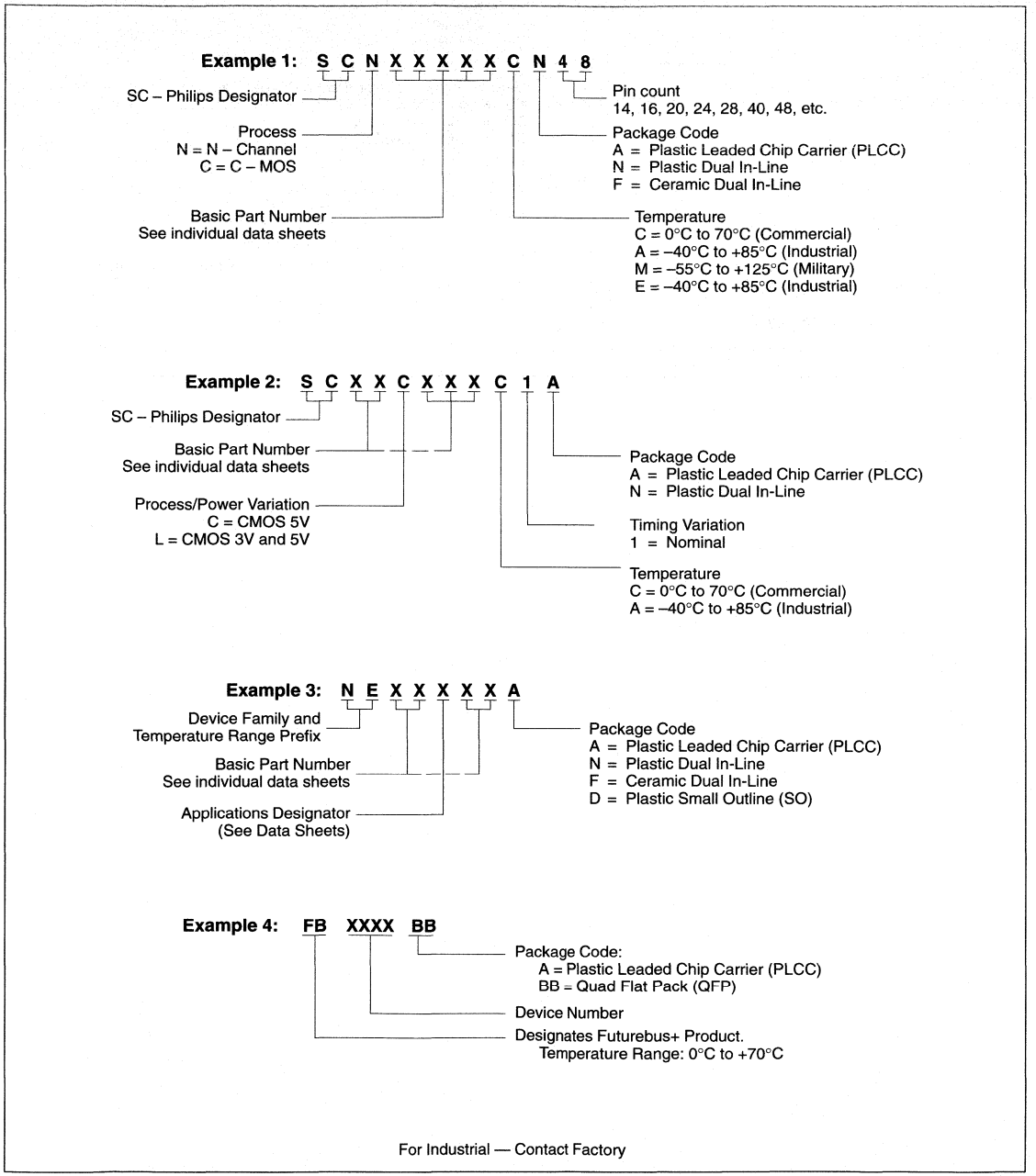
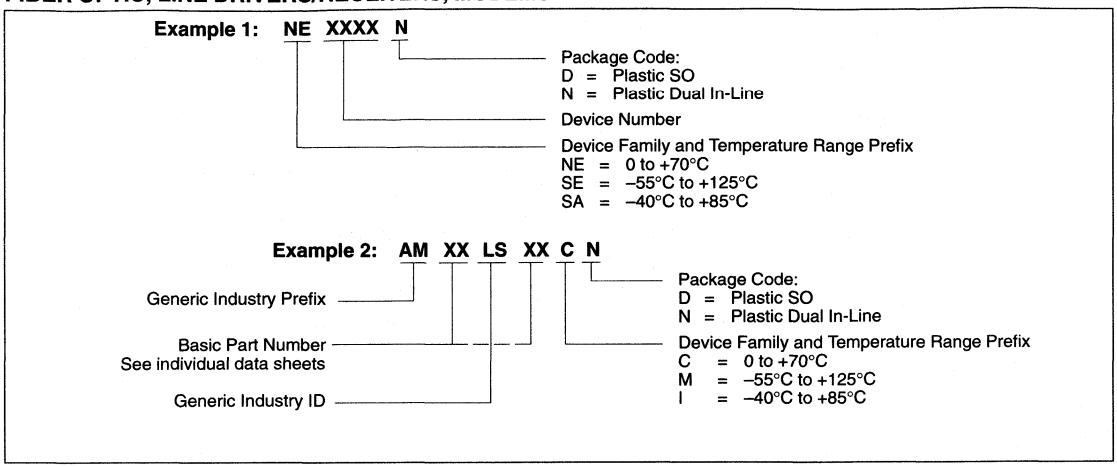
DATA COMMUNICATIONS, LOCAL AREA NETWORK, FUTUREBUS+



Ordering information

FIBER OPTIC, LINE DRIVERS/RECEIVERS, MODEMS



Network terms

A

Access method: A software/hardware method of transferring data between host–resident application programs and remote devices. This term is usually used to describe communications software residing in a mainframe computer.

ACK or acknowledge: A character or sequence of characters sent by a receiver to notify a sender that the last message was received correctly. ACK is also sent by a remote device as a "go–ahead" response to a selection sequence.

Acoustic coupler: A type of modem that permits use of a telephone handset as a connection to the public telephone network for data transmission by means of sound transducers.

Adaptive differential pulse code modulation: One of the methods of pulse code modulation utilized in digitizing an analog signal (32 Kbps is typical).

Adaptive equalization: A modem feature allowing it to automatically compensate for distortions on the line.

Adaptive predictive coding: A methodology used in compressing digitized voice signals.

Algorithm: A prescribed set of well–defined rules or processes for arriving at a solution to a problem. A mathematical process.

Alphanumeric: Made up of letters (alphabetic) and numbers (numeric).

Alternative route: A secondary communications path used to reach a destination if the primary path is unavailable.

Amplitude modulation: Transmission of information on a communications line by varying the voltage level or amplitude.

Ambient noise: Signal interference that is present on a communications line at all times (background noise).

Amplifier: A device that increases the power or amplitude of a signal.

Amplitude variation (ripple): Unwanted variation of signal voltage at different frequencies on a communications line.

Analog signal: A signal that changes in a non-discrete manner (smooth transitioning to different levels).

Answer back: A transmission from a receiving data processing device in response to a request from a transmitting data processing device that it is ready to accept or has received data.

ARQ, Automatic re-transmission request: A generic description of a protocol mechanism that involves re-transmission of message blocks received in error. There are several types of ARQ operation.

Asynchronous: A data transmission which does not require a separate clock signal for the reception of data. In code sets, character codes containing start and stop bits.

Asynchronous transmission (start–stop transmission): Provides transmission of one character at a time with a start bit and one or more stop bits appended on each one. Any amount of time can elapse before the next character can be sent.

Attenuation: Loss of communication signal energy.

Audio frequencies: Frequencies that can be heard by the average human ear, usually between 15 and 20,000 Hz.

Automatic dialer: A device that will automatically dial telephone numbers on the network. Operation of the dialer may be manual or automatic.

B

Backward channel (also called reverse channel): A channel used for sending data in the opposite direction of the primary (forward) channel. The backward channel is usually used for sending data at low speeds for either control purposes or keyboard data.

Balanced circuit: A circuit terminated by a network whose impedance balances the impedance of the line so that the return losses are negligible.

Bandwidth: The information carrying capability of a communications channel or line.

Baseband: The frequency band occupied by individual information bearing signals before they are combined with a carrier in the modulation process. In LANs, one transmitting device at a time on the circuit.

Base group: Twelve communications paths capable of carrying the human voice on a telephone set. A unit of frequency-division multiplexing systems bandwidth allocation.

Baud: Data communication rate unit taken from the name Baudot. Defined as the number of signal level changes per second regardless of the information content of those signals.

Baudot: A five-level code set named for the early French telegrapher who invented it. International Telegraph Alphabet (ITA) Number 2 is the formal name.

Bias: Communications signal distortion with respect to bit timing.

Bit: Binary digit contraction. The smallest unit of data communications information, used to develop code representations of characters.

Bit–oriented protocol: Refers to those data communications protocols that move bits across a data link without regard to the meaning of those bits. Nearly all bit-oriented protocols follow the international HDLC recommendations.

Bit rate: The rate at which bits (binary digits) are transmitted over a communications path. Normally expressed in bits per second (BPS). The bit rate is not to be confused with the data signaling rate (baud), which measures the rate of signal changes being transmitted.

Bit stream: Refers to a continuous series of bits being transmitted on a transmission line.

Blank: A condition of "no information" in a data recording medium or storage location, which can be represented by all spaces or all zeros, depending on the medium.

Block error rate testing: Testing a data line with groups of information arranged into transmission blocks for error checking.

Block: Some set of contiguous bits, bytes, or both that make up a definable quantity of information.

Block check character: A single character appended to the end of a data block for error-checking purposes. The BCC is usually LRC but could also be checksum results.

Blocked Asynchronous/Synchronous Transmission: A proprietary software package for sending asynchronous and synchronous information used primarily by personal computer interfaces.

Blocking: A condition in a switching system or PBX in which no paths or circuits are available to complete a call and no dial tone is

Network terms

returned to the calling party. In this situation there is no alternative but to hang up and try the call again. Also referred to as denial or busy condition.

Block multiplexer channel: A computer peripheral multiplexer channel that interleaves blocks of data. See also Byte multiplexer channel. Contrast with selector channel.

Break: A signal used to "break in" when the opposite party or unit is sending. A feature of dial point-to-point teletypewriter systems operating in half duplex.

Breakout box: A test device utilized for monitoring and inserting signals at the RS-232 interface. Bridge Equipment and techniques used to connect circuits and equipment to each other ensuring minimum transmission impairment. Bridging is normally required on multipoint data channels where the drop for the local loop is separated from the circuit that continues on to the next drop.

Broadband: Refers to transmission facilities whose bandwidth (range of frequencies they will handle) is greater than that available on voice-grade facilities; sometimes called wideband. Also used to describe a particular kind of local area network configuration where multiple different users can share the same cable facility in different channels.

Broadcast: The ability to send messages or communicate with many or all points on a circuit simultaneously.

Burst: A series of events occurring as a group.

Burst error: A series of consecutive errors in data transmission. Refers to the phenomenon on communication lines where errors are highly prone to occurring in groups or clusters.

Bus: A single connective link between multiple processing sites (co-located only) where any of the processing sites can transmit to any other but only one way at a time.

Byte: Some set of contiguous bits that make up a discrete item of information. Bytes are 8 bits long.

Byte multiplexer channel: Multiplexer channel that interleaves bytes of data from different sources. Contrasts with selector channel.

C

Call forwarding: Calls to one station can be automatically switched to another specified station.

Call setup time: The overall length of time required to establish a switched call between pieces of data terminal equipment.

Camp-on: A feature of a switching station or device that notifies a calling station that a called station is busy and allows the calling station to wait and be automatically connected when the line is free.

Carrier: An analog signal at some frequency modified by information (changes to frequency or amplitude or phase or combinations of amplitude and phase) to represent that data in a communication system.

Carrier system: A method of obtaining or deriving several channels from one communication path by combining them at the originating end, transmitting a wideband or high-speed signal, and then separating the original information at the receiving end.

Centrex: A type of private branch exchange service where the equipment is physically located in the local telephone exchange.

Chain: A series of processing locations that information must pass through each location on a store-and-forward basis in order to get to a final location.

Channel: A data communication path.

Channel bank: Communication equipment performing multiplexing. Typically used for multiplexing voice-grade channels.

Character: A language unit composed of bits.

Character parity: A technique of adding an overhead bit to a character code to provide error-checking capability.

Character synchronization: The process through which a receiving device can determine which bits, sent over a data link, should be grouped together into characters.

Checksum: A BCC or BCS that is computed using simple binary addition.

Circuit: The electrical path that provides communication between two or more locations.

Circuit switching: A method of communication in which an electrical connection between calling and called stations is established on demand for exclusive use of the caller until the connection is released.

Clocking: Time synchronizing of communication information.

Cluster: A group of user terminals co-located and connected to a single controller through which each terminal is afforded the opportunity to access a single communication line.

Cluster controller: An intelligent device, usually located at a remote site, that allows several "dumb" terminals or similar devices to connect to a single modem on a data link.

Coaxial cable: Cable with a shield against noise around a signal–carrying conductor.

CODEC, Coder/Decoder: A device for digitizing a voice signal or converting the digitized signal back to voice. Performs the opposite function of a modem.

Communication line controller: A hardware unit that performs line control functions with the modem.

Compandor: A device used on some telephone channels to improve transmission performance. The equipment compresses the outgoing speech volume range and expands the incoming speech volume range on a long–distance telephone circuit.

Concentrator: An electronic device that interfaces in a store and forward mode with multiple communication lines at a message level and then re-transmits those messages via one or more high-speed communications lines to a processing site.

Conditioning: A technique of modifying electrical circuit parameters on a communication line to improve the capability of that line to support higher data transmission rates. (See Equalization.)

Contention: User competition for use of the same communications facilities; a method of line control in which terminals request or bid to transmit. If the channel is not free, the terminals must wait until it is.

Control character: A character that is normally non-printable and used for control purposes rather than for the exchange of information.

Controlled carrier: A feature of a modem that allows the modem carrier signal to be turned on or off under command of the DTE. A controlled carrier is necessary at remote locations on multipoint lines.

Network terms

CRC, cyclic redundancy check: An error-checking control technique utilizing a specifically binary prime divisor that results in a unique remainder.

CSMA/CD, carrier sensed multiple access/collision detection: A method of transmitting information in the local area network environment (LAN) where only one transmitter may be on the line at any one time. If two devices transmit simultaneously, the signals "collide" and both must cease transmission. Each will try again at a later time determined by a different internal delay.

CTS, clear to send: A control line between a modem and a controller used to operate over a communication line.

Current loop: An interface in which the absence or presence of current now (as opposed to voltage levels) is used to provide signaling between devices.

Cursor: A lit area on an electronic display screen used to indicate the next character location to be accessed.

D

Data compression: The technique that provides for the transmission of fewer data bits without the loss of information. The receiving location expands the received data bits into the original bit sequence.

Data set (modem): An electronic terminating unit for analog lines used for data signal modulation and demodulation.

dBm: Power level measurement unit in the telephone industry. 0 dBm is 1mW at 1004 Hz terminated by 600Ω impedance.

Decibel (dB): Power level measurement unit.

Dedicated line: A communication line that is not dialed. Also called a leased line or private line.

Delay: A period of time that elapses between the end of one event and the start of another.

Delay distortion: A distortion that occurs on communication lines due to the different propagation speeds of signals at different frequencies. Some frequencies travel more slowly than others in a given transmission medium and therefore arrive at the destination at slightly different times. Delay distortion is measured in microseconds of delay relative to the delay at 1200 Hz. Delay distortion does not affect voice, but it can have a serious effect on data transmissions.

Demodulator: A functional section of a modem that converts the received analog line signals back to digital form.

Dial line: A communication line that is dialed.

Digital: A two-discrete-state signal.

Distortion: The unwanted modification or change of signals from their true form by some characteristic of the communication line or equipment being used for transmission (such as delay distortion, amplitude distortion).

DPCM, differential pulse code modulation: A method of digitizing an analog signal.

Drop outs: On a communication line, the signal can temporarily disappear, causing loss of data. Drop outs are often caused by environmental influences such as lightning.

DSSS, direct sequence spread spectrum: In wireless data transmission, method of multiplying the data with a pseudo-noise sequence made up of narrow impulses, called chips. In IEEE802.11 an 11 chip Barker code is used.

E

Echo distortion: A telephone line impairment caused by electrical reflections at distant points where line impedances are dissimilar.

Echoplex: An error-detection method in which characters sent by a terminal to a host are sent back to the terminal and displayed.

Echo suppressor: A device installed in long-distance telephone lines for eliminating echo back to the speaker. Echo suppressors can cause difficulties with simultaneous two-way communications unless they are disabled by the modems.

Emulation: The act of imitating or performing as if a device or program were something else.

Encryption: The technique of modifying a known bit stream on a transmission line so that it appears to be a random sequence of bits to an unauthorized observer.

End office: The first telephone office that a data line is connected to over the local loop or access line. The end switching office for a dialed connection.

Envelope delay: An analog line impairment where a variation of signal delay with frequency occurs across the data channel bandwidth (see Delay distortion).

Equalization: A technique used to compensate for distortions present on a communication channel.

Error rate: The number of errors per unit of information in the test to establish the error rate.

F

FDM, frequency-division multiplexing: A multiplexing technique with which a data line bandwidth is divided into different frequency sub-channels used to share a data line between several user terminals.

FHSS, frequency hopping spread spectrum: In wireless data transmission, method of hopping from channel to channel following a certain sequence to transmit information.

Fiber-optics: Glass fibers that carry visible light containing information in cables.

Filter: Electronic circuitry that blocks some components of a signal while allowing other components to pass through uniformly. For example, a high-pass filter blocks all frequencies in a signal that are below a specified frequency called the "cut off."

Firmware: A set of software instructions set permanently or semi-permanently into a read-only memory.

Fixed equalization: A simple equalization technique for modems by which the amount of compensation is preset internally or externally to the modem.

Flag: A bit field or character of data used to set apart the data on either side of the flag. A delimiter.

Flow control: A procedure by which a sending station can be "throttled" so that it does not send more data into the data link or network than can be handled by the link or network.

FM, frequency modulation: A method of transmitting digital information on an analog line by changing the carrier frequency between two different values.

Network terms

Format: A structure of a message or data such that specific controls or data can be identified by their position during processing.

Forward error correction: The technique that provides for the transmittal of additional information with the original bit stream so that if an error is detected the correct information can be recreated at the receive end without a re-transmission.

Four-wire circuit: A circuit that consists of two twisted pair cables. A four-wire circuit provides two separate circuits between stations.

Frame: Bit–oriented protocols refer to data blocks as frames. Also, in T-1 transmissions, 8 bits from each of 24 channels plus 1 frame bit for a total of 193 bits.

Frequency: The number of cycles of an alternating current signal per unit time.

Frequency shift keying, FSK: A form of frequency modulation in which the carrier frequency is made to vary or change in frequency at the instant there is a change in the state of the signal being transmitted (the carrier frequency on the line during a one or marking condition would be shifted to another predetermined frequency during a zero or spacing condition).

Frequency stacking: Another name for FDM, which indicates how the multiplexing is performed.

Front end: An auxiliary computer system that performs network control operations, freeing the host computer system to do data processing.

Full duplex: A four-wire circuit, or a protocol that provides for transmission in both directions at the same time between the same two points.

Full–duplex modem: Provides a channel for sending data in each direction. Full-duplex modems are required for two stations to send data to each other at the same time.

G

Gain: The degree to which the amplitude of a signal is increased. The amount of amplification realized when a signal passes through an amplifier or repeater. Normally measured in decibels.

Gaussian noise: A noise whose amplitude is characterized by the Gaussian distribution, a well known statistical distribution (white noise, ambient noise, hiss).

Geosynchronous: A communication satellite orbit at the correct distance from earth and at the correct speed to appear fixed in space as the earth rotates.

Gigahertz (GHz): An analog frequency unit equal to 1 billion Hz.

Go-back-N: A form of continuous ARQ in which all blocks or frames following a block received in error are discarded and need to be resent.

Group address: Used to address two or more stations in a predesignated group.

Guardband: The unused frequency band between two channels that provides separation of the channels to prevent mutual interference.

H

Half duplex: A communication line consisting of two wires or a protocol capable of transmitting only one direction at a time.

Handshaking: Line termination interplay to establish a data communication path.

Harmonic: Frequencies that are multiples of some fundamental frequency.

Harmonic distortion: A data communications line impairment caused by erroneous frequency generations along the line.

High-level data link control: An ISO standard data communications line protocol.

Hertz: Internationally recognized unit of measure for electrical frequency. The number of cycles per second. Abbreviated Hz.

House cables: Conductors within a building used to connect communications equipment to termination blocks.

Hybrid: An inductive device that converts a two-wire circuit into a four-wire circuit or a four-wire circuit into a two-wire circuit.

I

Impedance: The total opposition offered by a component or circuit to the flow of an alternating or varying current; a combination of resistance, capacitance, and inductance.

Impulse noise: A type of interference on communication lines characterized by high amplitude and short duration. This type of interference may be caused by lightning, electrical sparking action, or by the make-break action of switching devices.

Insertion loss: Signal power loss due to connecting communication equipment units with dissimilar impedance values.

Integrity of data: The status of information after being processed by software or transmitted over a communication link.

Interference: Refers to unwanted occurrences on communications channels that are a result of natural or man-made noises and signals, not properly a part of the signals being transmitted.

Intermodulation distortion: An analog line impairment where two frequencies create an erroneous frequency, which in turn distorts the original data signal representation.

Isochronous: The term given to the movement of start-stop data (asynchronous transmission) over a synchronous data link with each intervening time interval being an integral number of character times.

J

Jitter: Type of analog communication line distortion caused by the variation of a signal from its reference timing positions, which can cause data transmission errors, particularly at high speeds.

K

L

Leased line, private line, dedicated line: A communications line, usually a four-wire circuit, for voice, data, or both leased from a communications carrier on a monthly basis.

Line driver: An inexpensive amplifying device that allows two or more devices to communicate over inexpensive twisted-pair cable up to 2000 feet and up to 19,200 BPS.

Loading coils: Inductive devices that improve the quality of voice transmissions (distorts data signals and must therefore be compensated for by standard modems).

Network terms

Local loop: The access line from either a user terminal or a computer port to the first telephone office along the line path (also called station loop, end loop, or subscriber loop).

Logging: The act of recording something for future reference, such as error events or transactions.

Loopback: Directing signals back toward the source at some point along a communications path.

Loop current: A teletypewriter-to-line interface and operating technique that involves switching an electrical current on and off to represent data bits.

M

Mark: Interface standards define a mark to be the condition of the data line when sending a logic one.

Megahertz, MHz: A unit of analog frequency equal to 1 million Hz.

Message switching: Routing messages among three or more locations by store-and-forward techniques in a computer.

Metallic circuits: Refers to circuits that use metal wire (copper) from end to end. Implies that no loading coils or any other devices are interposed between the ends of the circuit. Metallic circuits have electrical (DC) continuity from end to end.

Microcode: A set of software instructions that executes a macro instruction.

Microwave: A radio carrier system using frequencies whose wavelengths are very short.

Milliampere, mA: Electric current measurement unit equal to 0.001 Ampere.

Milliwatt, mW: A power unit of measurement equal to 0.001 watt.

Modem (data set): An acronym taken from functions the unit performs by modulating and demodulating the digital information from a terminal or computer port into an analog carrier signal to be sent over an analog line.

Modem eliminator: A device that allows two DTE devices to be connected without using modems.

Modem sharing unit: A device that allows several terminals or other devices to share a single modem.

Multiplexer: A device that accepts many data lines and combines them into a single high-speed, composite data stream.

Multipoint line: Also called a multidrop line. A communications line having several subsidiary controllers that share time on the line under control of a central site.

Multistation controller: A terminal controller having more than one terminal device connected to it for subsequent access to the communication line.

N

Narrowband: Refers to a LAN configuration in which only one user can transmit at any one time (sometimes called baseband).

Noise: A communications line impairment that is inherent in the line design or induced by transient bursts of energy.

O

Octet: A group of eight bits that usually, though not necessarily, represents a byte, or word, and so on.

P

Packet switching: The transfer of data by means of addressed packets whereby a channel is only occupied for the duration of transmission of the packet. The channel is then available for the transfer of other packets.

PAD, packet assembler/disassembler: Equipment providing packet assembly and disassembly facilities.

Parity error: An error that occurs in a particular entity of data in which an extra or redundant bit is sent with the data. Detects only odd numbers of bit errors. Even numbers of bit errors are not detected.

Pass–band filters: Filters used in modem design to allow only the frequencies within the communication channel to pass, while rejecting all frequencies outside the pass band.

Patching jacks: Series–access devices used to patch around faulty equipment using spare units.

Private branch exchange: A telephone switchboard.

PCM, pulse code modulation: A generic method of converting an analog signal to a digital form.

Phase hits: A sudden electrical disturbance on a communication line which causes the phase of the carrier signal to change, causing bit errors on the data link.

Phase jitter: An analog line impairment caused by power and communication equipment along the line, shifting the signal phase relationship back and forth.

PM, phase modulation: A method of combining digital information onto a line-carrying signal by variation of the phase relationship of the signal. May also indicate preventive maintenance in the form of service functions provided during periods of normal operation to reduce the probability of failure later on.

Point to point: A communications line connected directly from one point to another, as opposed to multipoint lines.

Polling: A control message sent from a master site to a slave site as an invitation for the slave site to transmit data to the master site.

Propagation delay: The time necessary for a signal to travel from one point on the circuit to another.

Protocol: A formal set of conventions governing the format and control of inputs and outputs between two communicating processes. Includes handshaking and line discipline.

PSK, phase shift keying: A method of analog modulation utilizing differences in phase only as representing data bit one of several ways to represent an analog signal. Typical methods involve modifying the amplitude (PAM), width or duration (PDM), or position (PPM). The most common pulse modulation technique in telephone work is pulse code modulation (PCM). In PCM, the analog signals are sampled at regular intervals and a series of binary bits representing the amplitude of each pulse is transmitted, representing the amplitude of the information signal at that time. The standard sampling in today's environment is 8000 times per second with 8 binary bits representing each sample pulse giving a required transmission rate of 64,000 BPS.

Network terms

Q

QAM, quadrature amplitude modulation: A method of modulation in which two carriers in quadrature are used for modulation. One carrier is used for modulating the X axis and the other carrier is used for modulating the Y axis.

Quadrature distortion: Analog signal distortion frequently found in phase modulation modems.

R

Regenerative repeaters: A device interposed between the ends of a data link or between nodes of a network to regenerate distorted signals. Used in digital transmission.

Response time: The time measured from the depression of the enter key at a terminal to the display of the first character of the response at that terminal site.

Reverse channel: An optional feature provided on some modems that provides simultaneous communication from the receiver to the transmitter on a two-wire channel. It may be used for circuit assurance, circuit breaking, and facilitating certain forms of error control and network diagnostics. Also called backward channel.

RTS, request to send: An RS-232 control signal that requests a data transmission on a communication line.

S

SDLC, synchronous data link control: An IBM data communications message protocol. A subset of HDLC.

Slicing level: A voltage or current level of a digital signal that determines whether a one or zero bit will be recognized.

Slot: A unit of time in a TDM frame in which a sub-channel bit or character is carried to the other end of the circuit and extracted by the receiving TDM unit.

S/N, signal–to–noise ratio: The relative power levels of a communication signal and noise on a data line, expressed in decibels.

Space-division multiplexing: Refers to using a separate circuit or channel for each device. Essentially this means no multiplexing at all. If, for example, a new terminal needs to be added to a system, a separate wire is run to accommodate it.

Spread spectrum: Spreading the bandwidth needed to transmit information.

Start bit: In asynchronous transmission, the start bit is appended to the beginning of a character so that the bit sync and character sync can occur at the receiver. The start bit is always a "0" or "space" condition.

Start–stop: Also known as asynchronous transmission. A transmission technique in which each character is preceded by a start bit and followed by a stop bit.

Stop-and-wait ARQ: A form of ARQ in which the sender sends one block of data and stops sending until an acknowledgment for that block is received from the receiver. An example is bisync.

Stop bit: In asynchronous transmission, the stop bit is appended to th end of each character. The stop bit is always a "1" or "mark" condition. It sets the receiving hardware to a condition where it looks for the start bit of a new character. May be 1 or 2 bits.

Store and forward: A data communication technique that accepts messages or transactions, stores them until they are completely in the memory system, and then forwards them to the next location as addressed in the message or transaction header.

Streaming: A condition of a remote modem when it is sending a carrier signal on a multi-drop communication line and will not turn off.

String coding: A technique for combining multiple sequential occurrences of the same character or bits.

Switched service: A common carrier communications service that requires that call establishment take place before a data link can be established. For example, DDD is a switched service.

Sync (syn): A bit or character used to synchronize a time frame in a TDM. Also a synchronizing sequence used by synchronous modems to perform bit synchronization and by the line controller for character synchronization.

Synchronous modem: A DCE that utilizes a clocking signal to perform bit synchronization with the incoming data.

Synchronous transmission: Messages sent in blocks where all characters or bits are sent contiguously. No start or stop bits are appended to characters. Each block begins with a sync sequence and a start of message sequence so that character framing can occur at the receiver and ends with an end of message sequence to prepare the receiver to look for a new message.

T

Tariff: The rates, rules, and regulations concerning specific equipment and services provided by a communications carrier.

T-Carrier: The AT&T name for their digital carrier system used for carrying data or digitized voice signals.

TDMA, time division multiple access: A method utilized primarily in satellite transmission in which various users share their time on the same satellite link (portions of separate users are multiplexed onto the same link through a satellite).

Telemetry: Collection and transmission of data obtained from remote locations by sensing conditions in a real-time environment.

Telex: A teletypewriter service that allows subscribers to send messages to other subscribers on an international level over the public telephone network.

Terrestrial circuits: Non-satellite channels.

Text: That part of a message or transaction between the control information of the header and the control information of the trace section or tail that constitutes the information to be processed or delivered to the addressed location.

Thermal noise: A type of electromagnetic noise produced in conductors or in electronic circuitry that is proportional to temperature. See also Gaussian noise.

Time-division multiplexing, TDM: A technique for combining several information channels into one facility or transmission path in which each channel is allotted a specific position in the signal stream based on time. At the receiving end, the signals are separated to reconstruct the individual input channels.

Time-out: A protocol procedure that requires a device to make some response to a command or message block within a certain period of time. If the response does not occur within that period of time, a time-out condition occurs, which is considered an error condition.

Network terms

Time sharing: A processing technique by which multiple users at their own remote terminals have the ability to share common computer resources at the same time.

Trailer or trace block: Control information transmitted after the body or text of a message or transaction used for tracing error events, timing the communications through the network, and recovering misplaced blocks or transactions after system failures.

Transparency: A transmission mode achieved when both the sending and receiving devices do not react to the content of the data they are sending.

Trunk: A multiple line circuit that connects two switching or distribution stations or centers. Also a circuit from a PBX to a Class 5 telephone office.

Turnaround time: The time required for a modem to reverse direction of transmission on a two-wire circuit.

U

V

Validity checking: The techniques used to check the accuracy of data after transmission on data lines.

VF, voice frequency or voice-grade line: A 4.2kHz bandwidth telephone channel designed to carry the human voice from one telephone set to another. The usable portion of the band is 300 Hz to 3300 Hz.

VHF, very high frequency: A radio carrier frequency band used in radio transmissions.

VRC, vertical redundancy checking: A method of character parity checking.

W

WATS, Wide Area Telephone Service: A flat rate or measured bulk rate long–distance telephone service provided on an incoming or outgoing basis. By use of an access line, WATS permits a customer to make telephone calls to any dialable telephone number in a specific zone for an hourly rate. INWATS permits reception of calls from specific zones over an access line in like manner but the called party is charged with the call. The United States has been divided into five zones of increasingly greater coverage depending on the location of the customer.

White noise: See Gaussian noise; Thermal noise.

Wideband: In LAN systems, the ability for multiple users to communicate simultaneously in different channels. Same as broadband.

Word: One or more contiguous bytes, which may also be used to identify a class of computer.

NETWORK STANDARDS

Three types of Network Standards are described here. The first will be the Electronic Industries Association (EIA) specifications, which are always preceded by the letters RS (Recommended Standard) or EIA. The second set will be the CCITT standard interface specifications, which are always preceded by the letter V, and the third series of specifications, also established by the CCITT, are always preceded by the letter X. A V specification deals primarily with telephone circuits, while the X specifications deal primarily with data interfaces and public data networks. The most common specifications in use today are identified below.

EIA–232–D. Interface between data terminal equipment and data communication equipment employing serial binary data interchange (January 1987).

EIA–269–B. Synchronous signaling rates for data transmission (January 1976; identical to ANSI X3.1–1976).

EIA–334–A. Signal quality at interface between data processing terminal equipment and synchronous data communication equipment for serial data transmission (August 1981) (also adopted as ANSI X3.24–1967).

EM–334–A–1. Addendum No. 1 to EIA–334–A and EIA–404. Application of signal quality requirements to EIA449.

EIA–357. Interface between facsimile terminal equipment and voice–frequency data communication terminal equipment (June 1968).

EIA–363. Standard for specifying signal quality for transmitting and receiving data processing terminal equipment using serial data transmission at the interface with non-synchronous data communication equipment (May 1969).

EU–366–A. Interface between data terminal equipment and automatic calling equipment for data communication (March 1979).

EIA–404–A. Standard for start/stop signal quality between data terminal equipment and non-synchronous data communication equipment ANSI approved (January 1986).

EIA–404–1. Addendum No. 1 to EIA–404 and EIA–334–A. Application of signal requirements to EIA449.

EIA–410. Standard for electrical characteristics of class A closure interchange circuits (April 1974).

EIA–422–A. Electrical characteristics of balanced voltage digital interface circuits (December 1978).

EIA–423–A. Electrical characteristics of unbalanced voltage digital interface circuits (December 1978).

EIA–449–1. General–purpose 37–position interface for Data Terminal Equipment and Data Circuit terminating Equipment employing serial–binary data interchange. (The electrical signal characteristics for EIA–449 are defined by either EIA–422 or EIA–423, since EIA–449 is only a mechanical and functional definition standard) (February 1980).

EIA–470–A. Telephone instruments with loop signaling. Performance and technical criteria for connecting and interfacing various elements of the public telephone network.

EIA–491. Interface between a numerical control unit and peripheral equipment employing asynchronous binary data interchange over circuits having EIA–423–A electrical characteristics (October 1982).

EIA–496. Interface between data communication equipment (DCE) and the public switched telephone network (PSTN). ANSI approved (May 1984).

EIA–S30. High–speed 25–position interface for Data Terminal Equipment and Data Circuit Terminating Equipment. ANSI approved (March 1987).

V. CCITT. Code designation.

V.1. Equivalence between binary notation symbols and the significant conditions of a two–condition code.

V.2. Power levels for data transmission over telephone lines.

Network terms

V.3. International Telegraph Alphabet No. 5.

V.4. General structure of signals of International Telegraph Alphabet No. 5 code for data transmission over public telephone network.

V.5. Standardization of data–signaling rates for synchronous data transmission in the general switched telephone network.

V.6. Standardization of data–signaling rates for synchronous data transmission on leased telephone–type circuits.

V.7. Definition of terms concerning data communication over the telephone network.

V.10(X.26). Electrical characteristics for unbalanced double–current interchange circuits for general use with integrated circuit equipment in the field of data communications (and provisional amendments, May 1977).

V.11(X.27). Electrical characteristics for balanced double–current interchange circuits for general use with integrated circuit equipment in the field of data communications (and provisional amendments, May 1977).

V.15. Use of acoustic coupling for data transmission.

V.19. Modems for parallel data transmission using telephone signaling frequencies.

V.20. Parallel data transmission modems standardized for universal use in the general switched telephone network.

V.21. 300–bit/s full–duplex modem standardized for use in the general switched telephone network.

V.22. 1200 BPS full–duplex modem standardized for use in the general switched telephone network and on point–to–point two–wire leased telephone–type circuits.

V.22bis. 2400 BPS full–duplex modem using the frequency division technique standardized for use on the general switched telephone network and on point–to–point two–wire leased telephone–type circuits.

V.23. 600/1.2K BPS modem standardized for use in the general switched telephone network.

V.24. List of definitions for interchange circuits between data terminal equipment and data circuit terminating equipment (and provisional amendments, May 1977).

V.25. Automatic calling and/or answering equipment on the general switched telephone network, including disabling of echo suppressors on manually established calls.

V.25bis. Automatic calling and/or answering equipment on the general switched telephone network using the 100 series interchange circuits.

V.26. 2.4/1.2 KBPS modem standardized for use on four–wire leased telephone–type circuits.

V.26bis. 2.4/1.2 KBPS modem standardized for use in the general switched telephone network.

V.26ter. 2.4 KBPS full–duplex modem using the echo cancellation technique standardized for use on the general switched telephone network and on point–to–point two–wire leased telephone–type circuits.

V.27. 4.8 KBPS modem with manual equalizer standardized for use on leased telephone–type circuits.

V.27bis. 4.8 KBPS modem with automatic equalizer standardized for use on leased telephone–type circuits.

V.27ter. 4.8/2.4 KBPS modem standardized for use in the general switched telephone network.

V.28. Electrical characteristics for unbalanced double–current interchange circuits.

V.29. 9.6 KBPS modem standardized for use on point–to–point four–wire leased telephone–type circuits.

V.31. Electrical characteristics for single–current interchange circuits controlled by contact closure.

V.32. A family of two–wire, full–duplex modems operating at data signaling rates of up to 9600 BPS for use on the general switched telephone network and on leased telephone–type circuits.

V.35. Data transmission at 48 KBPS using 60– to 108–kHz group band circuits. V.36. Modems for synchronous data transmission using 60– to 108–kHz group band circuits.

V.37. Synchronous data transmission at a data signaling rate higher than 72 KBPS using 60–108 kHz group band circuits.

V.40. Error indication with electromechanical equipment.

V.41. Code independent error control system.

V.50. Standard limits for transmission quality of data transmission.

V.51. Organization of the maintenance of international telephone–type circuits used for data transmission.

V.52. Characteristics of distortion and error–rate measuring apparatus for data transmission.

V.53. Limits for the maintenance of telephone–type circuits used for data transmission.

V.54. Loop test devices for modems.

V.55. Specification for an impulsive noise measuring instrument for telephone–type circuits.

V.56. Comparative tests of modems for use over telephone–type circuits.

V.57. Comprehensive data test set for high data signaling rates.

V.100. Interconnection between public data networks (PDNs) and the public switched telephone network (PSTN).

V.110. Support of data terminal equipment (DTEs) with V–series type interfaces by an integrated services digital network (ISDN).

X

X. CCITT Recommendation designation.

X.1. International user classes of service in public data networks.

X.2. International user facilities in public data networks.

X.3. Packet assembly/disassembly facility (PAD) in a public data network.

X.4. General structure of signals of international alphabet no. 5 code for data transmission over public data networks.

X.20. Interface between data terminal equipment and data circuit–terminating equipment for start/stop transmission services on public data networks.

X.20bis(V.21). Compatible interface between data terminal equipment and data circuit–terminating equipment for start/stop transmission services on public data networks.

Network terms

X.21. General–purpose interface between data terminal equipment and data circuit–terminating equipment for synchronous operation on public data networks.

X.21bis. Use on public data networks of data terminal equipment that is designed for interfacing to synchronous V–series modems.

X.24. List of definitions of interchange circuits between data terminal equipment and data circuit–terminating equipment on public data networks.

X.25. Interface between data terminal equipment and data circuit–terminating equipment for terminals operating in the packet mode on public data networks (and provisional amendment, April 1977).

X.26. Electrical characteristics for unbalanced double–current interchange circuits for general use with integrated circuit equipment in the field of data communications (identical to V.10).

X.27. Electrical characteristics for balanced double–current interchange circuits for general use with integrated circuit equipment in the field of data communications (identical to V.11).

X.28. DTE/DCE interface for start/stop mode data terminal equipment accessing the packet assembly/disassembly facility (PAD) on a public network situated in the same country.

X.29. Procedures for exchange of control information and user data between a packet–mode DTE and a packet assembly/disassembly facility (PAD).

X.30. Standardization of basic model page–printing machine in accordance with International Telegraph Alphabet No. 5.

X.31. Characteristics, from the transmission point of view, at the interchange point between data terminal equipment and data circuit–terminating equipment in a 200 BPS start/stop data terminal.

X.32. Answer–back units for 200 BPS start/stop machines in accordance with International Telegraph Alphabet No. 5.

X.33. Standardization of an international text for the measurement of the margin of start/stop machines in accordance with International Telegraph Alphabet No. 5.

X.92. Hypothetical reference connections for public synchronous data net– works.

X.95. Network parameters in public data networks.

X.96. Call progress signals in public data networks.

X.500. A specification defining the universal interconnectivity of public electronic mail networks. X.500 implies a global directory for all of the different services, not just electronic mail; services include telephone, Telex, and other networks. X.500 is in its early stages of development.

X3.1. Synchronous signaling rates for data transmission.

X3.4. Code of information interchange.

X3.15. Bit sequencing of the American National Standard Code for Information Interchange in serial–by–bit transmission.

X3.16. Character structure and character parity sense for serial–by–bit data communication in the American National Standard Code for Information Interchange.

X3.24. Signal quality at interface between data processing technical equipment for synchronous data transmission.

X3.25. Character structure and character parity sense for parallel–by–bit communication in the American National Standard Code for Information Interchange.

X3.2. Procedures for the use of communication control characters of American National Standard Code for Information Interchange in specified data communications links.

X3.36. Synchronous high–speed data signaling rates between data terminal equipment and data communication equipment.

X3.41. Code extension techniques for use with seven–bit coded character set of American National Standard Code for Information Interchange.

X3.44. Determination of the performance of data communication systems.

X3.57. Message heading formats for information interchange using ASCII for data communication system control.

Networking acronyms

A

AAL ATM Adaptation Layer, two sublayers concerned with segmenting large PDUs into ATM cells; type 1 = CBR, 2 = VBR. See also SAR.

ABM Asynchronous Balanced Mode (layer 2).

ACD Automatic Call Distributor, PBX function or machine to spread calls among phones.

ACF Access Control Field, first byte in ATM header (802.6).

ACK Positive Acknowledgment, message or control bytes in a protocol (DtE + 1/0).

A/D Analog-to-Digital, usually a conversion of voice to digital formt.

ADCCP Advanced Data Communications Control Procedure, ANSI counterpart to HDtC.

ADCU Association of Data Communications Users.

ADM Add/Drop Multiplexer, node with 2 aggregates that supports data pass–through.

ADM Asynchronous Disconnected Mode (layer 2).

ADNS ARINC Data Network Service, a packet network.

ADPCM Adaptive Differential Pulse Code Modulation, a form of voice compression that typically uses 32 kbit/s.

ALS Active Line State, possible status of FDDI optical fiber.

AMI Alternate Mark Inversion, line coding for T–1 spans where 0 (space) is no voltage and successive 1s (marks) are pulses of opposite polarity. See also DMC, NRZ, 4B/5B.

AN Access Node.

ANSI American National Standards Institute, the US member of the ISO.

APDU Application PDU (OSI).

APS Automalic Protection Switch.

ARP Address Resolution Protocol, a way for routers to adjust addresses between different protocols or domains.

ARPA Advanced Research Projects Agency, created Arpanet packet network, folded into NSFnet in 1990.

ARQ Automatic Repeal reQuest, for retransmission; an error correction scheme for data links, used with a CRC.

ASCII American Standard Code for Information Interchange, based on 7 bits plus parity.

ASE Applications Service Element, protocol at upper layer 7 (SS7, OSI).

ASR Automatic Send/Receive, a printer with keyboard or a Teletype machine.

ATD Asynchronous Time Division, ETSI proposal for pure cell relay, without SONET or other framing.

ATM Asynchronous Transfer Mode, a type of framing used in BISDN and SONET.

AU Administrative Unit, payload plus pointers (SDH).

AUG AU Group, one or more AUs to fill an STM (SDH).

AWG American Wire Gauge, conventional designator of wire size.

B

B Bearer channel, a DS–0 for user trafrlc.

BCC Block Check Code, a CRC or similarly calculated number to find transmission errors.

BCD Binary Coded Decimal, 4–bit expression for 0 (0000) to 9 (1001).

BCM Bit Compression Mux, same as M44 for ADPCM.

BCN Beacon, frames sent downstream by station on ring when upstream input is lost (802.5).

B-DCS Broadband Digital Cross–connect System, DACS OC–1, STS–1, DS–3 and higher rates only (see W–DCS).

BER Bit Error Ratio, errored bits over total bits; should be < 1^{-7} for transmission lines.

BERT Bit Error Ralc Test(er).

BIP Bit Interleaved Parity, error checking method (BIP8 in SONET).

BISDN Broadband ISDN, generally access at more than 100 Mbit/s.

BISYNC Binary Synchronous communications, a protocol.

BITS Building Integrated Timing Supply, stratum 1 clock in CO.

BNS Broadband Network Switch, usually ATM or packet based, DS–3 and faster.

BOC Bell Operating Company, a telephone company.

bps Bits per second, serial digital stream data rate, now bit/s.

BPV Bipolar Violation, two pulses of the same polarity in a row.

BRA Basic Rate Access, ISDN 2B+D loop.

BRI Basic Rate Interface, 2B+D on one local loop.

BSC Binary Synchronous Communications, a half-duplex protocol.

BSS Broadband Switching System, cell-based CO switch for B-ISDN.

BWB Bandwidth Balancing, method to reduce a station's access to a transmission bus, to improve fairness (802.6).

C

C Capacitance, the property of a device that holds an electrical charge.

CASE Common Application Service Elements, application protocol (MAP).

CBR Constant (Continuous) Bit Rate, channel or service in ATM network for voice or sync data in a steady flow.

CBX Computerized Branch eXchange, PABX.

CCITT Comite Consultatif Internationale de Telegraphique et Telephonique, The International Telegraph and Telephone Consultative Committee, part of ITU.

CCIR International Radio Consultative Committee, sister group to CCITT.

CCR Commitment, Concurrency and Recovery (OSI).

CCS Common Channel Signaling.

CCSA Common Control Switching Arrangement.

Networking acronyms

CCS6 CCS system 6, first out of band signaling system in N.A. (CCIS).

CD Carrier Detect, digital output from modem when it receives analog modem signal.

CD Count Down, a counter that holds the number of cells queued ahead of the local message segment (802.6).

CDMA Code Division Multiple Access, spread spectrum; broadcast frequency changes rapidly in pattern known to receiver.

CELP Code-Excited Linear Predictive coding, a voice compression algorithm used at 8 kbit/s.

CEPT Conference on European Posts & Telecommunications (Conference of European Postal and Telecommunications administrations), a body that sets policy for services and interfaces in 26 countries.

CFA Carrier Failure Alarm, detection of red (local) or yellow (remote) alarm on T-1.

CGA Carrier Group Alarm, trunk conditioning applied during CFA.

CIT Computer Integrated Telephony, DEC's PHI.

CL Common Language, Bellcore codes to identify equipment, locations, etc.

CL ConnectionLess.

CLLM Consolidated Link Layer Management (802).

CLN Connectionless Network, packet address is unique and network routes all traffic.

CLNP Connectionless mode Network (layer) Protocol (SONET).

CLTS Connectionless Transport Service, OSI datagram protocol.

CMA Communications Managers Association.

CMDR Command Reject, similar to FRMR (HDLC).

CMI Coded Mark Inversion, line signal for STS–3.

CMIP Constanl Mark, Inverted; line coding for T–1 local loop in Japan.

CMIP Common (network) Management Information Protocol, part of the OSI network management scheme, connection oriented .

CMIS Common (network) Management Information Service, runs on CMIP (OSI).

CMISE CMIS Element.

CMOS Complementary Metal Oxide Semiconductor, low power method (lower than NMOS) to make ICs.

CMOT CMIP over TCP/IP.

CMT Connection Management, part of SMT that establishes physical link between adjacent stations (FDDI).

CO Central Office, of a phone company, where the switch is located; the other end of the local loop opposite CP.

COC Central Office Connection, separately tariffed part of T–1 circuit within a CO.

COCF Connection Oriented Convergence Function, MAC–layer entity.

CODEC COder–DECoder, converts analog voice to digital, and back.

COFA Change of Frame Alignment, movement of SPE within STS frame.

CO-LAN Central Office Local Area Network, a data switching service based on a data PBX in a carrier's CO.

CONP Connection mode Network layer Protocol.

COS Class Of Service.

Interconnection Networking in Europe.

COT Central office Terminal, equipment at CO end of digital loop or line.

CP Central Processor, CPU that runs network under center–weighted control.

CP Customer Premises, as opposed to CO.

CPE Customer Premises Equipment, hardware in user's office.

CPI Computer–PBX Interface, a data interface between NTI and DEC.

CPN Customer Premises Node, CPE.

CPU Central Processor Unit, the computer.

CR Carriage Return, often combined with a line feed when sending to a printer.

CRC Cyclic Redundancy Check, an error detection scheme, used with ARQ.

CRV Coding Rule Violation, unique bit signal for F bit in frame 1 of CMI.

CS Convergence Sublayer, where header and trailer are added before segmentation.

CSC Circuit–Switched Channel (Connection).

CSMA Carrier Sense Multiple Access, a LAN transport method, usually with "/CD" for collision detection or "/CA" collision avoidance.

CSPDN Circuit Switched Public Data Network.

CS–PDU Convergence layer PDU, info plus new header and trailer to make packet that is segmented into cells or SUs.

CSU Channel Service Unit, the interface to the T–1 line that terminates the local loop.

CTS Clear To Send, lead on interface indicating DCE is ready to receive data.

CV Coding Violation, transmission error in SONET section.

CVSD Continuously Variable Slope Delta modulation, a voice encoding technique offering variable compression.

D

D Delta (or Data) channel, 16 kbit/s in BRI, 64 kbit/s in PRI, used for signaling (and perhaps some packet data).

D3 Third generation channel bank, 24 channels on one T–1.

D4 Fourth generation digital channel bank, up to 48 voice channels on two T–1's or one T–1C.

D5 Fifth generation channel bank with ESF.

DA Destination Address, field in frame header (802).

D/A Digital-to-Analog, decoding of voice signal.

D/A Drop and Add, similar to drop and insert.

DACS Digital Access and Cross–connect System, a digital switching device for routing T–1 lines, and DS–O portions or lines, among multiple T–1 ports.

Networking acronyms

DARPA Defense ARPA, formerly just ARPA.

DAS Dual–Attached (Access) Station, device on main dual FO rings, 4 fibers (FDDI).

DASS Digital Access Signaling System, protocol for ISDN D channel in U.K.

dB Decibel, 1/10th of a bel; 10 log (x/y) where x/y is a ratio or like quantities (power).

dBm Decibel level referenced to 1 mW at 1004 Hz into 600 ohms impedance.

dBm0 Power that would be at zero TLP reference level, = measurement – (TLP at that point).

dBrn Power level relalivc to noise, dBm + 90.

dBrnC dBrn through a C–weighted audio filter (matches ear's response).

DB25 Code for 25–pin connector specified for RS–232 I/F.

D.C. Direct Current, used for some signaling forms; type of power in CO.

DCC Data Communications Channel, overhead connection in D bytes for SONET management.

DCE Data Circuit–terminating Equipment, see next DCE.

DCE Data Communications Equipment, 'gender' of interface on modem; see DTE.

DCS Digital Cross–connect System, DACS.

DDCMP Digital Data Communications Message Protocol.

DDD Direct Distance Dialing, refers to PSTN.

DDS Digital Data System, network that supports DATAPHONE Digital Service.

DDSD Delay Dial Start Dial, a start–stop protocol for dialing into a CO switch.

DES Data Encryption Standard, moderately difficult to break.

D/I Drop and Insert a mux function or type.

DIP Dual In–line Package, for chips and switches.

DIS Draft International Standard, preliminary form of OSI standard.

DISC Disconnect, command frame sent between LLC entities (layer 2).

DLC Data Link Connection, one logical bit stream in LAPD (layer 2).

DLC Digital Loop Carricr, mux system to gather analog loops and carry thcm to CO.

DLCI Data Link Connection Identifier, address in a frame (I.122).

DLE Data Link Escape, ESC.

DLL Data Link Layer, layer 2 (OSI).

DM Disconnected Mode, LLC frame to reject a connection request (layer 2).

DMC Differential Manchester Code, pulse pattern that puts transition at center of each bit time for clocking, transition [none] at start of period for 0 [1] (802.5).

DMI Digitally Multiplexed Interface, AT&T interface for 23 64 kbit/s channels and a 24th for signaling.

DMPDU Derived MAC Protocol Data Unit, a 44–octet segment of upper layer packet plus cell header/trailer (802.6); see L2PDU.

DMS Digital Multiplex System.

DNA Digital Network Architecture, DEC's networking scheme.

DNIC Data network Identification Code, assigned like an area code to public data networks.

DNIC Data Network Interface Circuit, 2B+D ISDN U interface.

DNIS Dialed Number Identification Service, where carrier delivers number of called extension after PBX acknowledges call.

DNR DCE Not Ready, signaling bit in CMI.

DoV Data over Voice, modems combine voice and data on one twisted pair.

DP Dial Pulse, rotary dialing rather than DTMF.

DPBX Data PBX, a switch under control of end users at terminals.

DPCM Differential Pulse Code Modulation, voice compression algorithm used in ADPCM.

DPNSS Digital Private network Signaling System, PBX interface for common channel signaling.

DPO Dial Pulse Originate, a form of channel bank plug–in that accepts dial pulses.

DPT Dial Pulse Terminate, a channel bank plug that outputs pulses.

DQDB Distributed Queue Dual Bus, an IEEE 802.6 protocol to access MAN's, typically at T–1, T–3, or faster.

DS–0 Digital Signal level 0, 64,000 bit/s, the worldwide standard speed for PCM digitized voice channels.

DS–OA Digital Signal level 0 with a single rate adapted channel.

DS–0B Digital Signal level 0 with multiple channels sub–rate multiplexed in DDS format.

DS–1 Digital Signal level 1, 1.544 Mbit/s in North America, 2.048 Mbit/s in CCITT countries.

DS–1A Proposed designation for 2.048 Mbit/s in North America.

DS–1C Two T–1's, used mostly by Telcos internally.

DS–2 Four T–1's, little used in US, common in Japan.

DS–3 Digital Signal level 3, 44.736 Mbit/s, carrying 28 T–1's.

DSAP Destination Service Access Point, address field in header of LLC frame to identify a user within a station address (layer 2).

DSI Digital Speech Interpolation, a voice compression technique that relies on the stalistics of voice traffic over many channels.

DSP Digital Signal Processor, specialized chip optimized for fast computations.

DSP Display System Protocol, protocol for faster bisync traffic over packet nets.

DSR Data Set Ready, signal indicating DCE and line ready to receive data.

DSSI D–channel Signaling System 1, access protocol for switched connection signaling (Q.931 & ANSI T1S1/90–214).

Networking acronyms

DSU Digital (Data) Service Unit, converts RS–232 or other terminal interface to line coding for local loop transmission.

DTAU Digital Test Access Unit, CO equipmcnt on T–1 line.

DTE Data Terminal Equipment, 'gender' of interface on terminal or PC; scc DCE.

DTMF Dual Tone Multi–Frequency, TOUCHTONE dialing, as opposed to DP.

DTR Data Terminal Ready, signal that terminal is ready to receive data from DCE.

DVI Digital Video Interactive, applications with large, bursty bandwidth.

DX Duplex, a 2–way audio channel bank plug without signaling.

E

E–1 European digital signal level 1, 2.048 Mbit/s.

E&M Signaling leads on a voice tie line, known as Ear and Mouth.

EBCDIC Extended Binary Coded Decimal Interchange Code, extended character SCI on IBM hosts.

EC Error Correction, process to check packets for errors and send again if needed.

ECC Error Checking Code, 2 bytes (usually) in frame or packet derived from data to let receiver test for transmission errors.

ECL Emilter Coupled logic, transislor clrcuit type optimized for high speed.

ECN Explicit Congestion Notification, network warns terminals of congestion by setting bits in frame header (I.122).

ECO Engineering Change Order, document from designer ordering change in product.

ED Ending Delimiter, unique symbol to mark end of LAN frame (TT in FDDI, HDLC flag, etc.).

EDI Electronic Document (Data) Interchange, transfer of business information (P. 0., invoice, etc.) in defined formats.

EGP Exterior Gateway Protocol, on the Internet (TCP/IP).

EIA Electronic Industries Association, publisher of standards (e.g. RS–232).

EMI Electro Magnetic Interference.

EMS Element Management System, usually a vendor–specifIc NMS for a hardware domain (OSI).

ENQ Enquiry, control byte that requests a repeat transmission or control of line.

EOC Embedded Operation Channel, D bytes devoted to alarms, supervision, and provisioning (SONET).

EOM End of Message.

EOT End Of Transmission, control byte; preceded by DLE indicates switched station going on hook.

ERL Echo Return Loss.

ERS Errored Second, a 1 sec. interval containing 1 or more transmission errors.

ESB Errored Second type B, new name for bursty ES.

ESC Escape, an ASCII character.

ESD ElectroStatic Discharge, electrical "shock" from person or other source that can destroy semiconduclors.

ESS Electronic Switching System, a CO switch.

ETC End of Transmission Block, control byte in BSC.

ETN Electronic Tandem network.

ETO Equalized Transmit Only, voice interface with compensation to correct for frequency response of the line.

ETX End of Text, control byte.

F

F Final, control bit in frame header (layer 2).

F Framing, bit position in TDM frame where known pattern repeats.

FACS Facility Assignment Control System, for telco to manage outside plant (local loops).

FAD Frame Assembler/Disassembler, functIons like a PAD, but for frames.

FADU File Access Data Unit (OSI).

FAS Frame Alignment Signal, bit or byte used by receiver to locate TDM channels.

FAX Facsimile.

FB Framing Bit.

FC Frame Control, field to define type or frame (FDDI).

FCC Federal Communication Commission, regulates communications in US.

FCOT Fiber oplic Central Office Terminal.

FCS Frame Check Sequence, error checking code (layer 2).

FDDI Fiber Distributed Data Interface, 100 Mbit/s FO standard for a LAN or MAN.

FDL Facility Data Link, part of the ESF framing bits available for user data, in some cases.

FDM Frequency Division Multiplexer.

FDX Full Duplex.

F_C Extended framing ("F sub c"), old name for ESF.

FEC Forward Error Correction, using redundancy in a signal to allow the receiver to correct transmission errors.

FEP Front End Processor, peripheral computer to mainframe CPU, handles communications.

FEXT Far End Cross Talk.

FIB Forward Indicator Bit, field in SUs (SS7).

FID Format Identification, bit C–1 in DS–3 format shows if M13, M28, or Syntran signal.

FIFO First In First Out, buffer type that delays bit stream.

FISU Fill–In Signaling Unit, 'idle' packet that carries ACKs as sequence numbers (SS7).

FITL Fiber In The Loop, optical technology from CO to customer premises.

Networking acronyms

FIX Fcdcral Interncl Exchangc, point or interconnection for U.S. agency research networks.

FO Fibcr Optic, bascd on optical cable.

FOTP Fiber Optic Test Procedure.

FOTS Fiber Optic Terminal System, mux or CO switch interface.

FPDU FTAM PDU.

FPDU Frame relay protocol Data Unit (I.122).

FR Frame Relay, interface to simplified packetized switching network (I.122).

FRS Frame Relay Switch.

FRMR Frame Reject, LLC response to error that cannot be corrected by ARQ, may cause reset or disconnect (layer 2).

FS Failed Second, now called UAS.

FSN Forward Sequence Number, sent sequence number of this SU/packet (SS7).

FT–1 Fractional T–1, digital capacity of N x 64 kbit/s but usually less than 1/2 a T–1.

FTAM File Transfer, Access, and Management; an OSI layer–7 protocol for LAN interworking (802).

FTP File Transfer Protocol (TCP/IP)

FLLC Fiber To The Curb, local loop is fibcr from CO to just outside CP, wire into CP.

G

G3 Group 3, analog facsimile standard at up to 9.6 kbit/s.

G4 Group 4, digital facsimile standard at 56/64 kbit/s.

Gbit/s Giga bit/s per second, billions (10^9) per second.

GOSIP Government OSI Profile, suite of protocols mandated for US Federal and U.K. contractors; –T = Transport model; –A = Application model.

GPS Global Positioning System, satellites that report exact time

GS Ground start, analog phone interface.

GSM Group Special Mobile, part of CEPT working on cellular.

GSTM General Switched Telephone Network, CCITT term to replace PSTN after 1990's privatizations.

H

H Halt, line State symbol (FDDI).

H_X High–speed bearer channel (ISDN).

H_0 384 kbit/s.

H_1 1.536 Mbit/s (N. Amer.) or 1.920 Mbit/s (CEPT areas).

H_{11} 1.536 Mbit/s (N. Amer.).

H_{12} 1.920 Mbit/s (CEPT areas).

H_2 DS–3 (N. Amer.) or 32.768 Mbit/s.

H_{21} 32.768 Mbit/s (CEPT).

H_{22} DS–3 (N. Amer.) (or 43 to 45 Mbit/s).

H_3 Would have been 60–70 Mbit/s but left undefined for lack of interest.

H_4 132.032 to 138.240 Mbit/s.

HCM High Capacity Multiplexing, 6 channels of 9600 in a DS–0.

HCS Header Check Sequence, CRC on header fields only, not on info; HEC (ATM).

HCV High Capacity Voice, 8 or 16 kbit/s scheme.

HDB3 High Density Bipolar 3–zeros, line coding for 2 Mbit/s lines replaces 4 zeros with BPV (CEPT).

HDLC High–level Data Link Control, layer–2 full–duplex protocol.

HDSL High bit–rate Digital Subscriber Line, proposal to T1E1 for way to duty T–1 over local loops without repeaters.

HDTV High Definition Television, double resolution TV image and candidate application for broadband networks.

HEC Header Error Control, ECC in ATM cell for header, not data. (See HCS)

HEL Header Extension Length, the number of 32–bit words in HE (802.6).

HIPPI HIgh–speed Peripheral Parallel Interface, computer channel simplex interface clocked at 25 MHz; 800 Mbit/s when 32 bils wide, 1.6 Gbit/s when 64 bits.

HLM Heterogeneous LAN Management, OSI NMS protocol specification without layers 3–6, developed by IBM and 3Com to save memory in workstations.

HOB Head Of Bus, station and function that generates cells or slots on a bus (DQDB).

HOPS Horizontally Oriented protocol Structure, proposal for high performance interfaces at broadband rates.

HPR High Peformance Routing, a form of dynamic call routing In the PSTN.

HRC Hybrid Ring Control, TDM sublayer at bottom of data link (2) that splits FDDI into packet– and circuit switched parts.

HSSI High Speed Serial Interface, of 600 or 1200 Mbit/s.

HSPS High Speed Peripheral Shelf.

Hz Herz, cycles/second.

I

I I class central office switch is not in HPR network.

I Idle, line state symbol (FDDI).

I Information, type of layer 2 frame that carries user data.

IAB Internet Activities Board, defines LAN standards like SNMP.

IBR Intermediate bit Rate, between 64 and 1536 kbit/s; fractional T–1 rates.

IC Integrated Circuit.

ICCF Industry Carriers Compatibility Forum.

ICMP Internal Control Message protocol, reports to a host errors detected in a router by IP.

IDF Intermediate Distribution Frame.

Networking acronyms

idle Integrated Digital Loop Carrier, combination or RDT (remote MUX), transmission facility, and IDT to feed voice and data into a CO switch.

IDT Integrated Digital Terminal, M24 function in a CO switch to terminate a T–1 line from RDT.

IEC International Electrotechnical Commission, standards body.

IEEE Institute or Electrical and Electronics Engineers, Inc.: engineering society that sets standards.

I/F Interface.

IG ISDN Gateway (AT&T).

IGRP Interior Gateway Routing Protocol, learns best routes through LAN (TCP/IP).

ILS Idle Line State, presence of idle codes on optical fiber line (FDDI).

IMD InterModulation Distortion.

IMPDU Initial MAC PDU, the SDU received from LLC with additional header/trailer to aid in segmentation and reassembly (802.6).

IN Intelligent Network.

IND Indication (OSI).

INE Intelligent Network Element.

I/O Input/Output.

IR InfraRed, light with wave length longer than red like 1300 nm used over fiber.

ISDN Integrated Services Digital Network.

ISDN–UP ISDN User Part, protocol from layer 3 and up for signaling services for users Q.761–Q.766 (SS7).

ISDU Isochronous Service Data Unit, upper layer packet from TDM or circuit–switched service (802.6).

ISI Inter–Symbol Interference, source of errors where pulses (symbols) spread and overlap due to dispersion.

ISO International Standards Organization (International Organization for Standardization). ANSI is US member.

ISSI Inter–Switching System Interface, between nodes in a public network, not available to CPE (e.g. SMDS to B–ISDN).

ISSIP ISSI Protccol.

ISUP ISDN User Part.

ITB End of Intermediate Transmission Block, control byte in BSC.

IWF InterWorking Function, the conversation process between FR and X.25, etc.

IWWU InterWorking Unit, adapter between circuit– and packet–based switches; e.g., SMDS and SONET.

J

J Non–data character for starting delimiter (11000) in 4B/5B coding (802.6).

JB7 Jam Bit 7, force bits in position 7 within a DS–0 to 1 for 1's density.

K

K Non–data character for starting delimiter (10001) in 4B/5B coding (802.6).

kbit/s Thousands of bits per second

KG Key Generator (Krypto Gear), encryption equipment from NSA.

kHz Kilohertz, thousands of cycles per second.

L

L2–PDU Layer 2 Protocol Data Unit, fixed length cell (SMDS).

L3–PDU Layer 3 Protocol Data Unit, a variable length packet at OSI level 3.

LADT Local Area Data Transport, telco circuit on copper pair.

LAN Local Area Network.

LAP Link Access Procedure, layer 2 protocol for error correcting.

LAPB LAP Balanced, HDLC protocol for data sent into X.25 network, etc.

LAPD Varian~ or tAPB lor ISDN D channels.

LAPD+ LAPD protocol for other than D channels, e.g. B channels.

LAPM LAP Modem, part of V.42 modem standard.

LAT Local Area Transport, DECnet protocol for terminals.

LATA Local Access and Transport Area, a geographic region. The LEC can carry all traffic within a LATA, but nothing between LATA's.

LC Local Channel, the local loop.

LCI Logical Connection Identifier, short address in connection–oriented frame.

LCN Logical Channel Number, form of address in a packet.

LDM Limited Distance Modem.

LED Light Emitting Diode, semiconductor used as light source in FO transmitters.

LLB Local Loop Back.

LLC Logical Link Control, the upper sublayer of the OSI data link layer (layer 2).

LLC1 Connection oriented LLC. LLC2 Connectionless LLC.

LME Layer Management Entity, the process that controls configuration, etc. (802.6).

LMI Local Management Interface, transport specification for frame relay that sets way to assign DLCIs, etc.

LOF Loss Of Frame, condition where mux cannot find framing, OOF, for 2.5 sec.

LOFC Loss of Frame Count, number of LOFs.

LOP Loss of Pointer, SONET error condition.

LOS Loss Of Signal, incoming signal not present (no rceivcd data).

LPC Linear Predictive Coding, voice encoding technique.

LSAP Link layer Service Access Point, logical address of boundary between layer 3 and LLC sublayer in 2 (802).

LSB Least Significant Bit, position in byte with smallest value.

Networking acronyms

LSSU Link Status Signaling Unit, control packet at layer 3 (SS7).

LSU Line State Unknown, possible report from FDDI line state monitor.

LTE Line Terminating Equipment, SONET nodes that switch, CLC, and so create or take apart an SPE (SONET).

LU Logical Unit, upper level protocol in SNA.

LU6.2 Set of services that support program-to-program communications at levels 4–6.

M

M Million when used as prefix to abbreviation: Mbit/s.

m Milli (1/1000) when used as prefix: mm = millimeter

m Meter (39.37 inches)

M13 Multiplexer between DS–1 and DS–3 levels.

M24 Multiplexer function between 24 DS–O channels and a T–1, a channel bank.

M28 Same as M 13, but different format, not compatible.

M41 Multiplexer function to put 44 ADPCM channels into one T–1; four bundles, each of one common signaling channel with 11 voice channels; transcoder or BCM.

M48 Multiplexer function to put 48 ADPCM channels into one T–1; signaling in each voice channel.

M55 ADPCM multiplexer that puts SS voice channels in five bundles on an E–1.

MAC Medium (Media) Access Control, the lower sublayer of the OSI data link layer.

MAN Metropolitan Area Network, typically 100 M bi t/s.

MAP Manufacturing Automation Protocol, for LANs; closely related to TOP, and written MAP/TOP (802.4).

MAU Media Access Unit, device attached physically to cable (802.3 layer 1).

MAU Multiple (Multistation) Access Unit, hub device in a LAN (802.5).

Mbit/s Megabit (1,00,00 bits) per second.

MCF MAC Convergence Function, how an SDU is framed into a packet (PDU), segmented, and loaded into cells (802.6).

MCP MAC Convergence Protocol, segmentation and reassembly procedure to put MSDUs into cells (802.6).

MDDB Multi–Drop Data Bridging, digital bridging of PCM encoded modem signals, equivalent to analog bridging.

MDF Main Distribution Frame, large CO wire rack for low speed data and voice cross connects.

MDI Medium Dependent Interface, link between MAU and cable (802 layer 1).

MF Multi–Frequency, tone signaling on analog circuits.

MFA MultiFrame Alignment, code in time slot 16 of E–1 to mark start of superframe.

MHS Message Handling System, OSI store and forward protocol.

MHz Megahertz, million cycles per second.

MIB Management Information Base, OSI defined description of a network for management purposes (SNMP, IP).

MIC Media Interface Connector, dual–fiber equipment socket and cable plug FDDI).

MIS Management Information Systems, dept. that runs the big computers.

MNP Microcom Networking Protocol, error correction in modems.

modem MOdulate/DEModulate, modulate analog signal from digital data and reverse.

MPDU MAC PDU (802.6).

MPL Maximum Packet Lifetime, number of hops allowed before packet is discarded.

ms Millisecond, I/l000 second.

M/S Master/Slave, relationship in a protocol where master always issues commands and slave only responds.

MSAP MAC Service Access Point, logical address (up to 60 bits) of boundary between MAC and LLC sublayers (802).

MSDU MAC Service Data Unit, data packet in LAN format; may be long and variable length before segmentation into cells.

MSS MAN Switching System.

MTBF Mean Time Between Failures, average for one device.

MTS Message Toll Service, normal dial up phone service.

MUX Multiplexer.

N

n Nano, prefix meaning 10^{-9} of the unit as nln = 10^{-9} meter.

NAK Negative Acknowledgment, protocol control byte indicating error.

NAS Network Applications Solutions, set of DEC APIs for communication.

NAU Network Addressable Unit, device or process running an SNA protocol stack.

NCB Network Control Block, command packet in SNMP.

NCB Network Control Block, transport protocol in LAN Manager (level 4).

NCC Network Control Center.

NCI Network Control Interface.

NCP Network Control Point, for SDN and AT&T switched network.

NCTE Network Channel Terminating Equipment; first device at CP end of local loop; e.g., CSU.

NDF New Data Flag, inversion of some pointer bits to indicate change in SPE position in STS frame (SONET).

NE Network Element

NEBS Network Equipment–Building Standards, Bellcore generic spec for CO equipment (TR63).

NEXT Near End Cross Talk, interference on 2–wire interfaces from sent signals leaking back into the receiver.

Networking acronyms

NFS Network File System, protocol for file transfers on a LAN.

NFS Network File Server, computer with shared storage, on a LAN.

NI Network Interface; demarcation point between PSTN and CPE.

NIC Network Interface Card, add–in card for PC, etc. to connect to LAN.

NID Network IDentification, field in network level header (MAP).

NISDN Narrowband ISDN, access at T-1 or less.

NM Network Management.

NME NM Element.

NMOS N–channel Metal Oxide Semiconductor, common IC type uses more power than CMOS.

NMP Network Management Protocol.

NMS Network Management System.

NNI Network–Node Interface, point-to-point interface between two switches for SDH, SONET, or B–ISDN network.

NPDU Network PDU, Layer 3 packet (OSI).

NR Number Received, control field sequence, tells sender the N_S that receiver expects in next frame (Layer 2).

NRZ Non–Return to Zero, signal transitions from positive to negative without assuming 0 value. See also DMC, AMI.

NRZI NRZ Invert on ones, coding changes polarity to indicate '1' and remains unchanged for '0.'

ns Nanosecond, 10^{-9} second.

NS Number Sent, sequence number of frame in its control field; determined by sender.

NSA Non–Service Affecting, fault that does not interrupt transmission.

NSAP Network Service Access Point,

NSC Network Service Center, for SDN.

NT–1 Network Termination 1, the first device on the CP end of the local loop (like the CSU).

NT–2 Network Termination 2, the second CP device, like the DSU (TSDN).

NTN Network Terminal Number, address of terminal on data network, part of global address with DMC (X.121).

NTSC National Television Standards Committee, group and format they defined for U.S. TV broadcasting.

NUI Network/User Interface.

O

OA&M Operations, Administration, and Maintenance.

OAM&P Operations, Administration, Maintenance, & Provisioning, telco housekeeping.

OC–1 Optical Carrier level I, SONET rate of 51.84 Mbit/s, matches STS–1.

OC–3 Optical Carrier level 3, SONET rate of 155.52 Mbit/s, matches STS–3.

OC–N Higher SONET levels, N times 51.84 Mbit/s.

OCU Office Channel Unit, "CSU" in the CO; also called OCR.

OCU–DP OCu–Data Port, channel bank plug I/0 to 4– wire local loop and CSU on CP.

OF Optical Fiber.

OLTP On Line Transaction Processing.

ONA Open Network Architecture, FCC plan for equal access to public networks.

ONI Operator Number Identification.

OOF Out Of Frame, mux is searching for framing bit pattern.

OOS Out Of Synchronization; multiplexers can't transmit data when OOS.

OPR Optical power received, by a FO termination.

ORL Optical Return Loss.

OS Operating System, main software to run a CPU.

OSI Open Systems Interconnection, a 7–layer model for protocols defined by the ISO.

OSI/NMF OSI Network Management Forum, standards group for NM protocols.

OSIone Global organization to promote OSI standards.

OSI TP OSI Transaction Processing, a protocol.

OTDR Optical Time Domain Reflectometry (Reflectometer), method (tester) to locate breaks in OF.

OW Order Wire, DS–0 in overhead intended for voice path to support maintenance.

P

PA Preamble, a period of usually steady signal ahead of a LAN frame, to set timing, reserve the cable, etc.

PA Pre–Arbitrated, portion of traffic on DQDB MAN with assigned bandwidth, usually isochronous connections (802.6).

PABX Private Automated Branch eXchange, electronic PBX.

PAD Packet Assembler/Disassembler, device to convert between packets (X.25, etc.) and sync or async data.

PAL Programmable Array Logic, large semi–custom chip.

PAM Pulse Amplitude Modulation; used within older channel banks.

PARIS Packetized Automated Routing Integrated System, fast switch developed by IBM.

PBX Private Branch eXchange, small phone switch inside a company, manual or automatic.

PC Path Control, level 3 in SNA for network routing.

PCM Pulse Code Modulation, the standard digital voice format at 64kbit/s.

PCN Personal Communications Network, second generation cellular system.

PCR Preventive Cyclic Retransmission, error correction procedure that repeats packets whenever link bandwidth is available (SS7).

PDG Packet Data Group, 12 octets in FDDI frame (outside of WBCs) not assignable to circuit–switched connections.

PDH Pleisiochronous Digital Hierarchy, present multiplexing scheme from T-1 to T–3 and higher, contrast with SDH.

Networking acronyms

PDN Public Data Network; usually packetized.

PDS Premises Distribution System, the voice and data wiring inside a customer office.

PDU Protocol Data Unit, information packet (ADDR, CTRL, INFO) passed at one level between protocol stacks (OSI).

pel Picture Element, the smallest portion of a graphic image encoded digitally.

P/F Poll/Final, bit in control field of LLC frames to indicate receiver must acknowledge (P) or this is last frame (F) (Layer 2).

PHY PHYsical, layer 1 of the OSI model.

PI Primary In, FO port that receives light from main fiber ring (FDDI).

PIN Positive–Intrinsic–Negative, type of semiconductor photo detector.

PL Pad Length, number (0–3) of octets of 0s added to make Info field a multiple of 4 octets (802.6)

PL Physical Layer, level 1 in OSI model.

PL Private Line, a dedicated leased line, not switched.

PL Performance Loop Back, LB done at point of ESF performance function in CPE.

PLCP Physical Layer Convergence Protocol (Procedure), part of PHY that adapts transmission medium to handle a given protocol sublayer (DQDB).

PLL Phase Locked Loop, electronic circuit that recovers clock timing from data.

PLP Packet Layer Protocol, at Layer 3 like X.25.

PLS Physical Link Signaling, part of layer 1 that encodes and decodes transmissions, e.g. Manchester coding (IEEE 802).

PMA Physical Medium Attachment, electrical driver for specific LAN cable in MAU, separated from PLS by AUI (802.3).

PMD Physical Layer, Medium Dependent, a sublayer in layer 1 (below PLS) of LAN protocols; also PMA (802).

PO Primary Out, FO port that sends light into the main fiber ring (FDDI).

POF Plastic Optical Fiber, for short distances rather than glass for long haul.

POH Path OverHead, bytes in SDH for channels carried between switches over multiple lines and through DCCs.

POP Point Of Presence; end of IXC portion of long–distance line at central office (Tel).

POS Point of Sale.

POTS Plain Old Telephone Service, residential type service.

PPDU Presentation (Layer) PDU (OSI).

ppm Parts Per Million.

PPP Point-to-Point Protocol, non–proprietary interface on routers for WAN links.

pps Pulses Per Second, speed of rotary dialing dial pulses.

PRC Primary Reference Clock, GPS–controlled rubidium oscillator used as stratum 1 source.

PRA Primary Rate Access, via PRI for ISDN.

PRBS PseudoRandom Bit Sequence, fixed bit pattern, for testing, that looks random.

PRI Primary Rate Interface; 23B+D (T–1) or 30B+D (CEPT).

PRS Primary Rate Source, stratum 1 clock.

PSI Primary Subnet Identifier, part of address in network level header (MAP).

PSN Packet Switched Network.

PSPDN Packet Switched Public Data Network.

PSTN Public Switched Telephone Network, the telco–owned dial–up network.

PTE Path Terminating Equipment, SONET nodes on ends of logical connections.

PTAT Private Trans–Atlantic Telephone, cable from US to U.K., Ireland, and Bermuda.

PUB AT&T Technical PUBlication, Bell System de facto standard.

PUC Public Utilities Commission, state body that regulates telephones, also PSC.

PVC Permanent Virtual Circuit, assigned connection over a packet/frame network, not switchable by user.

Q

Q Quiet, line state symbol (FDDI).

QA Queued Arbitrated, portion of packet traffic that contends for bandwidth (DQDB).

QOS Quality of Service.

QPSX Queued packet Synchronous eXchange, old name for DQDB; QPSX Systems Inc. originated it in Australia.

Q.921 CCITT recommendation for level 2 protocol in signaling system 7.

Q.931 CCITT recommendation for level 3 protocol in signaling system 7.

R

R Interface reference point in the ISDN model to pre–ISDN phones and terminals.

R Ring, one of the conductors in a standard twisted pair, 2–wire local loop (the one connected to the 'ring', the second part of a phone plug) or the DTE–to–DCE side of a 4–wire interface.

R1 Ring, or R lead of the DCE–to–DTE pair in a 4–wire interface.

RACE Research for Advanced Communications in Europe, program to develop broadband.

RAI Remote Alarm Indication.

RARP Reverse ARP, Internet protocol to let diskless workstation learn its IP address from a server (TCP/IP).

RBOC Regional Bell Operating Company, one of about 22 local telephone companies formerly part of Bell System.

RBS Robbed Bit Signaling, in PCM.

RD Receive Data, lead on electrical interface.

Networking acronyms

RD Request Disconnect, secondary station unnumbered frame asking primary station for DISC (Layer 2).

RDA Remote Database Access, service element (OSI).

REJ Reject, S-format LLC frame acknowledges received data units while requesting retransmission from specific errored frame (Layer 2).

RELP Residually-Excited Linear Predictive Coding, voice encoding scheme (8–16kBit/s).

REQ Request (OSI).

RF Radio Frequency.

RFI Radio Frequency Interference.

RFT Remote Fiber Terminal, equivalent to SLC96.

RI Ring Indicator, digital lead on modem tells DTE when call comes in.

RI Routing Indicator, bit in LAN packet header to distinguish transparent- from source-routed packets.

RIM Request Initialization Mode, Layer 2 supervisory frame.

RIP Routing Information Protocol, method for LANs to learn topology (TCP/IP).

RISC Reduced Instruction Set Computer.

RJ Registered Jack, connector for UNI; RJ1 1 is standard phone, RJ48 for T–1.

RJE Remote Job Entry, one form of BSC.

RL Ring Latency, time for empty token to traverse full ring with no load (FDDI).

RMN Remote Multiplexing Node.

RO Receive Only.

ROSE Remote Operation Service Element (OSI).

RNR Receiver Not Ready, S–format LLC frame acknowledges received data units but stops sender temporarily (Layer 2).

RR Receive Ready, S–format LLC frame acknowledges received data units and shows ability to receive more (Layer 2).

RSET Reset, Layer 2 supervisory frame to zero counters.

RSL Request and Status Link, same as PHI or SCAI.

RSP Response (OSI).

RTS Request To Send; lead on terminal interface.

RVI Reverse Interrupt, positive ACK that lets station take control of a BSC line.

RZ Return to Zero; signal pauses at zero voltage between each pulse, when making zero crossings.

S

S Status, signaling bit in CMI.

S ISDN interface point between TA and NT–2.

S Supervisory frame, commands at LLC level: RR, RNR, REJ, SREJ (Layer 2).

SA Source Address, field in frame header (802).

SA Synchronous Allocation, time allocated to FDDI station for sending sync frames (802.6).

SAA Systems Application Architecture, compatibility scheme for communications among IBM computers.

SABM Sel Asynchronous Balanced Mode, connection request between HDLC controllers or LLC entities (Layer 2).

SABME SABM Extended, uses optional 16–bit control fields.

SAFER Split Access Flexible Egress Routing, service at one site from two toll offices over separate T–1 loops (AT&T).

SAP Service Access Point, logical address of a session within a physical station, part of a header address at an interface between sublayers (802).

SAPI SAP Identifier, address between layers in protocol stack; e.g., subfield in first octet of LAP–D address.

SAR Segmentation And Reassembly, protocol layer that divides packets into cells.

SAR–PDU SAR Protocol Data Unit, segment of CS–PDU with additional header and possibly a trailer (e.g., a cell in ATM).

SARM Sel Asynchronous Response Mode, unnumbered frame connection request (Layer 2).

SARME SARM Extended, uses optional 16–bit control field.

SAS Single–Attached Station, FDDI node linked to network by 2 optical fibers (vs. DAS).

SB Signal Battery, second lead to balance M lead in E&M Circuit.

SCAI Switch–to–Computer Applications Interface, link between host CPU and voice switch to integrate applications; also PHI and RSL.

SCP Service Control Point, CPU linked to SS7 that supports carrier services (800, ANI).

SD Staging Delimiter, unique symbol to mark start of LAN frame (JK in FDDI, HDLC flag, etc.).

S/D Signal-to-Distortion ratio.

SDDN Software Defined Data network, virtual private network built on public data net.

SDH Synchronous Digital Hierarchy, digital multiplexing plan where all levels are synched to same master clock.

SDLC Synchronous Data Link Control; a half–duplex IBM protocol based on HDLC.

SDM Subrate Digital Multiplexing, a DDS service to put multiple low–speed channels in a DS–0.

SDN Software Defined Network.

SDS Switched Digital Service, generic term for carrier function.

SDU Service Data Unit, information packet or segment passed vertically between adjacent layers in a protocol stack.

SFND Clear to Send, signaling bit in CMI.

SES Severely Errored Second, interval when BER exceeds 10^{-3}, >319 CRC errors in ESF, frame slip, or alarm is present.

SF Single Frequency; form of on/off–hook signaling within telcos.

SF Super frame, 12 T-1 frames.

SFET Synchronous Frequency Encoding Technique, a way to send precise isoc clocking rate as a delta from system clock.

Networking acronyms

SG Signal Ground, second lead to balance E lead in E&M signal circuit.

SHR Self–Healing Ring, topology can survive one failure in line or node (802.6, etc.).

SI Sequenced Information, LAP–D frame type.

SI Secondary In, FO port that receives light from secondary fiber ring (FDDI).

SIM Set Initialization Mode, Layer 2 supervisory frame.

SIR Sustained Information Rate, average throughput; basis for SMDS access class.

SIT Special Information Tone, audible signal (often three rising notes) preceding an announcement by the network to a caller.

SIP SMDS Interface Protocol.

SIVR Speaker Independent Voice Recognition.

SLC Subscriber Loop Carrier, usually digital loop system.

SLIC Subscriber Line Interface Card (circuit), on a switch.

SMB Server Message Block, a LAN client–server protocol.

SMDR Station Message Detail Recording, keeping list of all calls from each phone, usually by PBX or computer.

SMDS Switched Multi–megabit Digital Service, offered on a MAN by a carrier; service mark of Bellcore.

SMF Single Mode Fiber, thin strand that supports only one transmission mode for low dispersion of optical waves.

SMT Station ManagemenT, NMS for FDDI.

SMTP Simple Mail Transfer Protocol (TCP/IP).

S/MUX Workstation software to allow UNIX daemons to talk to SNMP manager station.

SNA SDH Network Aspects, evolving standards for VC payloads and network management (SDH).

SNA Systems Network Architecture, IBM's data communication scheme.

SNADS SNA Distribution Services, communication architecture for electronic mail and other applications.

SNAP Sub–Network Access Protocol (802.1).

SNI Subscriber–Network Interface, the demark point.

SNMP Simple Network Management protocol, started in TCP/IP, but extending to many LAN devices (Layer 4–5).

SNR Signal-to-Noise Ratio, in dB.

SNRM Set Normal Response Mode, unnumbered command frame (Layer 2).

SNRME SNRM Extended, uses optional 16–bit control field.

SO Secondary Out, FO port that sends light into the secondary fiber ring (FDDI).

SO Serving Office, central office where IXC has POP.

SOH Section OverHead, bytes in SDH for channels carried through repeaters between line terminations like DCC or switch.

SOH Start of Header, control byte in BSC.

SONET Synchronous Optical Network.

SPAC Standards Promotion and Applications Group, has same function as COS.

SPCS Stored Program Controlled switch, CO switch (analog or digital) controlled by a computer.

SPDU Session (Layer) PDU (OSI).

SPF Synchronous Payload Envelope, data area in SONET/STS/SDH format, with POH.

SPF Shortest Path First, LAN router protocol that minimizes some measure (delay) and not just "hops" between nodes.

SREJ Selective REJ, Layer 2 frame that requests retransmission of one specific I frame.

SRL Singing Return Loss.

SRT Source Routing Transparent, variation of source routing combined with spanning tree algorithm for bridging (802).

SS7 Signaling System 7, to replace CCIS in ISDN.

SSA Systems Applications Architecture, SNA plan to allow programs on different computers to communicate.

SSAP Source Service Access Point, field in LLC frame header to identify the sending session within a physical station (802).

SSCP System Services Control Point, host software that controls SNA network.

SSM Single Segment Message, frame short enough to be carried in one cell.

ST Stream, network layer protocol for very high speed connections.

STDM Statistical Time Division Multiplexer.

STE Section Terminating Equipment, SONET repealer.

STM Synchronous Transfer Mode, one of several possible formats for SONET and BISDN.

STM–1 Synchronous Transport Module–1, smallest SDH bandwidth; = 155.52 Mbit/s, STM–n = n x 155.52 Mbit/s.

STP Shielded Twisted Pair, telephone cable with additional shielding for high speed data and LANs.

STP Signal Transfer Point, packet switch for SS7.

STS–1 Synchronous Transport Signal, level I; electrical equivalent of OC– 1, 51.84 Mbit/s.

STS–N Signal in STS format at N x 51.84 Mbit/s.

STSX–n Interface for cross–connect of STS–n signal that defines STS–n.

STX Start of Text, control byte in BSC.

SV Subvector, part of NMVT (SNA).

SVC Switched Virtual Circuit, temporary logical connection in a packet/frame network.

SWIFT Switched Fractional T–1, telco service defined by Bellcore, includes full T–1.

SW56 Switched 56 kilobit/s, digital dial up service.

SYN Synchronization character, 16h ASCII.

sync Synchronous.

SYNTRAN Synchronous Transmission, byte aligned format for an electrical DS–3 interface.

T

T Interface between NT–1 and NT–2 (ISDN).

Networking acronyms

T Non–data character in 4B/5B coding, ending delimiter (802.6).

T Tip, one of the conductors in a standard twisted pair, 2–wire local loop (the wire connected to the 'tip' of a phone plug) or one of the DTE–to–DCE pair or a 4–wire interface.

T–1 Transmission at DS–1, 1.544 Mbit/s.

T1 Tip or T lead of the DCE–to–DTE pair in a 4–wire interface.

T1DM T–1 Data Multiplexer, brings DS–OBs together on a DS–1 (Tel).

T1D1 TSC of T1 for BRI U interface.

T1E1 TSC or T1 for SNI.

T1M1 TSC or T1 for NMS and OSS.

T1Q1 TSC of T1 for ADPCM, voice compression, etc.

T1S1 TSC of T1 for ISDN bearer services.

T1X1 TSC of T1 for SONET and SS7.

TA Terminal Adapter, matches ISDN formats to existing interfaces like V.35, RS–232.

TABS Telemetry Asynchronous Block Serial, M/S packet protocol used to control network elements and get ESF stats.

TAPS Test and Acceptance Procedures, telco document for equipment instalation and set up.

TASI Time Assigned Speech Interpolation; analog voice compression comparable to DSI and statistical multiplexing of data.

TAT Trans–Atlantic Telephone, applied to cables, as TAT–8.

TBD To Be Determined, appears often in unfinished technical standards.

TC Terminating Channel; local loop.

TC Transport Connection.

TC Transmission Control, Level 4 in SNA.

TC Trunk Conditioning, insertion of various signaling bits in A and B positions of DS–0 during carrier failure alarm condition.

TCA TeleCommunications Association.

TCA Threshold Crossing Alert, alarm that a monitored statistic has exceeded preset value.

TCP/IP Transmission Control Protocol (connection oriented with error correction) of ten runs on Internet Protocol (a connectionless datagram service).

TD Transmit Data.

TDD Telecom Device for the Deaf, Teletype machine or terminal with modem for dial–up access.

TDM Time Division Multiplexing (or multiplexer).

TDMA Time Division Multiple Access, stations take turns sending in bursts, via satellite or LAN.

TDS Terrestrial Digital Service, MCI's T–1 and DS–3 service.

TE Terminal Equipment, supports native ISDN or B–ISDN formats without a TA.

TEI Terminal Endpoint Identifier, subfield in second octet of LAP–D address field.

TEST Test command, LLC UI frame to create loopback (Layer 2).

TH Transmission Header, 2 bytes in framing format for layer 4 protocol (SNA).

TLI Transport Level Interface, for UNIX.

TL1 Transaction Language 1, to control network elements (TR482); CCITT's form of MML.

TLP Transmission Level Point related to gain (or loss) in voice channel; measured power – TLP at that point = power at 0 TLP site.

TMN Telecommunications Management Network, a support network to run a SONET network.

TMS Timing Monitoring System.

TO Transmit Only; audio plug for a channel bank without signaling.

TOP Technical and Office Protocol; for LAN's.

TOPS Task Oriented Procedures, telco document for equipment operation and maintenance.

TOS Type Of Service, connection attribute used to select route in LAN (SPF).

TP Transaction Processing, work of a terminal on–line with a host computer.

TPEX Twisted Pair Ethernet Transceiver.

TP–N Transport Protocol of Class N (N = 0 to 4), OSI layer 4.

TP–0 Connectionless TP (ISO 8602).

TP–4 Connection oriented TP (ISO 8073).

TPDU Transport Protocol Data Unit (OSI).

TPF Transaction Processing Facility, IBM host software for OLTP.

TPSE Transport Processing Service Element (OSI).

TR Technical Reference, a final Bellcore standard.

TR Token Ring, a form of LAN.

TS Transport Service (OSI).

TSDU Transport Service Data Unit (OSI).

TSI Time Slot Interchange; method of temporarily storing data bytes so they can be sent in a different order than received; a way to switch voice or data.

TTC Telecommunications Technology Committee, Japanese standards body.

TTR Timed Token Rotation, type of token passing protocol (FDDI).

TTRT Target Token–Rotation Time, expected or allowed period for token to circulate once around ring (802.4, 802.6).

TTY Teletypewriter.

TU Tributary Unit, virtual container plus path overhead (SDH).

TUG TU Group, one or more TUs multiplexed into a larger VC (SDH).

TWX TeletypeWriter Exchange, switched service (originally Western Union) separate from Telex.

Networking acronyms

U

u English transliteration of Greek mu ( ), for micro or millionth; prefix in appreviation of units like us, um.

U Interface between CO and CP for ISDN.

U Unnumbered format, command frames, same as UI (Layer 2).

UA Unnumbered Acknowledgement, LLC frame to accept connection request (Layer 2).

UART Universal Async Receiver Transmitter, interface chip for serial async port.

UAS Unavailable Second, when BER of line has exceeded 10^{-3} for 10 consecutive seconds until next AVS start.

UDLC Universal Data Link Control, Sperry Univac's HDLC.

UDP/IP Universal Data Protocol or User Datagram Protocol, Internal protocol.

uF Microfarad, one millionth of the unit of capacitance.

UI Unnumbered Information, frame at LLC level whose control field begins with 11: XID, TEST, SABME, UA, DM, DISC, FRMR (802).

ULP Upper Layer Protocol.

UNI User–Network Interface, demark point or SDH and B–ISDN at customer premises.

UNR Uncontrolled Not Ready, signaling bit in CMI.

UP Unnumbered Poll, command frame (Layer 2).

U–Plane User Plane, bearer circuit for customer information, controlled by C–Plane.

UPS Uninterruptable Power Supply.

us Microsecond; 10^{-6} second.

USART Universal Sync/Async Receiver Transmitter, interface chip for sync and async data I/O.

USAT Ultra–Small Aperture SATellite; uses ground station antenna less than 1m diameter.

USOC Universal Service Order Code.

V

VAN Value Added Network; generally a packet switched network with access to data bases, protocol conversion, CIC.

VBR Variable Bit Rate, packetized bandwidth on demand, not dedicated (ATM).

VC Virtual Container, a cell of bytes carrying a slower channel to define a path in SDH; VC–n corresponds to DS–n, n = 1 to 4.

VC Virtual Circuit, logical connection in packet network so net can transfer data between two ports.

VCC Virtual Channel Connection (SMDS).

VCI Virtual Circuit (or Channel) Identifier, part of a packet/frame address header (X02.6, ATM).

VCX Virtual Channel Cross–connect, device to switch ATM cells on logical connections.

VDT Video Display Terminal, often applied to any type of "tube" or PC.

VF Voice Frequency, 300–3300 Hz.

VG Voice Grade; related to the common analog phone line.

VGPL Voice Grade Private Line, an analog line.

VHF Very High Frequency, radio band from 30 to 300 MHz.

VMTP Versatile Message Transport Protocol, designed at Stanford to replace TCP and TP4 in high–speed networks.

VNL Via Net Loss, related to TLP.

VPI Virtual Path Identifier, VCI in ETSI version or ATM.

VQC Vector Quantizing Code; a voice compression technique that runs at 32 and 16 kbit/s.

VQL Variable Quantizing Level; voice encoding method.

VR Receive state Variable, value in register at receiver indicating next NS expected (Layer 2).

VS Send state Variable, value in register or sender of Ns in last frame sent (Layer 2).

VSAT Very Small Aperture Terminal, satellite dish under 1m.

VT Virtual Tributary, logical channel made up of a sequence of cells within SONET or similar facility.

VTAM Virtual Telecommunications Access Method, SNA protocol and host program.

VTE Virtual Tributary Envelope, the real payload plus path overhead within a VT (SONET).

VTNS Virtual Telecommunications Network Service.

V35 Former CCITT recommendation for a modem with a 48 kbit/s interface, being replaced by TIA–530A.

W

WACK Wait before transmit positive Acknowledgment, control sequence or DLE plus second character (30 ASCII, 6B EBCDIC).

WAN Wide Area Network, the T–1, T–3, or broadband backbone that covers a large geographical area.

WATS Wide Area Telephone Service.

WBC WideBand Channel, one or 16 FDDI subframes of 6.144 Mbit/s assignable to packet or circuit connections.

W–DCS Wideband Digital Cross–connect System, 3/1 DACS for OC–1, STS–1, DS–3, and below, including T–1 (see B–DCS).

WDM Wavelength Division Multiplexing, 2 or more colors of light on 1 fiber.

X

X X class central office switch is in HPR net but not linked to NP.

X.25 CCITT recommendation defining Level 3 protocol to access a packet switched network.

XID Exchange Identification, type of UI command to set up exchange parameters between LLC entities (Layer 2).

XNS Xerox Network Services, a LAN protocol slack.

Networking acronyms

X–off Transmit Off, ASCII character from receiver to stop sender.

X–on Transmit On, ok to resume sending.

XTP eXpress Transfer Protocol, a simplified low–processing protocol proposed for broadband network.

Y

Y Yellow alarm control bit in sync byte (TS 24) of T1DM, Y=O indicates alarm.

Z

Z Impedance, nominal 600 ohm analog interface may be closer to complex value of 900 R + 2 uF C.

ZBTSI Zero Byte Time Slot Interchange, process to maintain 1's density.

Understand datacom protocols by examining their structures

Authors: Alex Goldberger and Stephen Y. Lau

Although you'll probably never design a datacom protocol, you'll often need to interface to a particular protocol environment. And you can better select among the many silicon implementations becoming available if you know protocol basics.

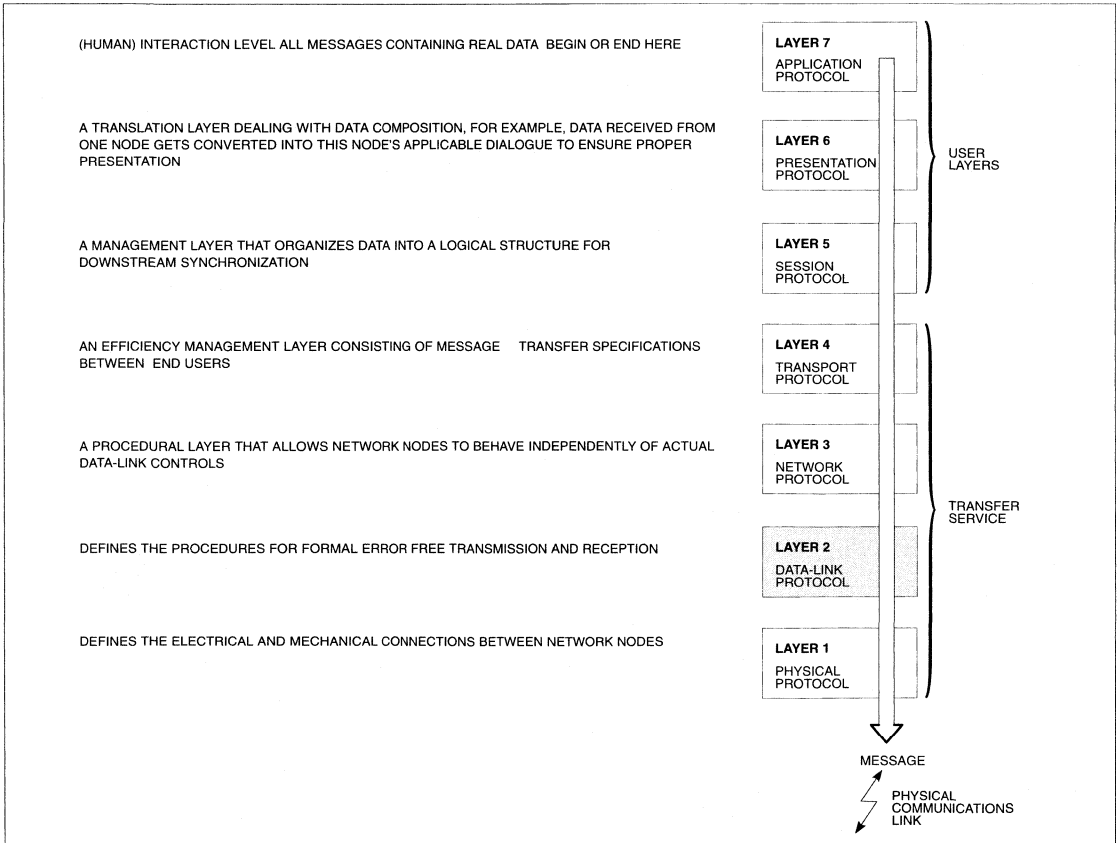
INTRODUCTION

As technical and market factors make your product's data communications capability more important, meeting the requirements of the datacom protocol dictated by the application environment becomes vital. Unfortunately, the wide variety of protocols and their subtle differences complicate the design task. But by understanding the tradeoffs involved in working with various protocols, you can design a product for many years of service in a variety of network environments. And the key to that flexibility lies in implementing a protocol that's now in wide use and likely to remain widely used, or at least compatible with future protocols. Further, becoming familiar with these protocols is the first step in intelligently selecting among the many IC-level implementations becoming available.

What is a protocol?

In the most general terms, a protocol is a formal set of conventions governing the format and relative timing of message exchange between two communications terminals. When dealing with protocols, though, most datacom engineers tend to think in terms of the 7-layer Open System Interconnection (OSI) reference model developed by the International Standards Organization (Figure 1). This widely (if academically) accepted architecture provides a framework in which you can define every aspect of data communications.

The model's first protocol, Layer 1, underwrites electrical and mechanical conventions such as connector format and signal/pin assignments. Familiar standards such as EIA's RS-232C, RS-442 and RS-449 as well as CCITT's V.24 and X.21 are Level 1 protocols. Layer 2 — the area in which datacom engineers get most involved and the focus of this article — defines procedures for error-free transmission and reception.



The International Standards Organization's OSI reference model breaks the various data-communications tasks into seven protocols. Layers 1 and 2 predate the model and are fairly mature in terms of standards and protocol implementation; at Layer 3 and above, many OSI-like implementations exist in proprietary system offerings, and standardization efforts are underway. Layer 2 protocols, the focus of this article precisely define the format of message transmissions and provide error-detection/recovery mechanisms.

Figure 1. Theoretically Describing Any Datacom Link

Understand datacom protocols by examining their structures

Layers 3 and 4 add standards for message transport, and the three highest layers define the procedures for human interaction with overall network services.

DLCs define transmission methods and detect and correct errors

Layers 1 through 4 are designated the transfer service because they move
messages from one point to another; layers 5 through 7 are known as the user layers because they provide user access to messages on the network.

From a design standpoint, the vast majority of work in both hardware and software implementations focuses on Layers 1 and 2. Above the link layer (Layer 2), implementations abound in the form of proprietary offerings from competing firms; the electronics industry is seeking a consensus on exactly what the corresponding standards and protocols should be.

Specifics of link-layer protocols

Although still undergoing development, Layer 2 protocols, also known as link-layer
protocols or data-link controls (DLCs) are relatively well defined by function and type. In terms of function, several aspects define a DLC. First, a DLC is a formal ritual for communications; it is the precise definition of message transmission and acknowledgement between computers and their peripherals for every message transfer. Although not the communicated data itself, every link-layer protocol facilitates communications by embodying a structure for transport of information from one point to another.

In addition, a clearly defined method for data transfer among computers and peripherals must accommodate coding and transmission errors even under the best circumstances. Besides the error sources that a busy

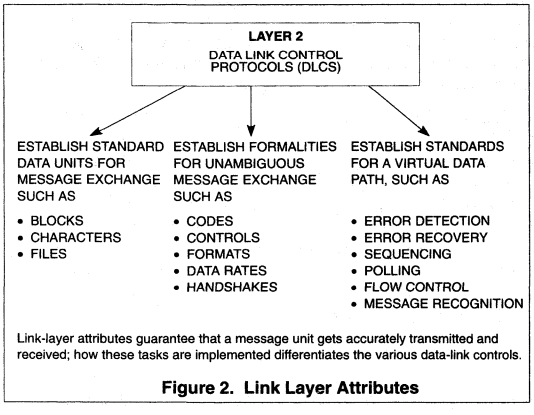


Figure 2. Link Layer Attributes

datacom link might suffer because of a low signal-to-noise ratio, receiving stations might be engaged in other tasks when a message gets sent. Thus, the second major characteristic of a DLC is the ability to detect and recover from mistakes and complete the communication process.

Figure 2 details other important link-layer-protocol attributes. All DLCs embody all or some of these features, whether implemented in hardware or software. In fact, variations of these features define the various link-layer protocols.

Thus, as a family of protocols, DLCs share many common features but also accommodate a wide variety of performance characteristics that require full understanding for correct DLC selection. For instance, it is not unusual for networks to use both synchronous and asynchronous transmission and wide variations in data rates. Datacom-equipment designers must carefully evaluate the choices to ensure correct positioning of their products in the marketplace.

To see how link-layer protocols fit into a typical datacom scheme, examine Figure 3. In this system, a terminal user wants access to an applications program that is physically located some distance away. Between the terminal and host computer that stores the desired program is a complex network of modems, transmission facilities and protocol-conversion devices. Each communications layer at the terminal end has an equivalent layer at the host-computer end. Thus, the modems "talk" only to each other, ignoring the actual meaning of the data they handle. Likewise, the data-link controls interact as peers to assure the successful transmission and reception of data without regard for the modems' modulation scheme.

This peer-to-peer communication, when combined with the structure of the OSI model, leads to the concept of enveloping. As the user data generated in Layer 7 moves down the model, the protocol associated with each layer adds control information. By the time the user data reaches the physical link layer (Layer 1), it has been successively enveloped several times. Following transmission across the data link, the enveloped data moves up the model. At each layer, the peer-level envelope of control information gets stripped off for evaluation and action by its peer protocol.

Datacom messages don't necessarily contain user data, though. Messages such as polling or acknowledgement — where a computer grants permission for a terminal to send a message, or where any receiver sends a short message ACKing or NAKing another message — can originate and terminate at Layer 2 with higher layers none the wiser.

For the system designer, an end-to-end view builds a virtual communications path through a network. Because you cannot always predict the various network environments in which a product will see use, you should concentrate your design effort on the data-link interface, thereby allowing for the use of any higher level protocols. Your goal, of course, is to control data transmission and reception by synchronizing sender and receiver and to detect errors and provide successful recovery techniques. A subordinate but no less important objective is to minimize overhead so that datacom efficiency remains high and costs remain low.

The DLCs at your disposal for this job can be classified according to several criteria, such as error-handling capability, message format, method of communication-line control and flow-control procedure. The implementation of any DLC requires knowledge of all these criteria because enough variation exists to mandate complete specification by the engineer. In other words, every data-link-control protocol is itself a procedure that offers several modes of operation depending on the aforementioned options.

Sync vs async transmission

Before selecting a DLC, you should first determine if your application requires synchronous or asynchronous operation because this aspect can limit DLC options. Furthermore, other technical issues are involved in the sync/async decision.

The prime distinction between sync and async operation lies in the time domain In async, the time interval between transmissions is variable. Control bits, which designate message start and stop, frame each character; asynchronous characters vary in length

Understand datacom protocols by examining their structures

depending on the information code (e.g., ASCII, EBC-DIC or IBM's 6-bit Transcode) and are usually 5- to 8-bits long. On the other hand, sync transmission proceeds without character-by-character framing once synchronization is achieved; there are no intervening control bits for start/stop.

Because of its inherent simplicity and historical momentum (async transmission methods were introduced years before sync methods), async transmission is now used in perhaps millions of terminals, primarily where low-speed communication (less than 1800bps) is sufficient. Async's prime disadvantage is its control overhead, which can reach three control bits for five data bits or 37%. In contrast, fully synchronous transmissions typically have less than 2% overhead and suit multiplexing. This high efficiency also allows synchronous data rates over voice-grade lines as high as 9.6kbps.

By comparing transmission data structures, you can see why async (with its inherent idle times) suits man/machine interfaces while continuously flowing sync offers the high speed needed in machine-to-machine interfaces. Thus, character-mode CRT terminals generally employ async transmissions to keep costs low. On the other hand, the trend in intelligent terminals, which pre-process data and then transmit it to a host in blocks, is toward sync transmissions.

Some equipment might provide both means. For example, a cluster controller, which interfaces a CPU to a group of terminals, can use async mode for the terminal ports while communicating with the host over a synchronous link.

By themselves, synchronous and asynchronous formats are not protocols. Rather, they are transmission methods that place performance restrictions on a communications channel to ensure data integrity. DLCs that use sync or async transmission mirror these performance restrictions and act as policemen to assure that messages are correctly transferred independently of the transmission methods employed.

Sync and async transmissions are closely related to the two main classifications of link-layer protocols: character-oriented protocols (COPs) and bit-oriented protocols (BOPs). Async mode, with its character-by-character framing, does not lend itself to BOPs, which inherently lack character framing in their information fields and thus required COP; sync transmission, in contrast, can use either a COP or BOP.

Despite this fact, BOPs and COPs are not direct competitors for datacom applications. One well-established rule of modern datacom engineering is that bit orientation is synonymous with high-speed operation. However, a great deal of installed datacom equipment requires relatively slow speeds; thus, the DLC decision in the applications environment rests with other factors contained in the definitions of BOPs and COPs.

For most applications, you will likely deal with one of the several widely used BOPs or COPs. Examining the BOPs first, note that they are all variations of the International Standards Organization's High Level Data Link Control (HDLC). The US version, sponsored by the American National Standards Institute (ANSI), is designated the Advanced Data Communications Control Procedure (ADCCP). Perhaps the most popular version of HDLC is IBM's Synchronous Data Link Control (SDLC), but a variation becoming more widely used is the Link Access Procedure B (LAPB), a host-to-node datacom protocol contained in the CCITT's X.25 multilevel protocol (which covers Layers 1, 2 and 3).

Turning to the COPs, note that the two dominant versions are IBM's Binary Synchronous Communications (BSC or Bisync) and Digital Equipment Corp's Digital Data Communications Message Protocol (DDCMP). Between these two exist hundreds of proprietary variations (such as ones for passenger-reservation systems) that emulate the IBM or DEC technique in thousands of compatible products.

To gain a better understanding of the differences among these DLC types, first examine the structures of two very popular BOPs (HDLC, and SDLC) and the two top COP contenders, Bisync and DDCMP (Figure [4]).

BOPs all have similar frame structures

HDLC-subset distinctions become visible with a field-by-field description of a typical BOP frame. Beginning with an 8-bit flag sequence, a frame is sequentially built by adding Address, Control, Information (data) and Frame Check fields and finally another flag. All fields except the Information field consist of single or multiple 8-bit patterns designated octets. The Information field can be of any length (not necessarily a multiple of characters or bytes), although some specific implementations such as SDLC require that it be an integer multiple of eight bits.

The entire transmitted frame, also called a block, gets examined by each station attached to the data link. The BOP hardware resident in each receiver continuously examines the Address field and enables that receiver immediately upon detection of its own address. The address is usually a single octet, but provisions are available for transmitting a multiple-octet address.

In all HDLC implementations, the DLC behaves differently for primary and secondary stations, or masters and slaves. In any network, only one master can exist, and slaves can transmit only when the master explicitly gives them permission to do so. When a secondary station transmits, the Address field is its own rather than the destination address. A primary station accepts this message only if it has given that secondary station permission to transmit. As one measure of flow control, the primary station periodically enables each secondary by transmitting an explicit permission message. Mandating the inclusion of the Address field in every message permits a primary station to interleave receptions from two or more secondary stations without garbled results.

Next in sequence, the control field contains one or two octets depending on which HDLC subset and mode — extended (two octets) or non-extended (one octet) — are used. Control determines (informs the receiver of) the message type, the sequencing of send and receive flames, the explicit poll command (permission to transmit) and/or the final response from secondary to primary station. A primary station uses the Control field to command specific actions by a secondary, while a secondary station encodes the Control field with appropriate response data. Together, the Address and Control fields make up a Header.

The Information field can contain virtually any number of bits, but practical considerations limit the field according to flow-control regulation in complex networks. (For instance, you might not want to repeat a 20-min block because one error shows up; you would use smaller blocks.) However, long Information fields are easily accommodated with sequential frames that collectively constitute a complete transmission. Data in the field can employ any code structure: BCD, standard binary, packed decimal or others. It is important to use a code defined by the terminal address. Note in addition that the special control characters exclusive to a particular secondary station get included in the Information field.

Understand datacom protocols by examining their structures

Finally, the Frame Check field provides a code that can serve at the receiving end to verify error-free message reception. It is generally the remainder of a CRC calculation based on a standardized polynomial.

BOPs use few control characters

BOPs do not use control characters to delineate message blocks. Only two distinct bit patterns, which need not occur on character boundaries, carry special meaning within a BOP message: Flag (01111110) and Abort (1111111). Thus, to achieve data transparency, you need only ensure that a sequence of six or more ONEs never gets transmitted unless you want to send a Flag or an Abort. (Transparency is important because every datacom message consists of bit patterns representing both data and control information that flow along one communications link; you therefore need techniques that distinguish data from control. Transparency allows characters (bit patterns) to get transmitted as data without regard for their inherent control definitions).

To ensure data transparency, BOPs use a bit-stuffing technique termed Zero Insertion and Deletion (Figure [5]a). The transmitting end examines the outgoing bit stream, and if it detects a sequence of five ONEs, it unconditionally inserts a ZERO into the bit stream (the Flag- and Abort-generation circuits bypass this step). The receiving end then deletes any ZERO that follows exactly five ONEs.

What are the major differences among the major BOPs? As seen in Figure [6], they differ primarily in the length of the Address and Control fields and method of re-transmitting rejected (erroneous) frames. When designing a data-link protocol into a piece of equipment, you will generally choose the one that your device must interface with. But if no such restrictions apply — for example, when you are interconnecting a closed system — the HDLC/ADCCP protocol provides the most flexibility because the Address-field extension allows you to address a large number of stations and the 2-octet Control-field option allows as many as 127 frames to remain unacknowledged before a response from the secondary station is required.

COPs: a more complex control structure

Turning to the structure of COP frames, note that although the exact nature and sequence of fields varies with the DLC, all COP blocks contain Header, Information (data) and Block Check fields. The detailed structure of a COP (Figure [4]) illustrates the options for each field, and the differences between the two most widely used COPs — Bisync and DDCMP — are discernible.

The first major field, the Header, although here an independent field, performs the same basic role as in BOPs — it can incorporate the address of either the message source or destination, a job number, message type (control or data) and required control action, as well as positive or negative acknowledgement related to error-free reception of a prior message. The control sub-field can serve to initialize a receiver, ask why an acknowledgement has not yet occurred, abort a message transfer or acknowledge correct or incorrect reception of prior blocks. Encoding of the control messages is accomplished with predetermined characters.

Next, a typical Information field can contain characters of an information code set in BCD, binary, floating point or other pure data codes. Because of its great flexibility, the field can also contain a special code or even a machine-language computer program.

Completing a message unit, the Block Check field provides a code that, when used at the receiving end, can verify error-free reception of a message. This field can be based on a parity check or, as is the case in all major DLCs, the remainder of a CRC calculation. Some DLCs provide a Block Check field at the end of both the Header and Information fields.

As previously noted, COPs have a common characteristic in that they all use a fully defined set of control characters (Figure [4]b). Remember that BOPs use only two control-character sequences; thus, the use of this character set makes code transparency in COPs a complex task because of a relatively long list of bit sequences that cannot appear in the Information field.

In their approach to handling data transparency, COPs fall into two sub-classes: The Character Controlled class (such as Bisync) uses special 2-character sequences to enter and exit the Transparent mode (Figure [5]b); the Character Count class (such as DDCMP) uses a standardized Header format that explicitly provides a character count for the Information field. This latter approach allows a receiver to determine the end of a message without including control characters in the Information field, thus automatically making this field transparent.

Some significant differences between BOPs and COPs should now be apparent (Figures 4, 5 and 6). Both types of DLC provide for data transparency, but the overhead for BOPs is lower than for COPs, resulting in higher data rates for BOPs. Furthermore, BOP message frames share many common characteristics regardless of the specific DLC used, including a standard frame format, code independence due to bit stuffing, positional significance rather than control characters or character counts, and either half- or full-duplex operation (only some COPs work in full-duplex mode). In addition, BOPs offer a wider range of modes and user programmability as well as the widest acceptance among vendors and standards organizations. Thus, despite the fact that COPs have been in use for more than 20 years and currently control more network nodes than any other type of link-layer protocol, you can safely assume that more datacom-engineering time will be devoted to designing-in HDLC-like BOPs during the next decade than to any other DLC.

The second major DLC function

Recall from the initial definition of a DLC that a key function is error detection and correction. This task varies in importance depending on the DLC application. It ranges from completely ignoring errors in applications such as hulk-text transfers of lengthy word-processing files to absolute zero-defect assurance in applications such as transferring financial records or stock quotes.

Statistical error rates for various applications give insight into the error-control/recovery task that you must consider in DLC selection. In transfers between a computer and disk at rates to 10^9 bps, the error rate typically equals one in 10^3 bits. In a typical datacom setting using a dial-up public telephone network, though, the data rate is a comparatively modest 10^3 to 10^4 bps while the error rate escalates to one in 10^5 bits. These two applications are thus more than 10 orders of magnitude apart in expected errors.

DLC error-control methods include Hamming codes, vertical (parity) and longitudinal redundancy checks (VRCs and LRCs) and cyclic redundancy checks (CRCs). Link-layer protocol structures always provide Error Control fields, and detected errors result in a request for re-transmission across the data link.

In general, DLCs offer two types of re-transmission requests (ARQs): Stop/Wait and Continuous. In the Stop/Wait procedure, the transmitting station literally stops sending after the transmission of a block or frame. It then waits until the receiving station performs the predetermined error check, sending an ACK to confirm correct reception. If the receiver finds the message erroneous, it sends a

Understand datacom protocols by examining their structures

NAK and the previous block gets re-transmitted. The overhead in terms of line idle time and turnaround for this type of ARQ is obviously very high, and DLCs that use it don't fully exploit line capacity. The Stop/Wait procedure is most often found in simplex and half-duplex communication links.

In continuous ARQ, blocks move continuously and the transmitter provides buffer storage while both the transmitter and receiver monitor block counts. When it detects an erroneous block, the receiver transmits a NAK control message that contains the defective block's number. Two implementations of this type of ARQ are widely used: Go-Back-N and selective repeat (Figure [7]). The former results in the re-transmission of both the defective block and all subsequent in-transit blocks; the latter improves link efficiency by re-transmitting only the defective blocks. Both implementations require a full-duplex link and typically can improve line utilization by a factor of two because line turnaround and idle time are virtually eliminated.

LANs vs datacom links

Although datacom links have seen wide use for many years, the great attention now given to local-area networks (LANs) raises the question of what differentiates the two.

To understand the distinctions, look first at the general description of a LAN: a datacom system that allows several independent devices to intercommunicate and that confines communication to a moderate-sized area such as an office building, a warehouse or a campus. It accomplishes communication over a physical channel with a moderate to high data rate (1M to 10M bps) and a consistently low error rate (because of LANs' well-defined cable links, you can better predict and control such speed-degrading factors as cable and unit delays). Finally, LANs allow any network user or device to have direct access to any other point.

A standard datacom link, on the other hand, generally uses a long-distance network consisting of interconnect facilities in different parts of a country or the world often a part of the public switched telephone network. A more important distinction, though, is that standard datacom links implicitly rely on a master that controls bus activity. Although the polling method used in standard datacom networks to allocate link usage functions adequately, it does have several disadvantages:

1. It is difficult to adapt the system to changing conditions. For instance, if some unit's activity peaks at certain times, you must write an elaborate software algorithm so that the master can account for this fact. Further, if system characteristics change over time, you must continually update this algorithm.

2. Modularity is difficult to implement. Because a central unit controls all system activity, adding or deleting modules from the bus dictates a change in the control software. This requirement holds even if you add or delete units that talk only to each other and not to the primary.

3. Total system reliability depends on the primary station's reliability; if that unit goes down for any reason, the entire system stops functioning.

4. Protocol overhead for data collection or control applications can be high. Because standard serial buses do not have interrupt capability, the primary must continually poll the data-gathering and status-monitoring units. Often, however, the polling action indicates no change in status and returns little meaningful data. Thus, protocol overhead is high compared with the volume of data gathered.

As noted earlier, most LANs do not employ the central-controller concept; each network unit can take control of the system bus when needed and transmit data directly to appropriate units. Because several units can vie for bus control simultaneously, two prevalent methods of resolving such conflicts have arisen: carrier sense multiple access with collision detection (CSMA CD) and token passing.

This networking concept leads to the following advantages over classical datacom structures:

1. The bus can self adapt to changing conditions because modules request the bus only when they need it. If necessary, some modules can be assigned higher priority than others.

2. Modularity is easy to implement. You can add units to the bus without disturbing existing units provided that the total at any time does not exceed the bus's effective bandwidth.

3. System reliability is high because system communications capability does not depend on any particular unit being connected.

4. Control and monitoring systems are efficiently implemented (when bus bandwidth is close to the data bandwidth) because any unit can directly address any other, effectively allowing interrupt capability.

Because LANs achieve high transmission speeds and typically interconnect intelligent equipment, they universally use synchronous transmission mode, generally implemented with BOPs. The LAN unit of information transfer, usually designated a packet, is structurally similar to an HDLC frame. It consists of a source address, destination address, control code, information and a frame-check sequence. The two addresses identify the transmitter and receiver, the control code tells the receiver what kind of data is being sent and the frame-check sequence allows detection of transmission errors. Unlike conventional BOP frames, however, LAN frames do not need bit stuffing to achieve data transparency. Rather, the start- and end-of-packet delimiters get implemented with special code-violation patterns in the modulation scheme (typically Manchester) that encodes the clock and data on one signal, instead of using a special character such as a flag.

Thus, although classical datacom networks could be designated LANs if they meet the general definition previously presented, there is nonetheless a clear distinction between them — although the functional differences between the most advanced datacom links and the least advanced LANs are small.

PREAMBLE	START FRAME DELIMITER	ADDRESS (DESTINATION)	ADDRESS (SOURCE)	MESSAGE LENGTH	MEDIA-ACCESS CONTROL DATA	PAD	FRAME CHECK	**CSMA** (TYPICAL)

START FRAME DELIMITER (2 OCTETS)	ACCESS CONTROL (1 OCTET)	ADDRESS (DESTINATION) (2/6 OCTETS)	ADDRESS (SOURCE) (2/6/ OCTETS)	INFORMATION (≤ 4099 OCTETS)	FRAME CHECK (4 OCTETS)	END FRAME DELIMITER (2 OCTETS)	**TOKEN RING**

PREAMBLE/ IDLE (1 OR MORE OCTETS)	START-FRAME DELIMITER (1 OCTET)	ACCESS CONTROL (1 OCTET)	ADDRESS (DESTINATION) (2/6 OCTETS)	ADDRESS (SOURCE) (2/6/ OCTETS)	INFORMATION (≤ 4099 OCTETS)	FRAME CHECK (4 OCTETS)	END FRAME DELIMITER (1 OCTET)	**TOKEN BUS**

Framing diagrams for popular LAN types show that these message packets require both source and destination addresses, in contrast to DLC protocol's single-master multiple-slave architectures, which require polling at the expense of speed.

A designer's review of data communications

Author: Alex Goldberger *Reprinted by permission of Computer Design, from May 1981 issue*

Efficient communication systems depend on knowledge of design concepts and principles for encoding and transmitting digital data

Recent developments in information systems and computer and microcomputer hardware have highlighted the need for efficient data communications. Industrialists, educators, financial institutions, and government organizations are finding computer services essential to their operation, and the data communications link is an integral part of these services.

Data communication refers to the electronic transmission of encoded information or data from one point to another. As used here, the term encompasses all the physical elements, systems, devices, and procedures that are required for the transmission and reception of data between two or more points. Elements of a data communication system are communication channels, transmission modes, line conditioning, modems, serial communication interfaces, data link configurations, information codes, and protocols.

The data communication process generally requires at least five elements: a transmitter or source of information, a message, a binary serial interface, a communication channel or link, and a receiver of transmitted information (Figure 1) . A data communications interface is often needed to make the binary serial data compatible with the communication channel.

Communication Channels and Facilities

A communications link or channel is a path for electrical transmission between two or more stations or terminals. It may be a single wire, a group of wires, a co-axial cable, or a special part of the radio frequency spectrum. The purpose of a channel is to carry information from one location to another. All channels have limitations on their information handling abilities, depending upon their electrical and physical characteristics.

There are three basic types of channels: simplex, half-duplex, and full-duplex. As an example of each, consider transmission between points A and B in Figure 1.

Transmission from A to B only (and not from B to A) requires a simplex channel. Simplex channels are used in loop mode configurations such as supermarket checkout terminals. Transmission from A to B and then from B to A, but not simultaneously, requires a half-duplex channel. If a 2-wire circuit is used, the line must be turned around to reverse the direction of transmission. A 4-wire circuit eliminates line turnaround. Transmission from A to B and from B to A simultaneously describes a full-duplex channel. Although four wires are most often used, a 2-wire circuit can support full-duplex communications if the frequency spectrum is subdivided into receive and transmit channels.

In addition to the direction of transmission, a channel is characterized by its bandwidth. In general, the greater the bandwidth of the assigned channel, the higher the possible transmission speed. This speed is usually measured in terms of the number of line signal elements per second, the baud rate. If a signal element represents one of two binary states, the baud rate is equal to the bit rate. When more than two states are represented, as in multilevel modulation, the bit rate exceeds the baud rate. The range of channels includes private wire, wideband, Digital Data Service, limited distance, voice grade, subvoice grade, and telegraph (Table 1).

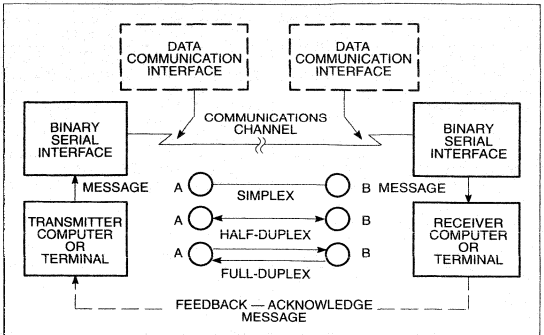


Figure 1. Elements of Data Communications Process. Five major elements are source, message, interface channel, and receiver. Channel can be any of three basic types.

Digital vs Analog Transmission

Digital transmission can be applied to digital data or analog voice signals. In either case, information is sent over the communications channel as a stream of pulses. Pulses transmitted over a communication line are distorted by line capacitance, inductance, and leakage.

The longer the line or the faster the pulse rate, the more difficult it is to interpret the received signal. This signal degradation is the reason for the closely spaced regenerative repeaters used in digital data transmission facilities. When noise and distortion threaten to destroy the integrity of the pulse stream, the pulses are detected and regenerated. If the regeneration process is repeated properly, the received signal will be an exact replica of the transmitted signal. It is possible to transmit pulses over short distances using privately owned cable or common carrier wire pairs. This is baseband transmission and usually requires line drivers and receivers on each end of the line. Longer distance communication must use the digital transmission facilities of the common carriers.

In analog transmission, a continuous range of signal amplitudes or frequencies is sent over the communications line. Linear amplifiers maintain signal quality. The voice telephone network supplied by the common carriers uses analog transmission facilities to service most data communications users. To interface the analog voice channels to digital terminals and computers, a modulator-demodulator (modem) is used. In a modem, digital information modulates a carrier signal, which passes through the telephone network just as does a voice signal. At the receiving end, the signal is demodulated back into digital form.

Voice Grade Lines

Voice grade telephone lines are available through the public switched network (Direct Distance Dialed or DDD); as private leased lines without conditioning; and as private, conditioned, leased lines. Although the bandwidth is the same for all three, the effective data rates vary because of different specifications for signal noise, amplitude attenuation, and envelope delay distortion.

Dial-up lines are the 2-wire pairs supplied by the common carriers on the public switched telephone network. Most often these lines are used for half-duplex operation, although frequency band splitting modems can facilitate full-duplex at 1200 bits/s. A major advantage of dial-up lines is that any point on a worldwide telephone network can be reached. Furthermore, communication costs are limited to the time the lines are actually in use.

A designer's review of data communications

Table 1. Communication Channel Characteristics

Channel Type	Channel Interface	Data Rates (bits/s)	Applications
Fiber optics	Fiber optic connector	Up to 2G	Computer-computer, WAN, Computer-high speed peripheral
Private wire or cable	Line drivers and receivers Modem eliminators Limited distance modems	1M to 155M	In-plant data communications Local Area Network
Wideband analog	Wideband Bell 300-series modems, CCITT V-series wideband modems	19.2k to 230.4k	Telephone channel multiplexing
Dataphone Digital Service	Data Service Unit Digital Station Terminal	2.4k, 4.8k, 9.6k, 56k, 1.544M	Private terminal-computer geographically dispersed links
Switched telephone network (DDD)	2-wire modems Acoustic couplers	0 to 2k (async), 2k to 4.8k (sync) 300, 450, 600, 1.2k (async)	Terminals, data collection stations, other interactive communications
Leased voice grade lines (with or without conditioning)	2/4 wire modems	0 to 2.4k (async) 2k to 9.6k (sync)	Remote batch, private communications networks
Subvoice grade	Narrowband modems	150 to 200	Teletypes, A-D converters, telemetry
Telegraph	DC signaling	45 to 75	TWX, TELEX

Four major problems are associated with the switched telephone network. First, the lines may be noisy. The human brain can interpret what is being said despite the interference that plagues many calls, but computers and terminals can easily lose or misinterpret data because of noise. Second, delay distortion is caused by the various frequency components of a signal being transmitted at a nonuniform speed through the transmission medium. This may result in received data that are erroneous. Third, the switched network requires relatively long connect, disconnect, and turnaround times, which limit the system data throughput. Fourth, the reliability of telephone switching equipment is relatively low.

Although more costly than dial-up lines, private leased lines largely circumvent the problems that afflict the switched network. Their basic advantages are ready availability and freedom from busy signals, fixed monthly charges, and conditioning for better data quality, as well as higher transmission rates and throughput. Leased lines are generally 4-wire circuits usable for half- or full-duplex operation. Simultaneous transmission and reception is possible, and line turn-around is eliminated. The basic disadvantages of leased lines are higher cost and the line's connection to only one location. However, if telecommunication demands entail high volume, high quality, high speed traffic between two points, a leased line is the best choice.

Digital Data Services

The Bell System developed a digital transmission network that provides higher data rates with fewer errors at a lower cost than conventional analog transmission facilities. Known as Dataphone Digital Service (DDS), the network is available in 32 U.S. cities and recently has been granted Federal Communications Commission (FCC) approval for 64 other cities. Two point, full-duplex, private line service is provided at synchronous data rates of up to l.544M bits/s. In June 1977, the FCC approved construction of American Telephone & Telegraph (AT&T)'s Dataphone Switched Digital Service (DSDS).

Specialized common carriers offer a variety of services in addition to those of the Bell System. These include shared private line services such as EXECUNET by MCI Communications and SPRINT by Southern Pacific; satellite services by the Radio Corporation of America, Western Union, and others; packet-switching carriers including Telenet by General Telephone and Electronics and Tymnet by Tymshare; and facsimile and electronic mail services such as Graphnet, TWX, TELENET, and SPEEDFAX.

Modems

Modems are devices that convert digital data from a computer or terminal to a modulated carrier waveform required by the communication channel. One modem is needed at each end of the channel, as shown in Figure 2. Modems are also known as data sets and are designed for specific kinds of service and for specific bandwidths or data rates. Those discussed here accept a binary serial input from the transmitter and provide a binary serial output to the receiver. Parallel input modems (used mostly for paper tape transmission) and analog input machines (used primarily for facsimile transmission) are not considered. The three types that are considered are short haul, wideband, and voice grade (Table 2).

Voice grade telephone lines with a bandwidth of 2700 Hz (300 to 3000 Hz) are by far the most common medium used for data communications. A voice grade modem, designed for use on these lines, should be selected on the basis of the type of service (dial-up or leased), the required data rate, and an acceptable level of error performance. The two broad categories of voice grade modems are asynchronous units and synchronous units. Asynchronous units operate at a maximum data rate of 1800 bits/s over dial-up facilities and 2000 bits/s on conditioned leased lines. Acoustic couplers are asynchronous modems designed for dial-up use that are generally limited to speeds of 600 bits/s or less. Synchronous units operate at a maximum data rate of 4800 bits/s over dial-up and 9600 bits/s on conditioned leased lines.

Wideband modems operate over telephone transmission facilities at speeds of 19.2k bits/s to 230.4k bits/s. This class of data set is supplied almost exclusively by the common carrier and requires the bandwidth of 6 to 60 dedicated voice grade channels. Examples are the Bell 303B, -C, and -D for 19.2k-, 50k- and 230.4k-bit/s full-duplex operation.

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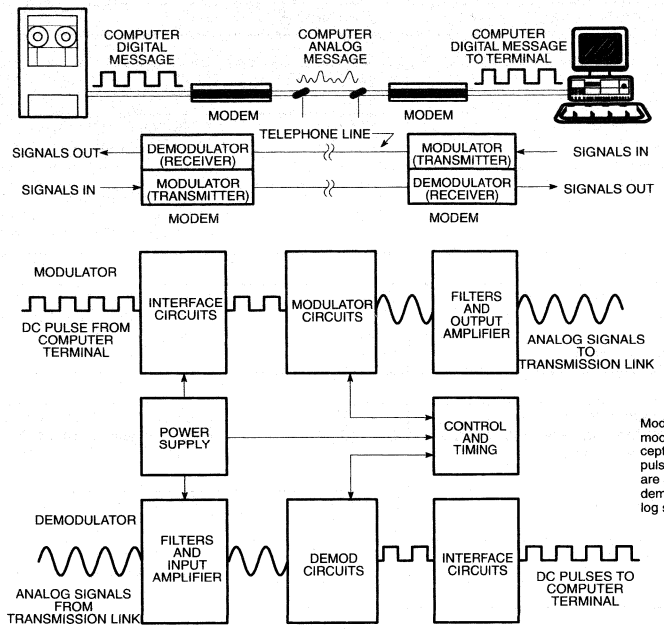


Modem is divided into two functional segments: modulator and demodulator. Modulator accepts digital input and converts squared DC pulse voltages to analog, audio signals, which are sent over transmission link. At end of link, demodulator of second modem reconverts analog signals to digital output.

Figure 2. Analog Transmission Using Modems

Short haul modems operate over relatively short distances — generally less than 10 mi (16 km) — on solid conductor, non-band limited, non-loaded lines. In some cases, they are not true modems but are line drivers and line receivers that transmit and receive digital data. Although the communication line must be carefully chosen, the cost can often be one-tenth that of a voice grade modem rated at the speed. Other advantages are higher speed and reliability and easier maintenance.

Asynchronous and Synchronous Transmission

Asynchronous data are typically produced by low speed terminals with rates of less than 1200 bits/s. In asynchronous systems [Figure 3(a)], the transmission line is in a mark (binary I) condition in its idle state . As each character is transmitted, it is preceded by a start bit, or transition from mark to space (binary 0), which indicates to the receiving terminal that a character is being transmitted. The receiving device detects the start bit and the data bits that make up the character. At the end of the character transmission, the line is returned to a mark condition by one or more stop bits, and is ready for the beginning of the next character. (An asynchronous character varies in length depending on the information code employed.) This process is repeated character by character until the entire message has been sent. The start and stop bits permit the receiving terminal to synchronize itself to the transmitter on a character by character basis.

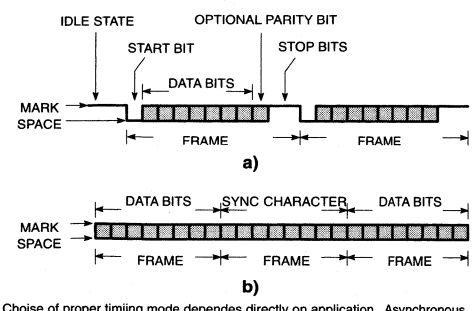
Synchronous transmission (Figure 3(b)) uses an internal clocking source within the modem to synchronize the transmitter and receiver. Once a synchronization character (SYN) has been sensed by the receiving terminal, data transmission proceeds character by character without the intervening start and stop bits. The incoming stream of data bits is interpreted on the basis of the receive clock supplied by the modem. This clock is usually derived from the received data through a phase locked loop. The receiving device accepts data from the modem until it detects a special ending character or a character terminal count at which time it knows that the message is over. The message block usually consists of one or two synchronization characters, a number of data and control characters (typically 100 to 10,000), a terminating character, and one or two error control characters. Between messages, the communication line may idle in SYN characters or be held to mark. Note that synchronous modems can be used to transmit asynchronous data, and, conversely, asynchronous modems can be used for synchronous data if the receiving terminal can derive the clock from the data.

Asynchronous transmission is advantageous when transmission is irregular (e.g., when it is initiated by a keyboard operator's typing speed). It is also inexpensive because of the simple interface logic and circuitry required. Synchronous transmission, on the other hand, makes far better use of the transmission facility by eliminating the start and stop bits on each character. Furthermore, synchronous data are suitable for multilevel modulation, which combines two or four bits in one signal element (baud). This can facilitate data rates of 4.8k- or 9.6k bits/s over a bandwidth of 2.4 kHz. Synchronous modems offer higher transmission speeds, but are more expensive because they require precisely synchronized clock and data.

A designer's review of data communications

Table 2. Communication Channel Characteristics

Modem Type	Communications Channel	Data Rates (bits/s)	Use
1. Voice grade (vg)			
a. High speed synchronous	Leased line (3002 Dial-up	4.8k, 7.2k, 9.6k 4.8k	High volume machine to machine communications. 600 to 1200 bits/s.
b. Medium speed synchronous Medium speed asynchronous Medium speed asynchronous	Leased line/dial-up Leased line Dial-up	2.4k, 3.6k 1.8k, 2k 1.2k	Interactive or low speed remote batch operations. 150 to 300 bits/s
c. Low speed asynchronous	Dial-up	300, 600	Interactive teleprinters and glass teletypewriters, data acquisition and collection. 30 to 60 bits/s
2. Wideband			
a. Super group (60vg) b. Group (12vg) c. Half group (6vg) d. Lineplexer (2vg)	5700, 5800 (TELEPAK) 8801 8803 2 leased lines	230.4k 40.8k, 50k, 56k 19.2k 19.2k	Large volume telephone line multiplexing, dedicated computer to computer links
3. Short haul			
a. Limited distance [<10 mi (<16km)]	Private wire/cable Non-loaded, non-conditioned, non-carrier line	2k to 1M 2k to 19.2k	Data communications in plant (private wire) or off premises where distance is <10 mi (<16 km) [(leased line)]
b. Medium distance [<50 mi (<80km)]	Leased line	2k to 9.6k	Intermediate distance [10 to 50 mi (16 to 80 km)]
4. Modem eliminators and line drivers/receivers	Private wire/cable	2k to 1.544M	On-premises data communications. Typical distances are 500 ft (152 m) to 2 mi (3.2 km)



Choise of proper timiing mode dependes directly on application. Asynchronous transmission (a) is used mostly with man-machine interfaces; synchronous transmission (b) offers high speed necessary for machine-machine communication.

Figure 3. Asynchronous and Synchronous Transmission

Modulation Techniques

Whether to use the dial-up network or leased lines depends on how the modem modulates data prior to sending them over the phone line. Certain modulation techniques permit higher transmission rates than others, and all modulation techniques directly affect the maximum data rate and the error performance. The three basic modulation techniques are frequency shift keying (FSK), amplitude modulation (AM), and phase modulation (PM) (Figure 4).

The most popular form of frequency modulation is FSK, in which the carrier frequency (operating at, say, 1700 Hz) is modulated ±500 Hz to present binary 1 or binary 0. Thus, a frequency of 1200 Hz represents a zero, while a frequency of 2200 Hz represents a binary 1. FSK techniques are generally quite suitable for low speed devices like teleprinters and allow operation at speeds as high as 1800 bits/s.

AM enables a modem to transmit and receive the analog equivalents of binary 1s and 0s. This technique involves varying the amplitude of the line's carrier frequency. Several levels of amplitude modulation are possible, allowing twice as much data to be sent in the same time frame. Both AM and FSK are quite suitable for data transmission; however, FSK has a noise advantage over AM, and AM allows more efficient use of the available bandwidth.

PM modems are generally described in terms of the number of phase shifts generated, and operate at speeds of 2000 bits/s and above. In this technique, the transmitted signal is shifted a certain number of degrees in response to the pattern of bits coming from the terminal or computer. For example, in a 2-phase PM modem, if the analog signal generated by the transmitting modem is shifted 180°, a binary 1 (or 0 if desired) is indicated. If there is no shift, then the signal will be interpreted as a series of zeros (or ones) until such a shift is sensed. Generally, PM modems operate in four and eight phases, permitting up to two or three times the data to be sent over the line in the same bandwidth. Most 4800- and 9600-bits/s modems use PM.

Conditioning and Equalization

As data in the form of analog signals are sent down the line between modems, they suffer from the effects of envelope delay and amplitude distortion. Signals of different frequencies are delayed or attenuated by varying amounts as they are transmitted. To compensate for these effects, two techniques are employed: line conditioning and modem equalization.

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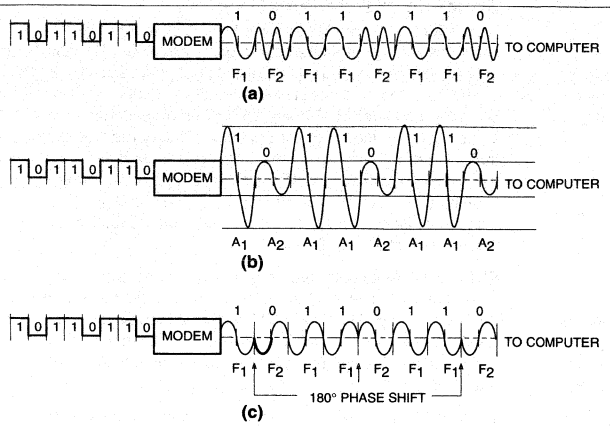


In frequency shift keying (a), digital signal (left) received by modem is shifted in frequency to represent binary 1 and binary 0. Because of the time needed to shift from one frequency to another, two is generally the maximum number used. In amplitude modulation (b), digital signals are amplitude modulated by modems using this technique. Here, one carrier signal amplitude (A1) represents binary 1, and another (A2), binary 0. In phase modulation (c), whenever 180° phase shift is encountered, receiving mode assigns value of binary 0; at all other times, value of binary 1 is assumed.

Figure 4. Modulation Techniques

Conditioning is the process by which the telephone company maintains the quality of a specific, privately leased line to a certain standard of permissible delay distortion and signal attenuation. AT&T has two types of conditioning referred to as C and D, There are five categories of C conditioning (C1 through C5) and two categories of D conditioning (D1 and D2). C conditioning attempts to equalize the drop in signal voltage and envelope delay for all frequencies transmitted; D conditioning controls the signal to noise ratio and harmonic distortion. Both may be used on the same communication channel.

Equalization refers to modem compensation for amplitude and envelope delay distortion of the line. Equalization is seldom required in lower-speed modems attached to a leased line, since minimum line conditioning is sufficient. However, conditioning and equalization are required when higher speed modems (4.8k- and 9.6k bits/s) are attached. Modems used for high speed transmission over the dial-up network must have equalization, since it is never certain exactly which unconditioned telephone line will be used.

Communication Line Sharing and Modem Sharing

When several input/output devices are required at one end of a communication link, a multiplexer or modem sharing unit, which enables these devices to share one communication line, can be used to reduce costs. Multiplexers take low speed inputs from a number of terminals and combine them into one high speed data stream for simultaneous transmission on a single channel. At the other end of the link, a second multiplexer (actually a de-multiplexer) reconverts the high speed data stream into a series of low speed inputs to the host computer. The channel is split into time slots (time division multiplexing) or frequency bands (frequency division multiplexing). Intelligent or statistical multiplexers increase line utilization by allocating time slots on the basis of a line activity algorithm.

Modem sharing units enable multiple terminals to share one modem. They are particularly valuable in networks that require clusters of terminals at remote sites because the number of modems and transmission lines are reduced. Operation is polled half-duplex. Multiport modems can split a high speed channel (e.g., 9600 bits/s) into various medium speed channels (e.g., four 2400 bits/s and two 4800 bits/s), thus permitting several medium speed terminals to share a 9600 bit/s line. A miniplexer is a device that performs channel splitting for DDS as well as for a single 3002 leased line. A lineplexer or biplexer splits 19.2 kbit/s data into two 9600 bit/s paths that can be transmitted over two conditioned full-duplex channels. This eliminates the need for a wideband channel to send and receive data at 19.2 kbits/s. A port sharing unit connects to a communication controller or central processing unit port and transmits or receives data from two to six terminals or modems. Less costly than a multiplexer, it reduces the number of controller ports in a polled terminal data communications configuration and makes more efficient use of connected ports.

Standards and Protection

The electrical, functional, and physical interface to data terminal equipment provided by modems is compatible with Electronics Industries Association (EIA) or International Consultative Committee for Telephone and Telegraph (CCITT) standards. Most commercial models conform to EIA RS-232, and plug to plug compatibility via a 25-pin connector is ensured between modems and data terminal equipment that subscribe to this standard. CCITT V.26 is the electrical equivalent of RS-232-C, while V.24 is the U.S. standard's functional pin equivalent. CCITT V.35, a current-mode, 34-pin connector interface standard for serial data transmission up to 56k bits/s, is used by wideband European modems and in the Bell System DDS Data Service Unit at 56k bits/s. Military standard (MIL-STD) 188 is a U.S. government standard for military communications equipment. An improved EIA functional standard, RS-449, was approved in November 1977.

Common carrier equipment on the switched telephone network must be protected. A device called a data access arrangement (DAA) limits the attached modem's signaling power to prevent it from exceeding the power level restrictions of the communication channel. In 1977, the FCC ruled that modem manufacturers can incorporate equivalent protective circuitry in their products, register them with the FCC, and connect them directly to the telephone network. DAAs are available from FCC-certified independent suppliers and can be leased from the Bell System. Modems rented from the Bell System or those used on leased lines do not require a DAA.

A designer's review of data communications

Protocols

Protocols provide the necessary ground rules to ensure the orderly and accurate transfer of data between digital devices. Data communications protocols are growing in importance as the terminal population increases, distributed processing becomes widespread, and new communications technologies, such as packet switching and satellite links, become commonplace.

Protocols associated with data communications have several major levels, or layers, that define various functions and operations. Each level is designed to be functionally independent of the others, but the function of each depends on the correct operation of the previous level. The protocols embodied in these levels range from those that define the physical and electrical links, e.g., RS-232-C and CCITT V.35, to those that are responsible for functions such as message buffering, code conversion, recognition and reporting of faulty conditions in terminals or lines, communication with the host mainframe, and management of the communication network. They are implemented by software packages like International Business Machines (IBM)'s Systems Network Architecture (SNA), CCITT's X.25, and Digital Equipment Corporation (DEC)'s DECnet.

The remainder of this article concerns data link control protocols (DLCs), the sets of rules necessary for effective communication between terminals and computers over conventional communications channels. DLCs are involved in handling the communications link itself and moving information across it efficiently and accurately. Their basic functions are to establish and terminate a connection between two stations; to ensure message integrity through error detection, requests for re-transmission, and positive or negative acknowledgments; to identify sender and receiver through polling or selection; and to handle special control functions such as requests for status, station reset, reset acknowledge, start, start acknowledge, and disconnect.

Structure of Data Link Controls

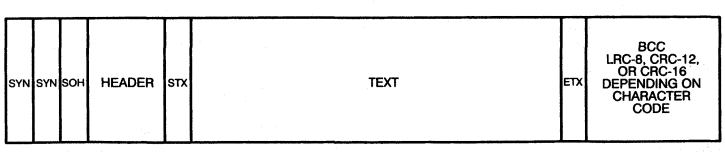
Data link controls can be classified into Character Oriented Protocols (COPs) and bit oriented protocols (BOPs). In COPs, a defined set of communication control characters effects the orderly operation of the data link. These control characters are part of a character code set. COP messages are transmitted in blocks composed of a header or control field, a body or text field, and a trailer or error checking field with characters used as field or block delimiters. Examples of COPs are IBM's Binary Synchronous Communications Protocol (BISYNC) and DEC's Digital Data Communications Message Protocol (DDCMP). Block formats for these are illustrated in Figure 5.

BOPs use only two or three specific control characters for operation of the data link. These characters are used to delimit the beginning (FLAG) and end (FLAG, ABORT, GA) of a message frame. Upon receipt of the opening FLAG, positional significance is used to delineate the bit sequence that follows into prescribed fields (Figure 5).

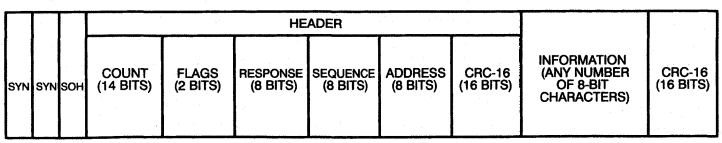
These fields are address, control, information, and frame check sequence. The address, control, and frame check fields are of fixed length; the information field length is variable and may be zero.

COP Messages

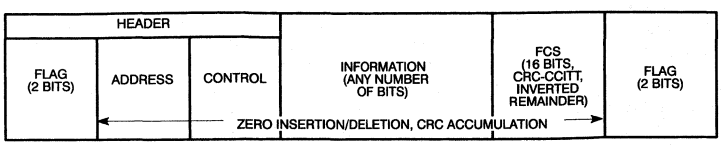
As already stated, COP messages are transmitted in units called blocks. The header field contains auxiliary information that identifies the address of the message destination or source, the job number (if any), the type of message (data or control), the control action, and a positive or negative acknowledgment to ensure error-free reception of a previous message (or messages). Control actions are used to reset or initialize a secondary station, to acknowledge good or bad reception of blocks, to inquire why a response or acknowledgment has not occurred within a specific time period, or to abort a transfer sequence. The control information is conveyed via special characters or character sequences.



a. Binary Synchronous Communications (BISYNC)



b. Digital Data Communications Message (DDCMP)



c. Bit Oriented Protocol (BOP) Block Format

SYN : SYNCHRONOUS IDLE
SOH : START OF HEADING
STX : START OF TEXT
ETX : END OF TEXT

BCC : BLOCK CHECK CHARACTER
LRC : LONGITUDINAL REDUNDANCY CHECK
CRC : CYCLIC REDUNDANCY CHECK
FCS : FRAME CHECK SEQUENCE

Byte control protocols (a) and (b) use special control characters to enforce orderly data transmission of blocks containing header, body text, and trailing data. Bit oriented protocol (c) requires only two or three special control characters; however, information must be distinguished from final FLAG.

Figure 5. Typical Data Link Control Structures

A designer's review of data communications

The text field contains any data being transmitted. The text may be characters of the information code set or may be transparent to that code set. In the latter case, pure data (binary, packed decimal, floating point), specialized codes, or machine language computer programs must be distinguished from characters in the code set being used. This is done by employing a transparent mode whose implementation depends on the specific DLC.

To ensure correct reception of information over communication facilities, a sequence of check bits, often called block check characters or BCC, are generated and transmitted as an error check field. Each block of data transmitted is checked for errors at the receiving station in one of several ways, depending on the code and functions employed. These checking methods include vertical redundancy check (VRC), a parity check on each character, in conjunction with a longitudinal redundancy check (LRC), a horizontal parity; and cyclic redundancy check (CRC), which involves a polynomial division of the bit stream by a CRC polynomial.

BOP Messages

BOPs are more straightforward and universal than the COP just discussed. BOP messages are also transmitted in frames, and all messages adhere to one standard frame format. Common characteristics of BOPs are the independence of codes, line configurations, and peripherals; the use of positional significance instead of control characters or character counts; one standard frame format for all messages; the possibility of half- or full- duplex operation; the achievement of information transparency through zero insertion and deletion; and error checking on a complete frame.

A frame starts with the 8-bit FLAG sequence, followed in order by the sequences ADDRESS, CONTROL, INFORMATION (if present), and FRAME CHECK, and ends with another FLAG sequence. Each station attached to the data link continuously searches for the FLAG sequence and an ADDRESS sequence. In multipoint operation, for example, a secondary station must detect a FLAG immediately followed by its own ADDRESS to enable the receiver.

When the primary station transmits, the station ADDRESS sequence, which is usually one 8-bit field, designates which secondary station is to receive the balance of the transmitted frame. When a secondary station transmits, the ADDRESS tells the primary station which secondary station originated the frame. A secondary station must recognize its valid address before it can accept a frame and take any action on the contents of that frame. Also, the primary station will accept a frame only when it contains the address of a secondary station that has been given permission to transmit. To ensure the integrity of the data being transmitted, the ADDRESS sequence appears within each frame. This enhances flexibility in that the primary station can interleave receptions from several secondary stations without intermixing individual station information transfers.

The CONTROL field follows the ADDRESS sequence and is composed of one or two 8-bit bytes, depending on the protocol implementation. It is the heart of the BOP message, for it determines the type of message, the send and receive frame sequence counts, and a poll command from the primary station or final response from the secondary station. The primary station uses CONTROL to tell (command) the addressed secondary station what operation to perform. The secondary station uses CONTROL to react (respond) to the primary station.

The INFORMATION field may vary in length; this includes different lengths in the sequential frames making up a complete transmission. The data may be configured in any code structure: straight binary, binary coded decimal, and packed decimal, among others. However, the content of the field must be self-defining by actual or implied means. For example, peripheral device control characters, such as carriage return, will actually be part of the INFORMATION field, while the code being used may be implied in the address of a

Table 3. Common Protocol Characteristics

Feature	BiSYNC	DDCMP	SDLC	ADCCP
Full duplex	No	Yes	Yes	Yes
Half duplex	Yes	Yes	Yes	Yes
Message format	Variable	Fixed	Fixed	Fixed
Link control	Control character, character sequences, option header	Header (fixed)	Control field (8 bits)	Control field (8/16 bits)
Station addressing	Header	Header	Address field (8 bits)	Address field (8 bits to 00)
Error checking	Information field only	Header, information field	Entire frame	Entire frame
Error detection	VRC/LRC-8 VRC/LRC-16	CRC-16	CRC-CCITT	CRC—CCITT
Request for retransmission	Stop and wait	Go back N	Go back N	Go back N, selected reject
Maximum frames outstanding	1	255	7	127
Framing —start	2 SYNs	2 SYNs	Flag	Flag
—end	Terminating characters	Count	Flag	Flag
Gaps between characters allowed	Yes	No	No	No
Information transparency	Transparent mode	Inherent (count)	Inherent (zero/insertion/deletion)	Inherent (zero/insertion/deletion)
Control characters	Numerous	SOH, DLE, ENQ	None	None
Character codes	ASCII EBCDIC Transcode	ASCII (control character only)	Any	Any

A designer's review of data communications

specific terminal designed for a specific code. Furthermore, whether a frame contains an INFORMATION field at all depends on the particular CONTROL format transmitted. Table 3 presents a comparison of common DLCs.

Synchronization Techniques

Four kinds of synchronization — bit, character, block and message — must be distinguished when using synchronous transmission. Bit synchronization is achieved through a received clock signal which is coincident with the received serial data stream. Most modems or "business machines" (i.e., terminals) derive this clock by means of phased lock loops from the 0 to I and I to 0 transitions occurring in the received data. This technique, called self-clocking, overcomes the effect of propagation delay between distant stations and the tendency of electronic circuits within the modem to drift.

Character synchronization is accomplished by recognizing one or two "phasing" characters, often called SYN or sync characters. The receiver senses these SYN characters and phases its receive logic to recognize, by bit count, the beginning and end of each subsequent character. To ensure character synchronization throughout a message, SYN sequences are sometimes inserted in the transmitted data stream at 1- or 2-second intervals. This permits receiving stations to verify that they are in sync.

Request for Re-transmission

As previously mentioned, DLCs include an error checking field to allow the receiving station to validate the message. When errors are detected, the receiving station issues a request for re-transmission (ARQ). The two types of ARQs are stop and wait and continuous Each provides defined methods for acknowledging correct (error free) reception of transmitted blocks of information.

When a connection is established in the stop and wait ARQ, the transmitter sends one block and then stops. Eventually, the receiver acquires that block, subjects the block to an error check, and then sends an ACK control character to the transmitter to indicate that the block is correct, or a NAK control character to indicate an error. If an ACK is returned, the transmitter sends the next block in sequence. If a NAK is returned, that block is re-transmitted. Thus, the stop and wait mode involves periods of idleness, including propagation delays between each block, so that the line is not communicating nearly at its rated capacity.

In continuous ARQ, the transmitter keeps sending one block after another without stopping. The receiver and transmitter retain individual counts of the blocks outstanding and provide buffer storage to retain those blocks. Only when an erroneous block is detected does the receiver tell the transmitter to re-send that block and all subsequent in-transit, but unacknowledged, blocks.

Summary

As the installed base of computers and the speed and volume of their output have increased, so has the need to transmit that output to more places over longer distances. Inherent in the data communications process — the electronic transmission of encoded information from one point to another — are various physical elements, devices, and systems, as well as standards and procedures. An understanding of these basic elements and concepts can help users of computer services to take advantage of the communication systems that are now available.

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Complex datacom peripheral ICs interface to many processors

Revised by: A. Kazmi

Single-chip datacom peripherals have become so powerful they now implement a variety of software-selectable protocols. A large family of such devices is designed to interface to the 68000 and 80x processor families.

With computing power and memory dropping in price, you can now cost effectively put computational capability closer to where information is gathered or displayed. To capitalize on this distributed-processing trend, you must be aware of how to make various system elements communicate. Thus, you must be familiar with communication protocols and the ways to implement them with the variety of datacom peripherals now available.

First select the protocol

Protocols are the standard procedures and conventions that govern the transfer of data among communicating data-processing machines (see reference). They're classified by the manner in which they allow data to be transmitted, and for the purposes of this article (which addresses device-to-device links rather than bus-architecture interconnects such as local-area networks), you must be familiar with the terms asynchronous, synchronous, bit oriented and byte oriented protocols.

In asynchronous systems, transmission begins with a Zero/One transition that, when held long enough, becomes the start bit. Thus, the receiving node doesn't have to anticipate a transmission, and the structure of unique start and stop bits allows the receiver to synchronize itself to the transmitter on a character-by-character basis. In practical applications, you'll typically find asynchronous data in low-speed terminals with bit rates less than 1200 bps.

For higher speed synchronous transmission, the protocol coordinates the sending and receiving stations. There are two broad categories of protocols used in synchronous communication known as character-oriented protocols (COPs) and bit-oriented protocols (BOPs). COPs, dominated by IBM's Bisync and DEC's DDCMP, use units called blocks; in addition to data, these blocks contain error-checking and -correcting information. BOPs, although relatively new, have proliferated quickly; they're more straightforward in structure and application than COPs. BOP messages are transmitted in frames, and all messages adhere to a common format. Two of the most common BOPs are HDLC (ISO's high-level data-link control) and SDLC (IBM's synchronous data-link control). And while COPs can work in asynchronous as well as synchronous mode, BOPs can't. datacom peripheral chips now exist to help you implement all these protocols.

Look over this family tree

If your design goal is a system with minimum cost and maximum reliability, you'll likely investigate single-chip implementations for the central controller and protocol peripheral. One large family of datacom peripherals revolves around the 68000 and 80x processor families.

These parts often have dual numbers such as the 2681 and 68681. The former is the processor-independent version; the latter offers direct 68000 interface with minimum glue circuitry. If the last three digits of the part numbers are the same, their internal control sections are virtually indistinguishable. Understanding this fact gives you a head start in selecting the correct device for a particular processor and protocol. Following is a list of some of the more popular devices that you can now obtain; they appear in numerical order:

- 2652/68652 multiprotocol communications controller (MPCC) — dedicated to synchronous protocols and formats. It transmits and receives bit- and character-oriented protocols and also includes extra support for Bisync operation. Because the device can recognize and create special characters such as message delimiters (flags), sync characters and other link-control operators, it further enhances synchronous-communications transparency for bit-oriented protocols.
- 2661/68661 enhanced programmable communication interface (EPCI) — an upgraded version of the popular 2651 PCI. It functions as a universal synchronous/asynchronous receiver/transmitter (USART) that provides special support for Bi-sync. The EPCI also provides features that free the host from preprocessing data. For instance, if the µP can't feed data to it fast enough, it inserts control characters that serve as controlled datacom Wait states so the controller doesn't lose synchronization with the other node or otherwise lose data.

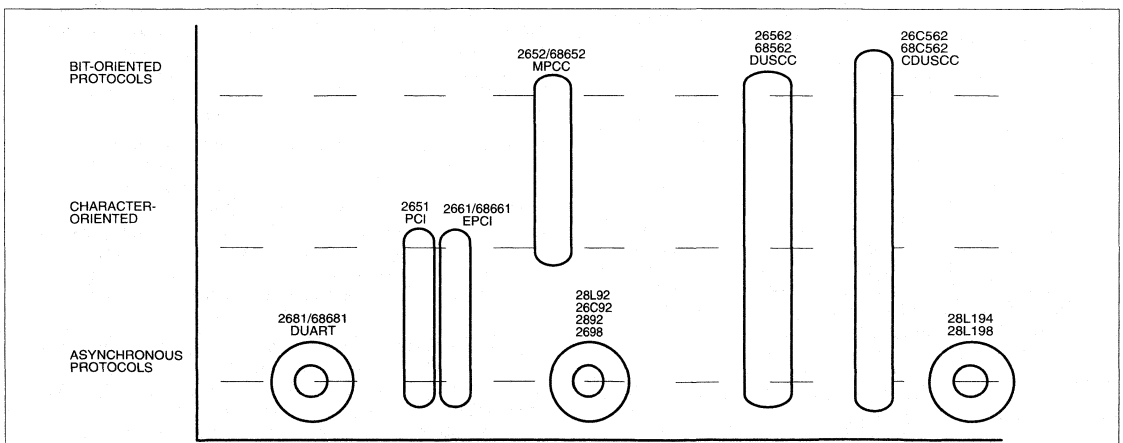
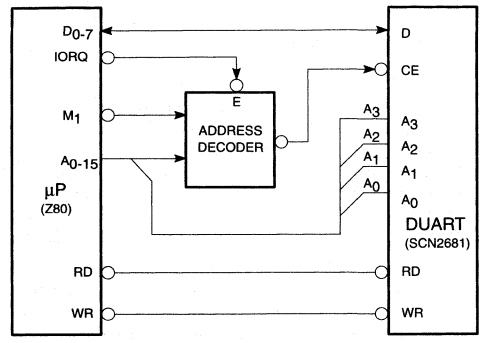


Figure 1. Philips Data Communication Products

Complex datacom peripheral ICs interface to many processors

- 2681/68681 dual universal asynchronous receiver/transmitter (DUART) — this dual-channel device performs well with 8- and 16-bit processors. The 2681 provides enhancements compared with single- and dual-channel UARTs: In addition to its two asynchronous data channels, it offers independent bit-rate generators (BRGs), self testing and interrupt handling. Moreover, you can use it in either polled or interrupt-driven systems. The 2681 comes in configurations of 24, 28 or 40 pins, each with different levels of I/O. For interfacing to the 68000, the 40-pin 68681 supplies the asynchronous handshake signals that the 68000 requires as well as an interrupt vector in response to receipt of an interrupt-acknowledge signal.
- The SC26C92 is a CMOS dual full duplex UART that is pin and software compatible with the previous SCN2681 and SCC2692. It features 8 byte FIFOs for each transmitter and receiver with four interrupt levels for each FIFO. Internal baud rates are provided to 230.4Kb; to 1Mb with an external clock.
- The SC28C94 is configured as four independent CMOS UARTs. It features 8 byte FIFOs for each receiver and transmitter with internal baud rates from 50b to 460.8Kb; to 1Mb with external clock. Its principle difference from the traditional Philips family UARTs resides in arbitrating interrupt system which drives a context sensitive configurable interrupt vector. Two 16 bit programmable counter/timers are provided with four I/O pins for each UART.
- The SCC2698B is a CMOS octal UART based upon the previous design of Philips UARTs and is software compatible with previous SCC and SCN type devices. It features 8 full duplex and independent UARTs with internal baud rates from 50b to 115.2Kb, four open-drain interrupt pins, four 16 bit programmable counter/timers and a multiplicity of general purpose output pins. Automatic RTS/CTS hand-shake is supported for all channels.
- The SC28L198 is a CMOS octal UART based upon the SC28C94. It features 16 byte FIFOs for each receiver transmitter, internal baud rates from 50 to 460.8Kb; to 1Mb with an external clock. It has an arbitrating interrupt system which drives a context sensitive and configurable interrupt vector. Its new features include programmable control of a fully automatic Xon/Xoff function, Multidrop character recognition, a general three character recognition system and a synchronous or asynchronous bus interface operating at a nominal 33MHz.
- The 26562 and 68562 Dual Universal Serial Communications Controller (DUSCC). This dual channel communication controller offers synchronous and asynchronous modes. In synchronous mode it offers Bit Oriented Protocols (BOP) such as HDLC, SDLC, etc. and Character Oriented Protocols (COP) such as BiSYNC, DDCMP, etc. It offers a wide range of Tx/Rx clock selection, one counter/timer per channel and an easy to use DMA interface. DUSCC has an on-board DPLL to reconstruct clock from receive data and various data encoding schemes such as NRZ, NRZI, FM and Manchester. DUSCC offers various methods of error detection ranging from parity generation/detection to CRC–16 generation detection (it also includes LRC and VRC methods). The 68562 provides bus interface signals for Mot 68000 family and 26562 provides bus interface with Intel 80x family. DUSCC can be used in interrupt or vector driven environments for control purposes and in DMA, interrupt and vectored mode for data I/O purpose.
- The 26C562/68C562 CMOS Dual Universal Communication Controller (CDUSCC) is an enhancement of its predecessor NDUSCC. It offers faster bus interface and higher serial data rate. It also offers deeper FIFOs, more standard baud rates, better interrupt control/enabling scheme and reduced power consumption.

These devices allow datacom designers to easily address protocol requirements in either synchronous or asynchronous mode because the controllers take over much of the datacom requirements for interpreting protocol rules.



Asynchronous interfacing can be simple, especially for 8-bit designs. This Z80/SCN2681 dual universal asynchronous receiver/transmitter (DUART) interface requires only one address decoder.

Figure 2. Asynchronous Interfacing

Design examples use similar software

Whether used individually or in combination, the Philips Semiconductors datacom interface chips support most standard protocols for device-to-device communications. To help you select the proper device for your system, consider the following design examples. Note that these examples don't provide software listings because they all operate on the same basic principles, and the routines would vary little.

Prior to initiating data communications, you must instruct the controller to program in the peripheral's operational mode by performing write operations to the Mode and Command registers; likewise, you can re-configure the devices any time during program execution. But if you do, be sure to disable the transmitter and receiver pair prior to loading the new command and mode information, or else you run a high risk of truncating a character during transmission or losing it during reception.

Once initialization is complete, software can control the transfer of information by either polling or interrupt subroutines or DMA operation. In all cases, the software must determine the request, whether for transmit- or receive-data requests. In addition, the routines should check for any errors that might have occurred and resolve those problems. In all cases, the routine must reset the condition that indicated the request. In most cases, it does so by reading or writing data to appropriate buffers on the communication chip.

Hardware design should be just as straightforward, if not easier. Take for example the asynchronous interface circuit in Figure 2, which serves simple datacom tasks such as connecting dissimilar communication devices like printers and modems. It uses the 2681/68681 DUART, which interfaces to either an 8- or 16-bit system with relatively few parts; this I/O-mapped Z80 interface requires only an address decoder. The processor's MI signal inhibits

Complex datacom peripheral ICs interface to many processors

the Chip Enable signal during interrupt-acknowledge cycles. A Wait state ensures that the data lines settle before the peripheral reads the data. And as simple as this circuit seems, the Z80/2641 UART interface is even simpler. It also requires only a decoder, but reduces the number of connections to eight data lines, the Chip Enable signal and three address lines for device selection and read/write control.

Compare the simplicity of Figure 2's 8-bit interface to the 16-bit interface in Figure 3. Part of the latter's complexity, however, arises because the DUART takes advantage of the DMA capability provided by the 68430 DMA interface (DMAI). The DMAI provides all the signals necessary to interface to the 68000 as both a peripheral and system master. The control signals drive the bus directly, while five other ICs demultiplex the address/data bus from the DMAI. During a register read/write cycle, U_4 and U_5 function as bi-directional data buffers and U_1 serves as an input buffer for the register address. U_1 to U_3 are active during the DMA operation and drive the memory address onto the bus.

The rest of the circuitry interfaces the DUART as a 68000 peripheral or a DMAI device. The address lines to the DUART come from multiplexer U_6, and the DMAI selects U_6's output with its $\overline{Own}$ signal (Own is an output-control signal asserted during DMA transfers). The controller thus selects between two sets of multiplexer inputs: the address bus and $\overline{Uds}$ (upper data strobe) or a hardwired address.

Because of its two channels, the DUART is normally addressed at even or odd memory locations. To address contiguous memory locations, however, try ANDing the DUART select with Lds or Uds (U_8 and U_9) to generate the DUART Cs signal, and then use Uds for the DUART least significant address. The hardwired address, selected during DMA operations, addresses the transmitter/receiver registers. The most significant bit of this address comes from flip flop U_7, which determines the channel that is accessed. The system sets the flip-flop during the initialization process.

To control the data path to the DUART during system and direct memory access, multiplexer U_{10} gates the DUART's $\overline{Cs}$ and $R/\overline{W}$ signals. The ANDed signals from U_8 and U_9 also enable the proper transceiver buffer for the data to or from the DUART through multiplexer U_{10}. During DMAI operation, RI_W is inverted to the DUART because a memory read is a write to the DUART.

During host access, the system requires a Dtack (data transfer acknowledge) signal at the proper time. For that purpose, U_8 and U_{13} gate the DUART's Dtack signal onto the system bus during host access. Finally, the interrupt request (Intr) asks for a DMA operation by being routed to the DMAI's Req input. When a DMA transfer is in process, the Dtack from the DUART serves as $\overline{Rdy}$ for the DMAI.

Complex datacom peripheral ICs interface to many processors

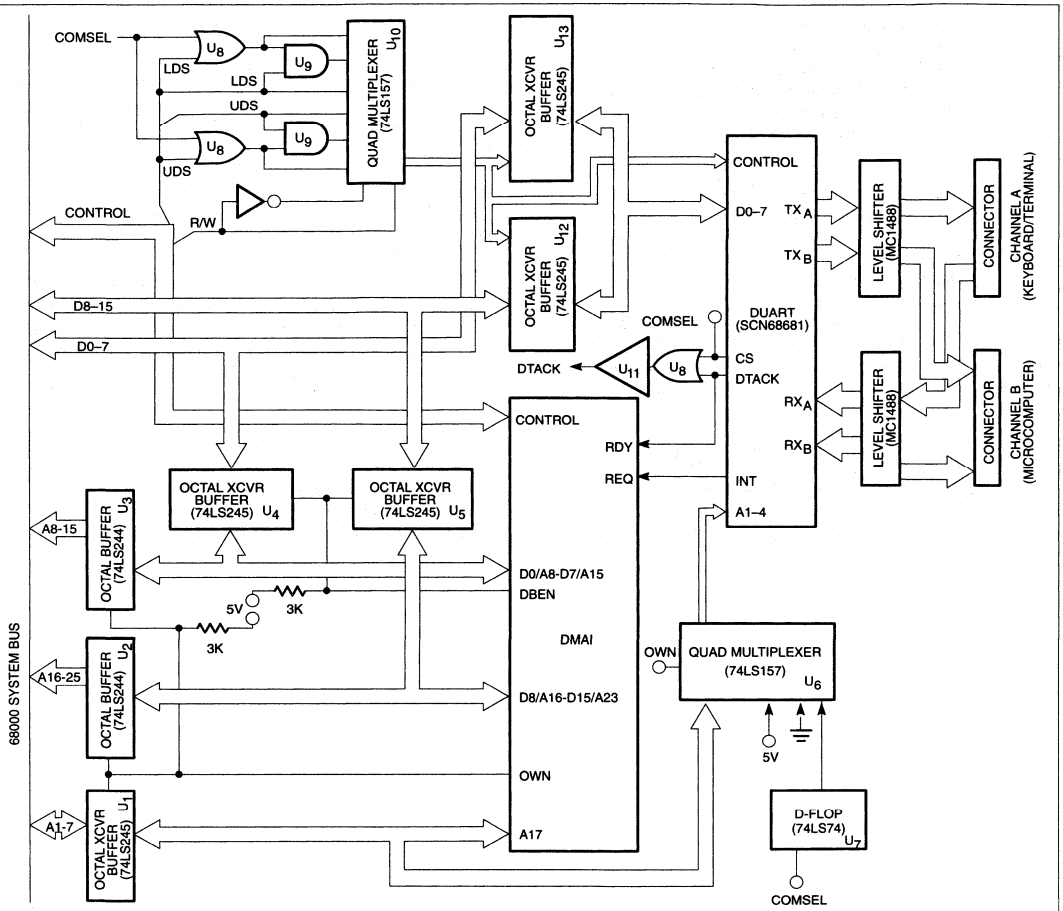


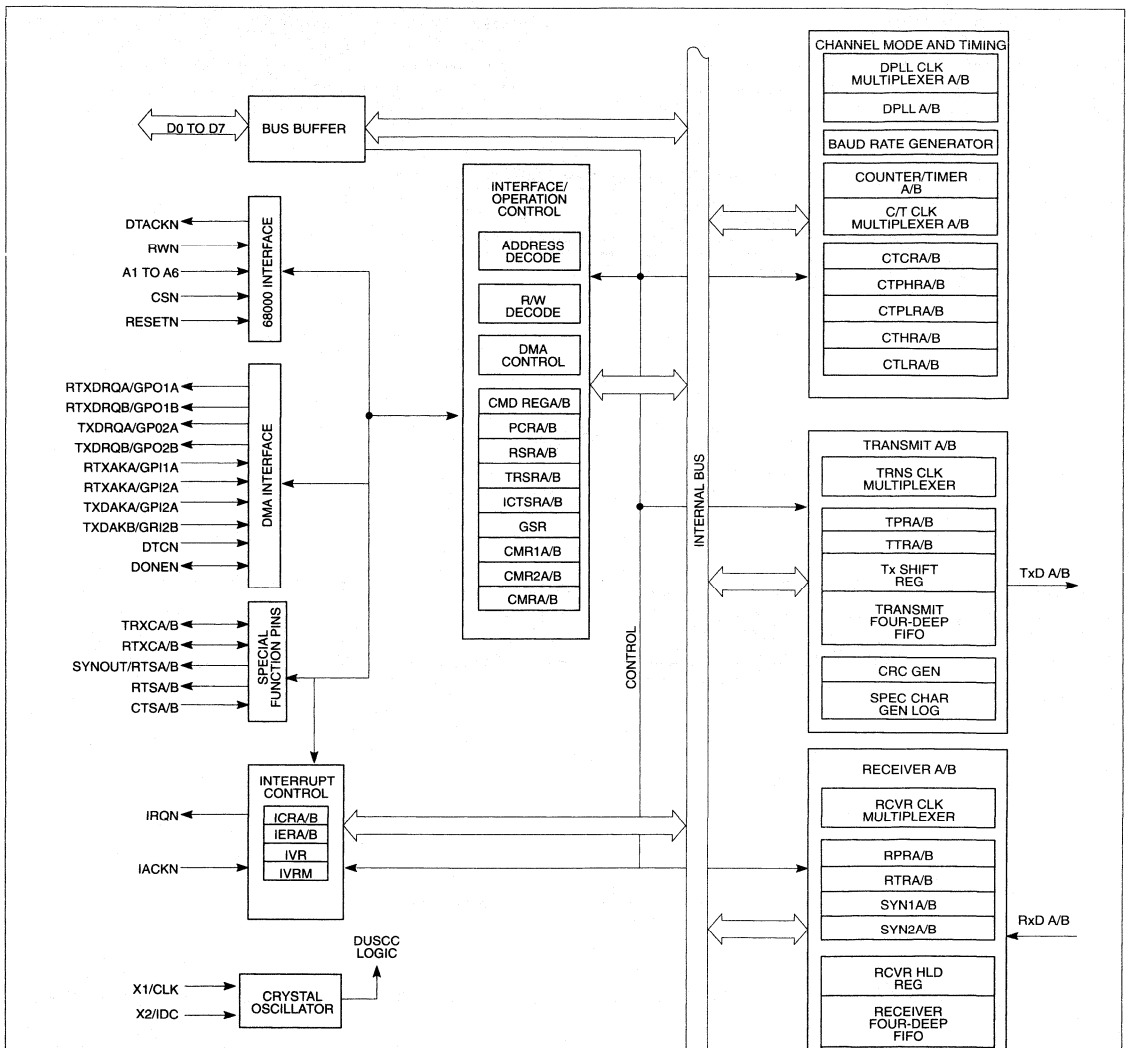
Figure 3 – To add DMA to asynchronous capability with the 2681, add the direct memory access interface (DMAI) to the design. The DMAI provides the control signals necessary to interface to the 68000 as both a peripheral and system master.

Controller contents with multiple protocols

The most widely used data communication protocols are now supported by a single-chip controller that requires minimum external hardware.

The need to transfer large amounts of data at high speed between several different local workstations and large computer systems has generated a variety of message transaction schemes or protocols. While several protocols have evolved, development of dedicated controller ICs to handle them has not kept pace.

A single-chip VLSI device from Philips Semiconductors, the SCN68562 Dual-Channel Universal Synchronous Communications Controller (DUSCC), incorporates circuitry for virtually all subsystems and functions required in advanced data communication systems. The chip provides interfacing to advanced DMA controllers and supports such interrupt structures as vectored, daisy chained, priority, and masked using minimum external logic. In many applications, the DMA and interrupt interfaces are implemented easily through direct connections from the DUSCC's request and acknowledge lines to the control bus.



Almost all data communication protocols and functions are supported by the Philips Semiconductors SCN68562 communications controller (DUSCC) chip's interface and operational control section, timing circuitry and channel receivers and transmitters. The VLSI device's hardware simplifies such system operation as DMA interfacing and setup of interrupt mechanisms.

Controller contents with multiple protocols

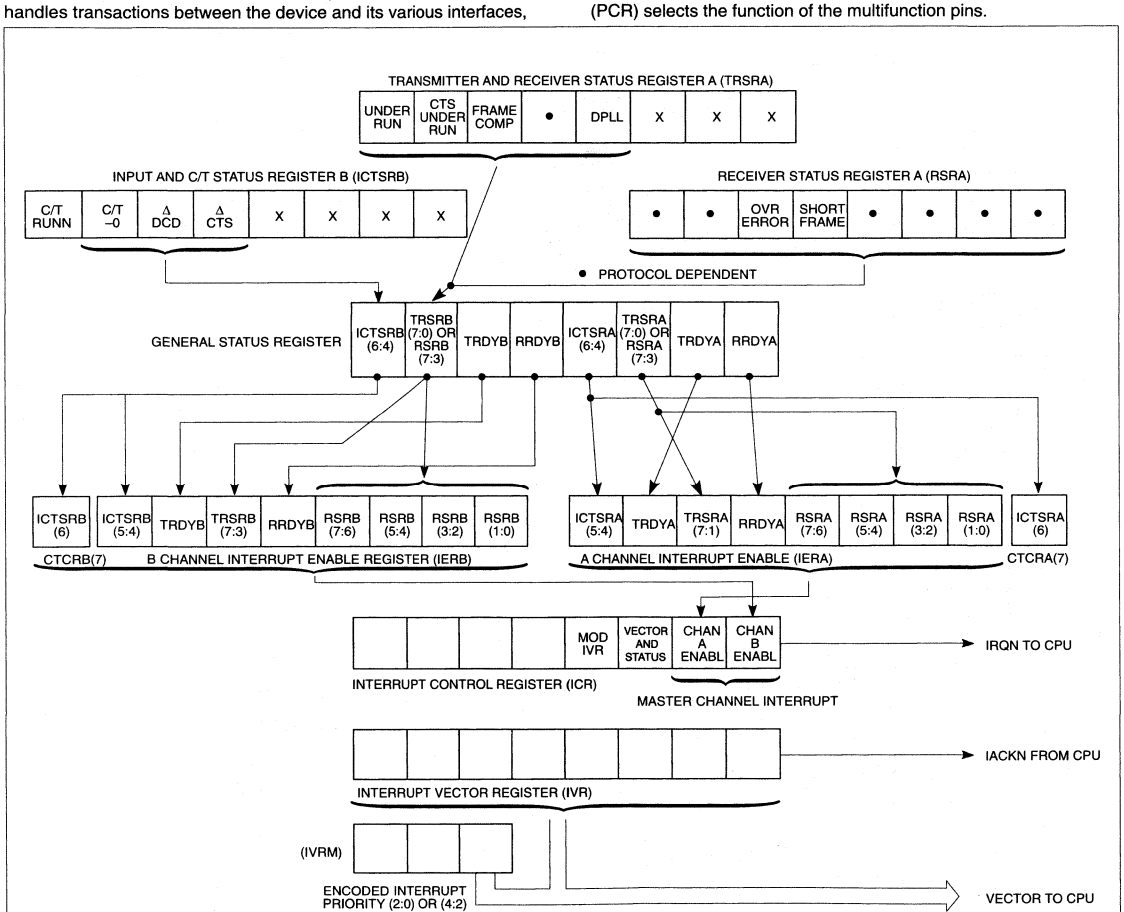
The DUSCC's two independent data communications channels permit substantial programming flexibility for handling multiple protocols. Because of variations in bit- and character-oriented protocols, a controller must provide a more encompassing solution for high performance data communication systems. For example, when the transmitter/receivers can be operated either as full-duplex synchronous or asynchronous channels, the chip can embrace a broad range of advanced bit- and character-oriented protocols, including HDLC/ADCCP, SDLC, X.25, X.75 link level, IBM Bisync, DDCMP, and X.21.

An architectural overview

Architecturally, the DUSCC has four major sub-sections: interface and operational controls, timing circuitry, channel receivers, and channel transmitters. The interface and operational control section handles transactions between the device and its various interfaces, coordinates activities between the other sections, and executes commands. Interface circuitry extends to a host processor, an interrupt structure, the DMA, and multifunction pins.

The host processor interface is dedicated to the complete set of control, data, and bus signals for the 68x and 80x processor families. Eight DMA interface pins can be configured to provide individual DMA request and acknowledge signals for the individual transmitters and receivers. An additional control signal, DONE, provides flow control. For example, it can signify the completion of a message sequence and the termination of DMA operation.

A triple set of registers configures each channel. The channel-mode configuration pair (CMR1 and CMR2) selects the channel protocol/transmission mode, message format, and error-check sequence. The system interface and pin configuration register (PCR) selects the function of the multifunction pins.



A variety of interrupt schemes including vectoring, daisy chaining, and masking can be set up through the DUSCC's interrupt control register (ICR) and interrupt enable register (IER). The ICR determines the relative interrupt priorities of one data communication channel with respect to the other. Channel interrupt conditions are enabled in the IER.

Controller contents with multiple protocols

Interrupt masking can be performed either on individual groups or channel interrupt conditions using the IER, or on an entire channel under control of the ICR. In addition to handling interrupt request and acknowledge signals, the DUSCC provides a mechanism to create interrupt daisy chains using its X2/IDC pin to propagate the interrupt acknowledge signal. Most application timing functions can be derived from the DUSCC's internal timing circuitry. This section consists of independent 16-bit timer/counters and digital phase locked loop (DPLL) circuits for each channel, and a common crystal clock and baud rate generator. Clock signals for the transmitters and receivers can be selected from an external source or from one of the internal sources mentioned above.

The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2/IDC pins or from an external clock connected to the X1/CLK pin. The oscillator's output provides the clock signal for the DUSCC's logic and other internal timing circuits.

The baud rate generator runs off the oscillator signal or on the external signal, generating 16 baud rates simultaneously. These signals are made available to the receiver, transmitter, DPLL, and counter/timer. Since the 16 baud rates are available simultaneously, each receiver and transmitter can select its baud rate independently.

Each channel includes a DPLL that is used in synchronous modes to recover clock information from the received data stream. The DPLL contains a 6-bit counter that is incremented by sampling a clock signal at 32 times the nominal data rate. The clock source can be from an external input, the receiver baud rate, the counter/timer, or the crystal oscillator. The DPLL uses the sampling clock signal together with the received data to construct a data clock that can be used as the DUSCC receiver data clock, transmitter clock or both. This results in a DPLL square wave output clock at a data rate that can be programmed to be sent out on a special pin. Users can select NRZ/NRZI, FM0, FM 1, or Manchester as the encoding format of the received data.

Transmitter/receiver flexibility

Dedicated hardware is integrated within the transmitter and receiver circuits to generate and detect special character sequences, to generate various error sequences and to handle many of the overhead tasks associated with advanced message formats. The large number of operational registers for each channel and the concise set of control commands allow easy setup and operation of the DUSCC.

Each transmitter channel consists of three major sections: clock multiplexer and control registers; TxFIFO and shift register; and special character generation logic. After a channel is configured for a protocol/transmission mode, transmitter operation is refined by the contents of the transmitter parameter register (TPR) and the transmitter timing register (TTR).

The transmitter's clock source is selected from inputs to the transmitter-clock multiplexer. Inputs are the channel counter/timer, the other channel's counter/timer, baud rate generator, DPLL, or an external clock signal. The TPR selects the clock source and baud rate if the baud rate generator is chosen as the transmitter clock signal.

The transmitter accepts parallel character data from the data bus and loads the data into the transmitter FIFO register (TxFIFO), which consists of four 8-bit holding registers. Data is then moved to the transmitter shift register (TxSR), which serializes it according to the transmission format. The TxSR can also be loaded from special character logic or from the cyclic redundancy check/longitudinal redundancy check.

The transmitter-ready signal, TxRDY, indicates the status of the TxFIFO and is set either when an empty position exists in the FIFO or if the entire FIFO is empty. The user can choose the frequency of service requests because the DMA and interrupt service request follow the state of TxRDY.

The receiver architecture is basically similar to that of the transmitter. The receiver consists of a clock multiplexer and control registers, FIFO and shift register, receiver data path, and error accumulation logic. After a channel is configured for the receive mode, receiver operation is refined by the contents of the receiver parameter register (RPR) and receiver timing register (RTR). The RPR selects the number of bits per character and controls operation of an external enable control line for all receiver transmission modes. The interpretation of the remaining bits in the RPR depends on the receive mode selected.

Timing signals are selected from the receiver timing multiplexer. Its inputs are an external timing source, the baud rate generator, channel counter/ timers, and the DPLL output clock. The clock source and data rate selections of the baud rate generator are made through the RTR. This register also selects the DPLL clock source from among counter/timers, external source, baud rate generator, and crystal oscillator inputs.

No single data path can support the diverse requirements of the various transmission modes efficiently. Thus, the DUSCC data path can be viewed as four separate paths — an asynchronous path and three paths to support the requirements of different protocols. Each data path is responsible for assembling characters into the receiver shift receiver (RxSR). After assembly, characters are sent to the receiver FIFO along with appropriate status information.

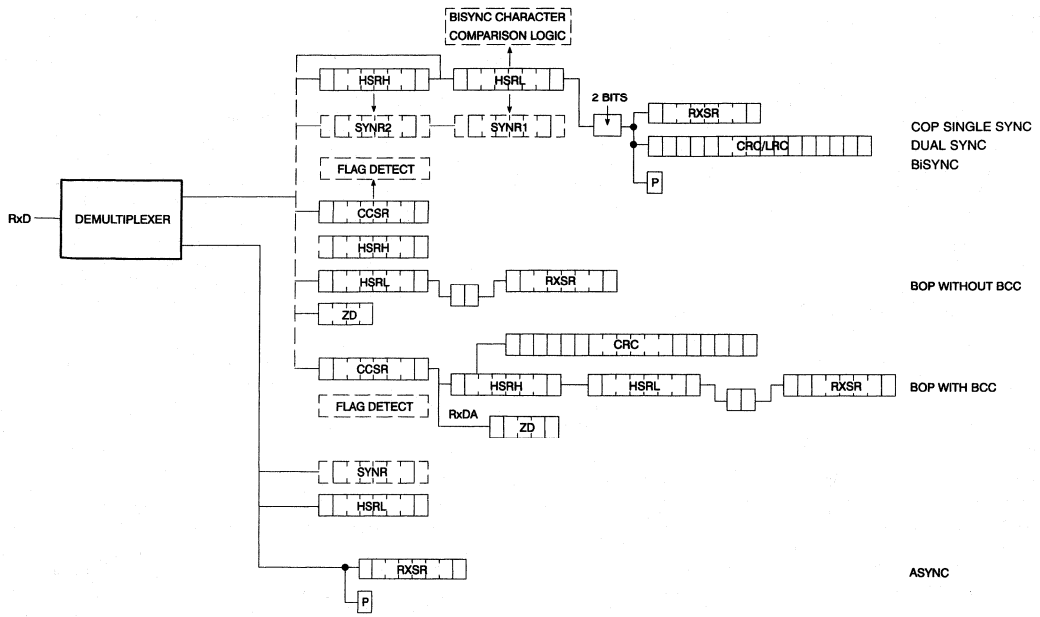
The receiver FIFO consists of four 8-bit holding registers with appended status bits. Data is loaded into the FIFO after a character is assembled; data is removed when a character is read. The state of the receiver FIFO (RxFIFO) is indicated by the receiver ready status signal (RxRDY). As in the operation of the transmitter, a user can choose when the RxRDY bit is set.

Down the data paths

The asynchronous path of the DUSCC is comprised of the holding register (HSRL) and the RxSR in parallel. The HSRL path is active only if a character comparison option is selected. In this case, all incoming data is matched against the contents of the SYN1 register on a bit-by-bit basis to determine a character match. If a match is obtained, a flag in the receiver-status register is set. This feature can be used to generate an interrupt. If the character comparison option is not selected, character data is shifted only to the RxSR. After a character is assembled in the RxSR, it is loaded into the RxFIFO.

Synchronous data paths can be pictured as one of three parallel paths that become active in the following channel conditions: a character-oriented protocol (COP) with or without a block-check character (BCC); a bit-oriented protocol (BOP) without BCC and BOP with BCC. The COP path contains the two 8-bit holding registers (HSRH and HSRL) in series with the shift register, CRC accumulation logic, two synchronizing flip-flops, and special Bisync comparison logic. Data entering this path is held first in either or both of the holding registers. During each bit time, data in the register (or registers) is compared against the contents of either the SYN1 register or the SYN1 and SYN2 registers. Comparison depends on the synchronizing pattern chosen — whether the pattern uses single or dual SYN characters. A match is indicated by the setting of a status bit in the receiver status register (RSR).

Controller contents with multiple protocols



To support the requirements of various protocols, the DUSCC provides a number of internal data paths. One path is asynchronous — the holding register (HSRL) in parallel with receiver shift register (RxSR) configuration at the bottom of the figure — while the other three paths are synchronous. Synchronous paths are used for the bit-oriented protocol (BOP) without CRC, BOP with CRC, and the character-oriented protocol (COP) including BiSYNC data communication protocols.

The BOP without a BCC path uses three parallel inputs to the character comparison (CCSR), HSRH, and HSRL registers, in series with the receiver register. In this arrangement, data is shifted into the three registers simultaneously. The holding pair of shift registers compares their contents with the SYN1 and SYN2 registers to determine if the correct station address has been received. All data entering this path is compared in the CCSR for the flag sequence. When a match occurs, the status bit in the RSR is set. Data entering the HSRL is assembled in character form in the RxSR and then transferred to the FIFO. Zero deletion occurs on all data received unless a flag or abort is detected.

In the case of the BOP with BCC data path, the CCSR, the holding registers, and the RxSR, are arranged in series. The CCSR remains active throughout a message frame and compares the incoming bit stream to determine the flag sequence. The address is compared using the 16-bit holding registers. As character data bits are shifted from the CCSR to the holding register pair, they generate the received BCC character according to the selected accumulation format of the CRC/LRC logic.

In Bisync mode, special comparison logic checks for control sequences and is active for both normal and transparent operation. Comparisons can be made either with EBCDIC or ASCII text messages as selected in the channel mode register. When detected, these sequences cause either a status bit in the RSR to be set or initiate special processing. This comparison logic makes the DUSCC a powerful tool for processing Bisync text. It frees the processor from searching for these special sequences and eliminates the need for additional processing associated with such sequences.

Minimum of hardware

An advanced two-channel data communication system can be implemented with the DUSCC. (The Table depicts the specifications for a typical data communication system supporting the different protocols.) Because so much of the hardware is already in the device, few additional parts are required.

Since the DUSCC provides separate DMA request and acknowledge signals for the transmitter and receiver, the full-duplex requirement for channel A is satisfied with a minimum of hardware between the DMA controllers and the DUSCC.

The complex vectored interrupt scheme for channel B is established by programming the interrupt control register for vectored interrupts and their formats. Separate interrupt vectors can be generated for the transmitter, receiver, and counter/timer by selecting bits in the interrupt control reg'ster. An interrupt masking can be performed through the interrupt-enable register. The interrupt interface involves simply connecting the interrupt request and acknowledge signals to the appropriate control bus signals. No additional hardware is necessary to complete this portion of the design.

A minimum of design is required to select the various interfaces for both channels. For channel A, five registers are used to select the channel interfaces and to set up the protocol requirements. Channel-configuration registers CMR1 and CMR2 establish the DMA structure and define operation of the data channel. External

Controller contents with multiple protocols

inputs are defined by the pin-control register and the address of the secondary station is stored in the SYN1 and SYN2 registers. Channel B is set up just as easily. But it requires additional programming of the interrupt control and enable registers to establish the interrupt structure.

Operating refinements for each channel are made through the transmitter and receiver parameter registers (TPR and RTR). These define the message format and select automatic features that are invoked under various transmitter and receiver conditions. The channel A transmitter, for example, is set up to terminate the BOP message automatically by sending an end of message sequence and then mark the data line when an underrun occurs. In similar fashion, channel B is set up to linefill with a sync pattern until another character is loaded into the transmitter when an underrun occurs. These actions do not require the intervention of the host processor.

Once the interfaces are established, transmitter and receiver operations are controlled and monitored through the command and the transmitter/receiver status registers. The DUSCC provides a set of commands that directly supports transmission of Bisync and BOP messages. Each command performs an action necessary to generate a message in the specific protocol. In Bisync, the first character of a message after the SYN pattern is an SOH, STX, or DLE-STX pattern. The send-DLE command not only sends the DLE-STX sequence, but the command can be appended to any character to transmit special control sequences as the protocol requires.

In BOP mode, the message frame after the flag character consists of 0 to n address bytes, followed by 1 or 2 control bytes. The sequence is transmitted by loading the data into the transmitter FIFO. After the last control byte, the transmitter switches automatically to the programmed character length. A feature of the transmitter is its ability to send the last character for a bit count less than the programmed character length by specifying a shorter character length in the output/miscellaneous register.

Section 2
Universal Asynchronous Receiver/Transmitters

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SCN2681T	Dual asynchronous receiver/transmitter (DUART)	121
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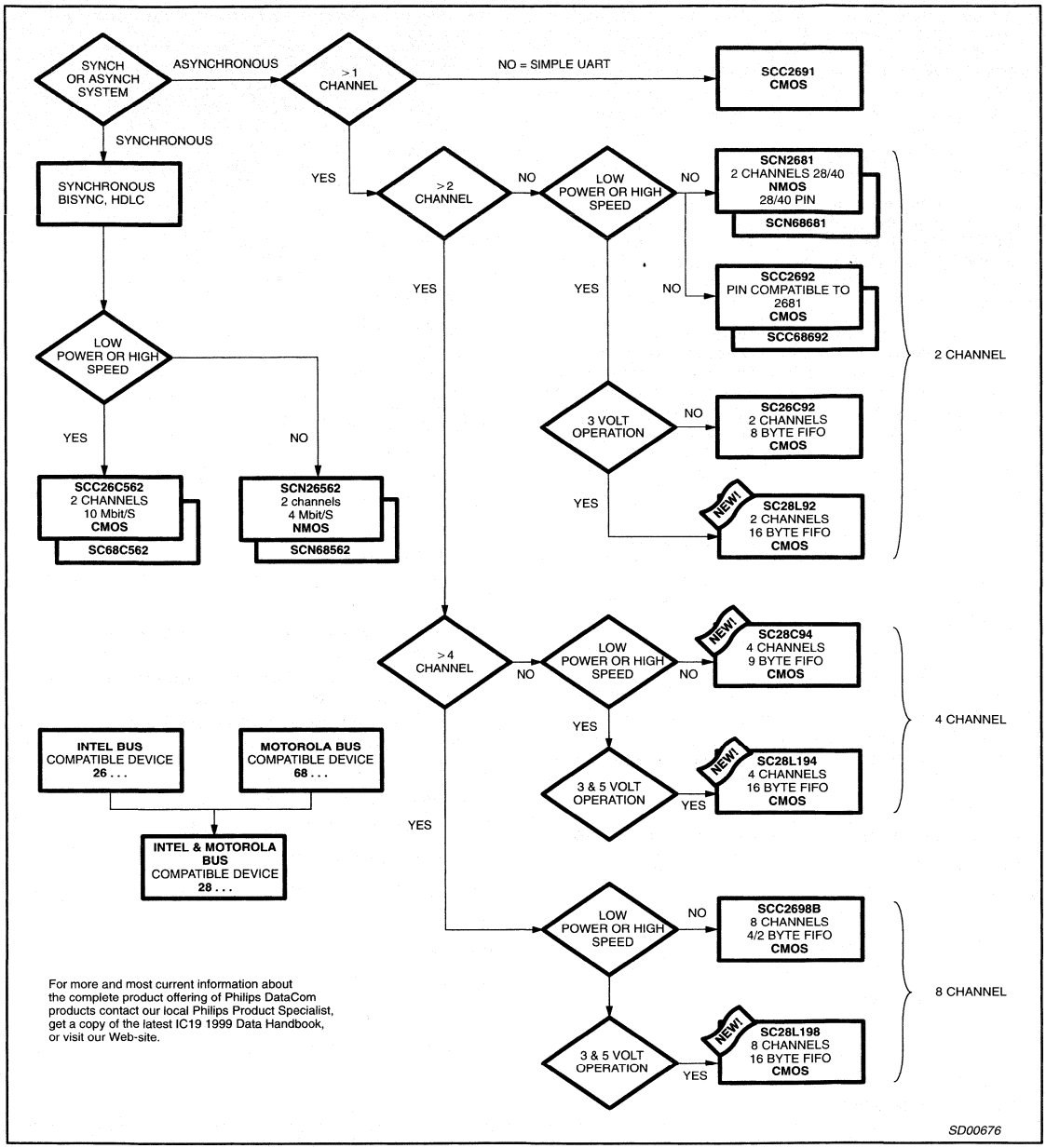
UART/DUSCC selection guide



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Dual universal asynchronous receiver/transmitter (DUART) SC26C92

DESCRIPTION

The SC26C92 is a pin and function replacement for the SCC2692 and SCN2681 with added features and deeper FIFOs. Its configuration on power up is that of the 2692. Its differences from the 2692 are: 8 character receiver, 8 character transmit FIFOs, watch dog timer for each receiver, mode register 0 is added, extended baud rate and overall faster speeds, programmable receiver and transmitter interrupts. (The SCC2692 is not being discontinued.)

The Philips Semiconductors SC26C92 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver and transmitter is buffered by eight character FIFOs to minimize the potential of receiver overrun, transmitter underrun and to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote transmitter when the receiver buffer is full.

Also provided on the SC26C92 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SC26C92 is available in three package versions: 40-pin 0.6" wide DIP, a 44-pin PLCC and 44–pin plastic quad flat pack (PQFP).

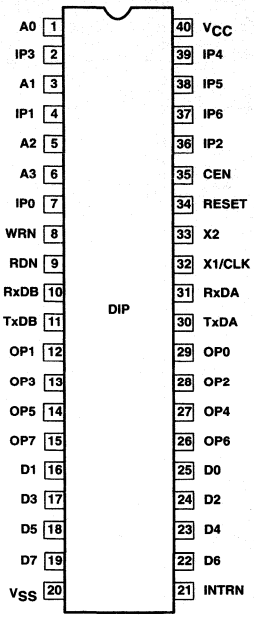
FEATURES

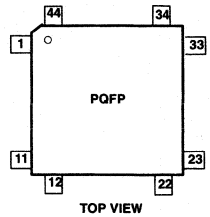
- Dual full-duplex independent asynchronous receiver/transmitters
- 8 character FIFOs for each receiver and transmitter
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- 16-bit programmable Counter/Timer
- Programmable baud rate for each receiver and transmitter selectable from:
  - 23 fixed rates: 50 to 230.4k baud
  - Other baud rates to 230.4k baud at 16X
  - Programmable user-defined rates derived from a programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
  - Multidrop mode (also called 'wake-up' or '9-bit')
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - Inputs have typically >100k pull-up resistors
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
  - Each FIFO can be programmed for four different interrupt levels
  - Watch dog timer for each receiver
- Maximum data transfer rates:
  1X – 1Mb/sec, 16X – 1Mb/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver timeout mode
- Single +5V power supply
- Powers up to emulate SCC2692

ORDERING INFORMATION

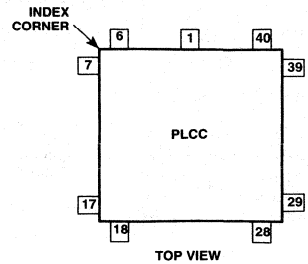
DESCRIPTION	INDUSTRIAL V_{CC} = +5V ±10%, T_A = -40 to +85°C	DWG #
40-Pin Plastic Dual In-Line Package (DIP)	SC26C92A1N	SOT129-1
44-Pin Plastic Leaded Chip Carrier (PLCC)	SC26C92A1A	SOT187-2
44–Pin Plastic Quad Flat Pack (PQFP)	SC26C92A1B	SOT307–2

PIN CONFIGURATIONS





PIN/FUNCTION		PIN/FUNCTION	
1	A3	23	N/C
2	IP0	24	OP6
3	WRN	25	OP4
4	RDN	26	OP2
5	RxDB	27	OP0
6	TxDB	28	TxDA
7	OP1	29	RxDA
8	OP3	30	X1/CLK
9	OP5	31	X2
10	OP7	32	RESET
11	N/C	33	CEN
12	D1	34	IP2
13	D3	35	IP6
14	D5	36	IP5
15	D7	37	IP4
16	GND	38	V_{CC}
17	GND	39	V_{CC}
18	INTRN	40	A0
19	D6	41	IP3
20	D4	42	A1
21	D2	43	IP1
22	D0	44	A2



PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RXDB	33	TXDA
12	NC	34	NC
13	TXDB	35	RXDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	V_{SS}	44	V_{CC}

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Figure 1. Pin Configurations

BLOCK DIAGRAM

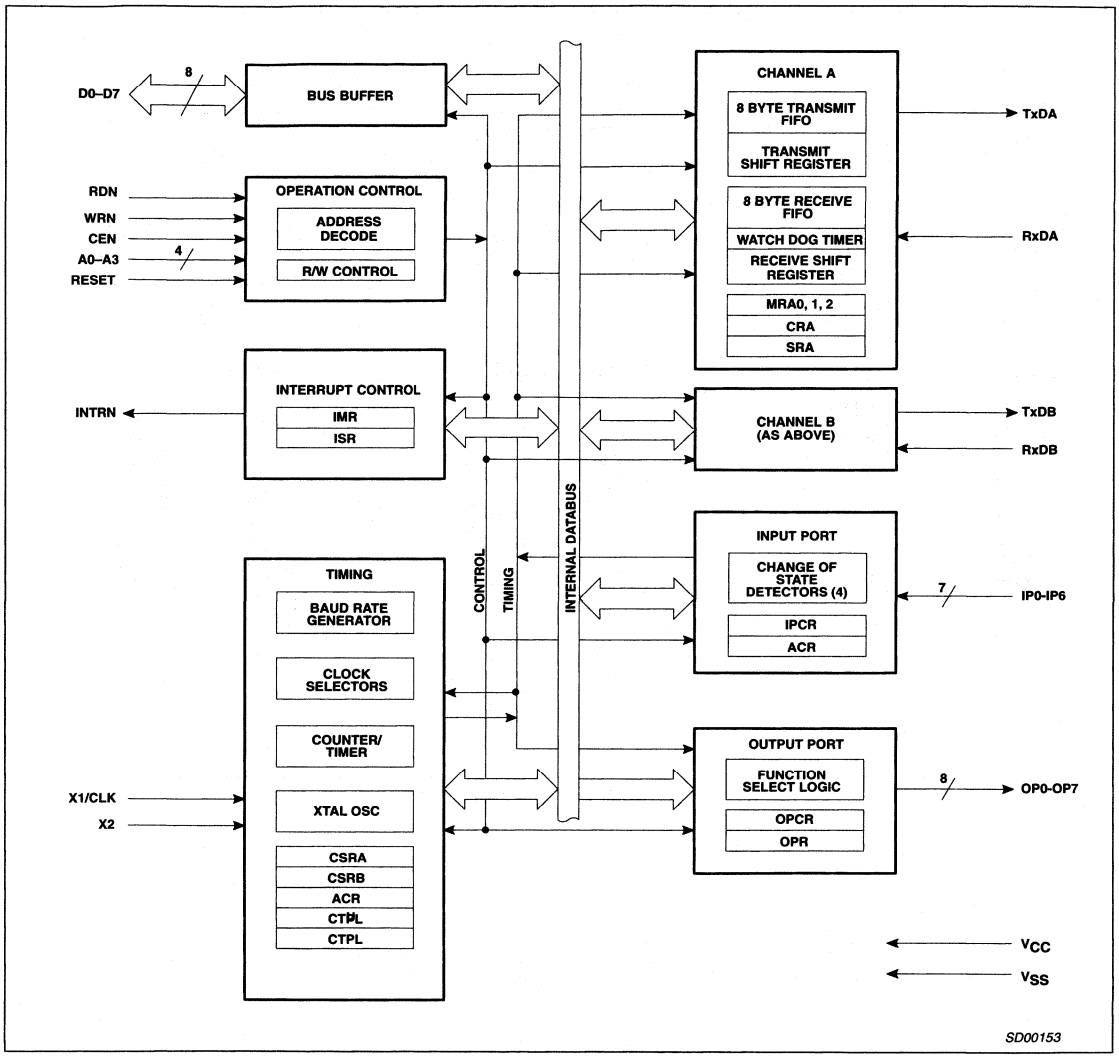


Figure 2. Block Diagram

PIN DESCRIPTION

SYMBOL	PKG 40,44	PIN TYPE	NAME AND FUNCTION
D0-D7	X	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When High, places the D0-D7 lines in the 3-State condition.
WRN	X	I	**Write Strobe:** When Low and CEN is also Low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	I	**Read Strobe:** When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0-A3	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	I	**Reset:** A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0-OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Sets MR pointer to MR1 and resets MR0.
INTRN	X	O	**Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	I	**Crystal 1:** Crystal connection or an external clock input. A crystal of a clock the appropriate frequency (nominally 3.6864 MHz) must be supplied at all times. For crystal connections see Figure 7 (included in CD-ROM version), Clock Timing.
X2	X	I	**Crystal 2:** Crystal connection. See Figure 7 (included in CD-ROM version). If a crystal is not used it is best to keep this pin not connected although it is permissible to ground it.
RxDA	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	X	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	X	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	X	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	X	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	X	O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	X	O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	X	O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxA interrupt ISR[1] output.
OP5	X	O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxB interrupt ISR[5] output.
OP6	X	O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxA interrupt ISR[0] output.
OP7	X	O	**Output 7:** General purpose output, or Channel B open-drain, active-Low, TxB interrupt ISR[4] output.
IP0	X	I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP1	X	I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP2	X	I	**Input 2:** General purpose input or counter/timer external clock input. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP3	X	I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP4	X	I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP5	X	I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP6	X	I	**Input 6:** General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
V_{CC}	X	I	**Power Supply:** +5V supply input.
GND	X	I	**Ground**

Quad UART for 3.3V and 5V supply voltage SC28L194

DESCRIPTION

The Philips 28L194 Quad UART is a single chip CMOS-LSI communications device that provides 4 full-duplex asynchronous channels with significantly deeper 16 byte FIFOs, Automatic in-band flow control using Xon/Xoff characters defined by the user and address recognition in the Wake-up mode. Synchronous bus interface is used for all communication between host and QUART. It is fabricated in Philips state of the art CMOS technology that combines the benefits of low cost, high density and low power consumption.

The operating speed of each receiver and transmitter can be selected independently from one of 22 fixed baud rates, a 16X clock derived from one of two programmable baud rate counters or one of three external 16X clocks (1 available at 1x clock rate). The baud rate generator and counter can operate directly from a crystal or from seven other external or internal clock inputs. The ability to independently program the operating speed of the receiver and transmitter makes the Quad UART particularly attractive for dual speed full duplex channel applications such as clustered terminal systems. The receivers and transmitters are buffered with FIFOs of 16 characters to minimize the potential for receiver overrun and to reduce interrupt overhead. In addition, a handshaking capability and in-band flow control are provided to disable a remote UART transmitter when the receiver buffer is full or nearly so.

To minimize interrupt overhead an interrupt arbitration system is included which reports the context of the interrupting UART via direct access or through the modification of the interrupt vector. The context of the interrupt is reported as channel number, type of device interrupting (receiver COS etc.) and, for transmitters or receivers, the fill level of the FIFO.

The Quad UART provides a power down mode in which the oscillator is stopped but the register contents are maintained. This results in reduced power consumption of several orders of magnitudes. The Quad UART is fully TTL compatible when operating from a single +5V or 3.3V power supply. Operation at 3.3V or 5.0V is maintained with CMOS interface levels.

Uses

- Statistical Multiplexers
- Data Concentrators
  - Packet-switching networks
  - Process Control
  - Building or Plant Control
  - Laboratory data gathering
  - ISDN front ends
  - Computer Networks
  - Point-of-Sale terminals
- Automotive, cab and engine controls
- Entertainment systems
  - MIDDI keyboard control music systems
  - Theater lighting control
- Terminal Servers
  - Computer-Printer/Plotter links

FEATURES

- Single 3.3V and 5.0V power supply
- Four Philips industry standard full duplex UART channels
- Sixteen byte receiver FIFOs for each UART
- Sixteen byte transmit FIFOs for each UART
- In band flow control using programmable Xon/Xoff characters
- Flow control using CTSN RTSN hardware handshaking
- Automatic address detection in multi-drop mode
- Three byte general purpose character recognition
- Fast data bus, 15 ns data bus release time, 125 ns bus cycle time
- Programmable interrupt priorities
- Automatic identification of highest priority interrupt pending
- Global interrupt and control registers ease setup and interrupt handling
- Vectored interrupts with programmable interrupt vector formats
  - Interrupt vector modified with channel number
  - Interrupt vector modified with channel number and channel type
  - Interrupt vector not modified
- IACKN and DACKN signal pins
- Watch dog timer for each receiver (64 receive clock counts)
- Programmable Data Formats:
  - 5 to 8 data bits plus parity
  - Odd, even force or no parity
  - 1, 1.5 or 2 stop bits
- Flexible baud rate selection for receivers and transmitters:
  - 22 fixed rates; 50 - 230.4K baud or 100 to 460.8K baud
  - Additional non-standard rates to 500K baud with internal generators
  - Two reload-counters provide additional programmable baud rate generation
  - External 1x or 16x clock inputs
  - Simplified baud rate selection
- 1 MHz 1x and 16x data rates full duplex all channels.
- Parity, framing and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal(full duplex)
  - Diagnostic modes
    automatic echo
    local loop back
    emote loop back
- Four I/O ports per UART for modem controls, clocks, RTSN, I/O, etc.
  - All I/O ports equipped with "Change of State Detectors"
- Two global inputs and two global outputs for general purpose I/O
- Power down mode
- On chip crystal oscillator, 2-8 MHz
- TTL input levels. Outputs switch between full V_{CC} and V_{SS}
- High speed CMOS technology
- 80-pin Low Profile Quad Flat Pack LQFP and 68-pin PLCC

ORDERING CODE

PACKAGES	V_{CC} = 3.3V ±10%	V_{CC} = 5V ±10%	DWG #
	Industrial -40°C to +85°C	Industrial -40°C to +85°C	
68-Pin Plastic Leaded Chip Carrier (PLCC)	SC28L194A1A	SC28L194A1A	SOT188-3
80-Pin Plastic Low Profile Quad Flat Pack (LQFP)	SC28L194A1BE	SC28L194A1BE	SOT315-1

PIN CONFIGURATIONS

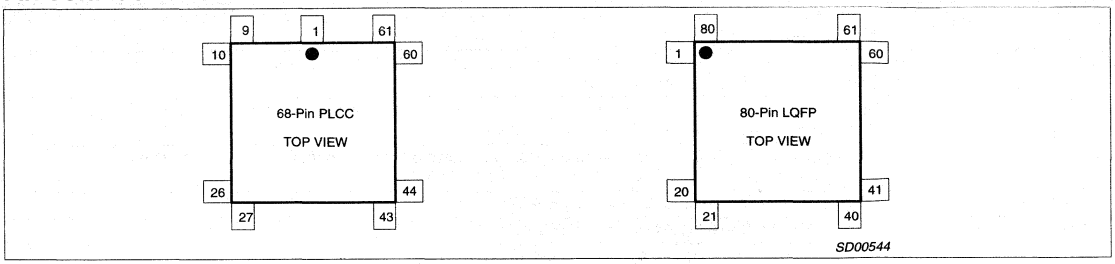


Figure 1. Pin Configurations

Pin Description

MNEMONIC	TYPE	DESCRIPTION
SClk	I	Host system clock. Used to time operations in the Host Interface and clock internal logic. Must be greater than twice the frequency of highest X1, Counter/Timer, TxC (1x) or RxC (1x) input frequency.
CEN	I	Chip select: Active low. When asserted, allows I/O access to QUART registers by host CPU. W_RN signal indicates direction. (**Must not be active in IACKN cycle**)
A(7:0)	I	Address lines (A[6] is **NOT** used. See "Host Interface")
D(7:0)	I/O	8-bit bi-directional data bus. Carries command and status information between 28L194 and the host CPU. Used to convey parallel data for serial I/O between the host CPU and the 28L194
W_RN	I	Write Read not control: When high indicates that the host CPU will write to a 28L194 register or transmit FIFO. When low, indicates a read cycle. 0 = Read; 1 = Write
DACKN	O	Data Acknowledge: Active low. When asserted, it signals that the last transfer of the D lines is complete. **Open drain requires a pull-up device.**
IRQN	O	Interrupt Request: Active low. When asserted, indicates that the 28L194 requires service for pending interrupt(s). **Open drain requires a pull-up device.**
IACKN	I	Interrupt Acknowledge: Active low. When asserted, indicates that the host CPU has initiated an interrupt acknowledge cycle. **(Do not use CEN in an IACKN cycle)**
TD(a-d)	O	Transmit Data: Serial outputs from the 4 UARTs.
RD(a-d)	I	Receive Data: Serial inputs to the 4 UARTs
I/O0(a-d)	I/O	Input/Output 0: Multi-use input or output pin for the UART.
I/O1(a-d)	I/O	Input/Output 1: Multi-use input or output pin for the UART.
I/O2(a-d)	I/O	Input/Output 2: Multi-use input or output pin for the UART.
I/O3(a-d)	I/O	Input/Output 3: Multi-use input or output pin for the UART.
Gin(1:0)	I	Global general purpose inputs, available to any/all channels.
Gout(1:0)	O	Global general purpose outputs, available from any channel.
RESETN	I	Master reset: Active Low. Must be asserted at power up and may be asserted at other times to reset and restart the system. **See "Reset Conditions" at end of register map.** Minimum width 10 SCLK.
X1/CCLK	I	Crystal 1 or Communication Clock: This pin may be connected to one side of a 2-8 MHz crystal. It may alternatively be driven by an external clock in this frequency range. Standard frequency = 3.6864 MHz
X2	O	Crystal 2: If a crystal is used, this is the connection to the second terminal. If a clock signal drives X1, this pin must be left unconnected.
Power Supplies	I	16 pins total 8 pins for Vss, 8 pins for Vcc

NOTE:

1. Many output pins will have very fast edges, especially when lightly loaded (less than 20 pf). These edges may move as fast as 1 to 3 ns fall or rise time. The user must be aware of the possible generation of ringing and reflections on improperly terminated interconnections. See previous note on Sclk noise under pin assignments.

BLOCK DIAGRAM

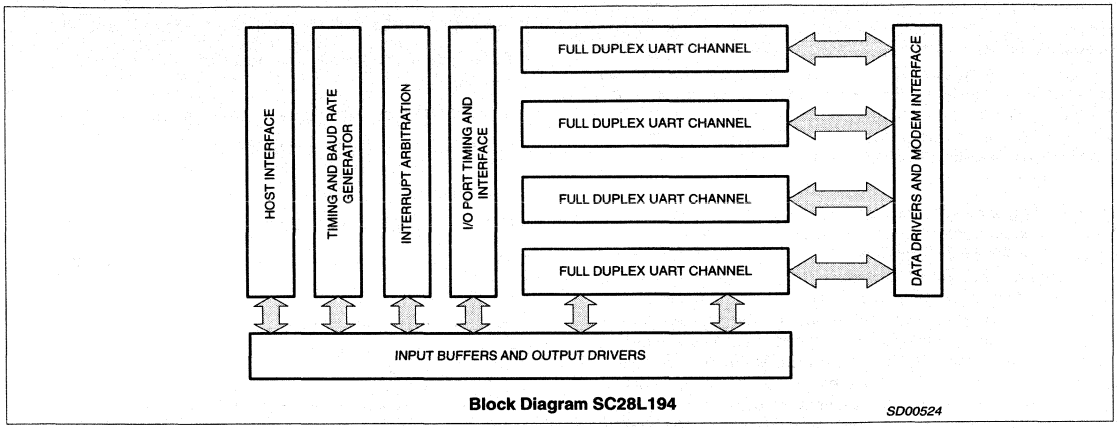


Figure 2. Block Diagram

Octal UART for 3.3V and 5V supply voltage SC28L198

DESCRIPTION

The Philips 28C198 Octal UART is a single chip CMOS–LSI communications device that provides 8 full-duplex asynchronous channels with significantly deeper 16 byte FIFOs, Automatic in–band flow control using Xon/Xoff characters defined by the user and address recognition in the wake up mode. Synchronous bus interface is used for all communication between host and OCTART. It is fabricated using Philips 1.0 micron CMOS technology that combines the benefits of low cost, high density and low power consumption.

The operating speed of each receiver and transmitter can be selected independently from one of 22 fixed baud rates, a 16X clock derived from one of two programmable baud rate counters or one of three external 16X clocks (1 available at 1x clock rate). The baud rate generator and counter can operate directly from a crystal or from seven other external or internal clock inputs. The ability to independently program the operating speed of the receiver and transmitter makes the Octal UART particularly attractive for dual speed full duplex channel applications such as clustered terminal systems. The receivers and transmitters are buffered with FIFOs of 16 characters to minimize the potential for receiver overrun and to reduce interrupt overhead. In addition, a handshaking capability and in–band flow control are provided to disable a remote UART transmitter when the receiver buffer is full or nearly so.

To minimize interrupt overhead an interrupt arbitration system is included which reports the context of the interrupting UART via direct access or through the modification of the interrupt vector. The context of the interrupt is reported as channel number, type of device interrupting (receiver COS etc.) and, for transmitters or receivers, the fill level of the FIFO.

The Octal UART provides a power down mode in which the oscillator is stopped but the register contents are maintained. This results in reduced power consumption of several orders of magnitudes. The Octal UART is fully TTL compatible when operating from a single +5V power supply. Operation at 3.3 volts is maintained with CMOS interface levels.

The device also offered in a version which maintains TTL input and output levels while operating with a 3.3 volt power supply.

FEATURES

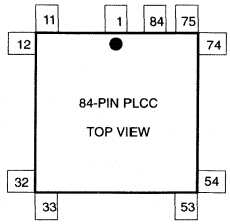
- Single 3.3V and 5V power supply
- Eight Philips industry standard full duplex UART channels
- Sixteen byte receiver FIFOs for each UART
- Sixteen byte transmit FIFOs for each UART
- In band flow control using programmable Xon/Xoff characters
- Flow control using CTSN RTSN hardware handshaking
- Automatic address detection in multi-drop mode
- Three byte general purpose character recognition
- Fast data bus, 30 ns data bus release time, 125 ns bus cycle time
- Programmable interrupt priorities
- Automatic identification of highest priority interrupt pending
- Global interrupt and control registers ease setup and interrupt handling
- Vectored interrupts with programmable interrupt vector formats
  - Interrupt vector modified with channel number
  - Interrupt vector modified with channel number and channel type
  - Interrupt vector not modified
- IACKN and DACKN signal pins
- Watch dog timer for each receiver (64 receive clock counts)
- Programmable Data Formats:
  - 5 to 8 data bits plus parity
  - Odd, even force or no parity
  - 1, 1.5 or 2 stop bits
- Flexible baud rate selection for receivers and transmitters:
  - 22 fixed rates; 50 – 230.4K baud or 100 to 460.8K baud
  - Additional non–standard rates to 500K baud with internal generators
  - Two reload–counters provide additional programmable baud rate generation
  - External 1x or 16x clock inputs
  - Simplified baud rate selection
- 1 MHz 1x and 16x data rates full duplex all channels.
- Parity, framing and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal(full duplex)
  - Diagnostic modes
    automatic echo
    local loop back
    emote loop back
- Four I/O ports per UART for modem controls, clocks, RTSN, I/O etc.
  - All I/O ports equipped with "Change of State Detectors"
- Two global inputs and two global outputs for general purpose I/O
- Power down mode
- On chip crystal oscillator, 2–8 MHz
- TTL input levels. Outputs switch between full V_{CC} and V_{SS}
- High speed CMOS technology
- 84 pin PLCC
- 100 pin LQFP

ORDERING CODE

PACKAGES	V_{CC} = 5V ±10% Industrial[1] -40°C to +85°C	DWG #
84-Pin Plastic Leaded Chip Carrier (PLCC)	SC28L198A1A	SOT189-3
100-Pin Plastic Low–Profile Quad Flat Pack (LQFP)	SC28L198A1BE	SOT407–1
	V_{CC} = 3.3V ±10% Industrial[1] -40°C to +85°C	
84-Pin Plastic Leaded Chip Carrier (PLCC)	SC28L198A1A	SOT189-3
100-Pin Plastic Low–Profile Quad Flat Pack (LQFP)	SC28L198A1BE	SOT407–1

NOTES:
1. For availability, please contact factory.

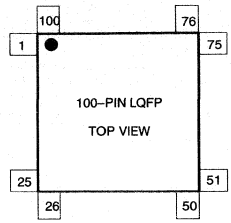
PIN CONFIGURATIONS



PINOUT

Pin	Function	Pin	Function	Pin	Function
1	V_{SS}	29	I/O1d	57	I/O2g
2	V_{CC}	30	I/O2d	58	I/O1g
3	CEN	31	I/O3d	59	I/O0g
4	W_RN	32	RxDd	60	RxDg
5	A2	33	Vss	61	TxDg
6	A1	34	TxDd	62	V_{SS}
7	A0	35	RESETN	63	X1
8	DACKN	36	Gin0	64	X2
9	I/O0a	37	Gout0	65	TxDf
10	I/O1a	38	D0	66	I/O3f
11	RxDa	39	D1	67	I/O2f
12	RxDb	40	D2	68	I/O1f
13	I/O2a	41	D3	69	I/O0f
14	I/O3a	42	V_{SS}	70	TxDe
15	TxDa	43	V_{CC}	71	I/O3e
16	I/O0b	44	D4	72	I/O2e
17	I/O1b	45	D5	73	I/O1e
18	I/O2b	46	D6	74	RxDf
19	I/O3b	47	D7	75	RxDe
20	TxDb	48	Gin1	76	I/O0e
21	I/O0c	49	I/O3h	77	IRQN
22	Vss	50	I/O2h	78	A7
23	I/O1c	51	I/O1h	79	A6
24	I/O2c	52	I/O0h	80	A5
25	I/O3c	53	Vss	81	A4
26	TxDc	54	RxDh	82	A3
27	RxDc	55	TxDh	83	IACKN
28	I/O0d	56	I/O3g	84	SCLK

PIN CONFIGURATIONS



PINOUT

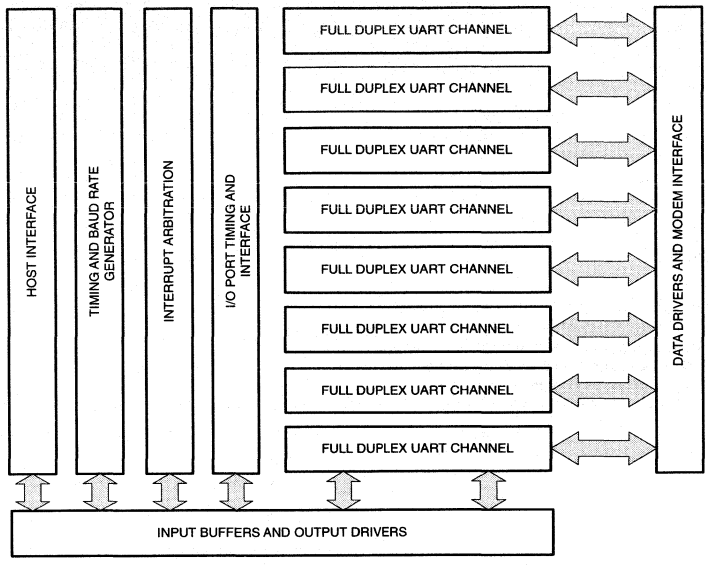
Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	N/C	26	V_{SS}	51	N/C	76	N/C
2	RxDb	27	TxDd	52	N/C	77	RxDe
3	I/02a	28	RESETN	53	RxDh	78	I/O0e
4	I/03a	29	$G_{IN}0$	54	TxDh	79	IRQN
5	TxDa	30	$G_{OUT}0$	55	I/O3g	80	A7
6	I/O0b	31	D0	56	I/O2g	81	A6
7	I/O1b	32	D1	57	I/O1g	82	A5
8	I/O2b	33	D2	58	I/O0g	83	A4
9	I/O3b	34	D3	59	RxDg	84	A3
10	TxDb	35	V_{SS}	60	TxDg	85	IACKN
11	I/O0c	36	V_{SS}	61	V_{SS}	86	Sclk
12	V_{SS}	37	V_{CC}	62	V_{SS}	87	V_{SS}
13	V_{SS}	38	V_{CC}	63	X1	88	V_{SS}
14	I/O1c	39	D4	64	X2	89	V_{CC}
15	I/O2c	40	D5	65	TxDf	90	V_{CC}
16	I/O3c	41	D6	66	I/O3f	91	CEN
17	TxDc	42	D7	67	I/O2f	92	W_RN
18	RxDc	43	$G_{IN}1$	68	I/O1f	93	A2
19	I/O0d	44	$G_{OUT}1$	69	I/O0f	94	A1
20	I/O1d	45	I/O3h	70	TxDe	95	JA0
21	I/O2d	46	I/O2h	71	I/O3e	96	DACKN
22	I/O3d	47	I/O1h	72	I/O2e	97	I/O0a
23	RxDd	48	I/O0h	73	I/O1e	98	I/O1a
24	N/C	49	V_{SS}	74	RxDf	99	RxDa
25	N/C	50	V_{SS}	75	N/C	100	N/C

Pin Description

MNEMONIC	TYPE	DESCRIPTION
SClk	I	Host system clock. Used to time operations in the Host Interface and clock internal logic. Must be greater than twice the frequency of highest X1, Counter/Timer, TxC (1x) or RxC (1x) input frequency.
CEN	I	Chip select: Active low. When asserted, allows I/O access to OCTART registers by host CPU. W_RN signal indicates direction. (**Must not be active in IACKN cycle**)
A(7:0)	I	Address lines (A[6] is **NOT** used. See "Host Interface")
D(7:0)	I/O	8–bit bi–directional data bus. Carries command and status information between 28C198 and the host CPU. Used to convey parallel data for serial I/O between the host CPU and the 28C198
W_RN	I	Write Read not control: When high indicates that the host CPU will write to a 28C198 register or transmit FIFO. When low, indicates a read cycle. 0 = Read; 1 = Write
DACKN	O	Data Acknowledge: Active low. When asserted, it signals that the last transfer of the D lines is complete. Open drain.
IRQN	O	Interrupt Request: Active low. When asserted, indicates that the 28C198 requires service for pending interrupt(s). Open drain.
IACKN	I	Interrupt Acknowledge: Active low. When asserted, indicates that the host CPU has initiated an interrupt acknowledge cycle. **(Do not use CEN in an IACKN cycle)**
TD(a–h)	O	Transmit Data: Serial outputs from the 8 UARTs.
RD(a–h)	I	Receive Data: Serial inputs to the 8 UARTs
I/O0(a–h)	I/O	Input/Output 0: Multi–use input or output pin for the UART.
I/O1(a–h)	I/O	Input/Output 1: Multi–use input or output pin for the UART.
I/O2(a–h)	I/O	Input/Output 2: Multi–use input or output pin for the UART.
I/O3(a–h)	I/O	Input/Output 3: Multi–use input or output pin for the UART.
$G_{IN}(1:0)$	I	Global general purpose inputs, available to any/all channels.
$G_{OUT}0$	O	Global general purpose outputs, available from any channel.
RESETN	I	Master reset: Active Low. Must be asserted at power up and may be asserted at other times to reset and restart the system. See "Reset Conditions" at end of register map. Minimum width 10 SCLK.
X1/CCLK	I	Crystal 1 or Communication Clock: This pin may be connected to one side of a 2–8 MHz crystal. It may alternatively be driven by an external clock in this frequency range. Standard frequency = 3.6864 MHz
X2	O	Crystal 2: If a crystal is used, this is the connection to the second terminal. If a clock signal drives X1, this pin must be left unconnected.
Power Supplies	I	8 pins total 6 pins for Vss, 2 pins for Vcc

NOTE: Many output pins will have very fast edges, especially when lightly loaded (less than 20 pf.) These edges may move as fast as 1 to 3 ns fall or rise time. The user must be aware of the possible generation of ringing and reflections on improperly terminated interconnections. See previous note on Sclk noise under pin assignments.

BLOCK DIAGRAM



Block Diagram SC28C/28L198 *SD00193*

Quad universal asynchronous receiver/transmitter (QUART) SC28C94

DESCRIPTION

The 28C94 quad universal asynchronous receiver/transmitter (QUART) combines four enhanced Philips Semiconductors industry-standard UARTs with an innovative interrupt scheme that can vastly minimize host processor overhead. It is implemented using Philips Semiconductors' high-speed CMOS process that combines small die size and cost with low power consumption.

The operating speed of each receiver and transmitter can be selected independently at one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the QUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is buffered with eight character FIFOs (first-in-first-out memories) and one shift register to minimize the potential for receiver overrun and to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full. (RTS control)

The 28C94 provides a power-down mode in which the oscillator is stopped and the register contents are stored. This results in reduced power consumption on the order of several magnitudes. The QUART is fully TTL compatible and operates from a single +5V power supply.

FEATURES

- New low overhead interrupt control
- All commercial parts meet industrial timing and temperature parameters
- Four Philips Semiconductors industry-standard UARTs
- Eight byte receive FIFO and eight byte transmit FIFO for each UART
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Baud rate for the receiver and transmitter selectable from:
  - 23 fixed rates: 50 to 230.4K baud Non-standard rates to 1.0M baud
  - User-defined rates from the programmable counter/timer associated with each of two blocks
  - External 1x or 16x clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation

PIN CONFIGURATIONS

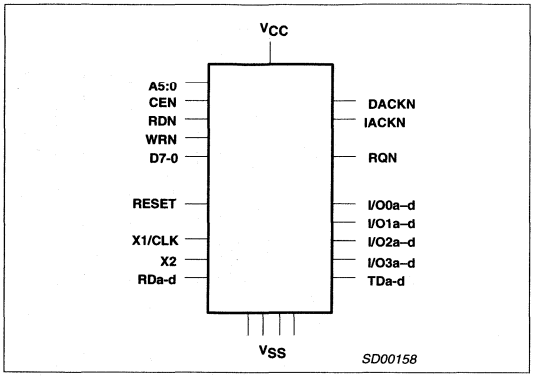


Figure 1. Pin Configuration

- Programmable channel mode
  - Normal (full-duplex), automatic echo, local loop back, remote loopback
- Programmable interrupt priorities
- Identification of highest priority interrupt
- Global interrupt register set provides data from interrupting channel
- Vectored interrupts with programmable vector format
- IACKN and programmable DTACKN signals
- Built-in baud rate generator with choice of 18 rates
- Four I/O pins per UART for modem controls, clocks, etc.
- Power down mode
- High-speed CMOS technology
- 52-pin PLCC and 48-pin DIP
- Commercial and industrial temperature ranges available
- On-chip crystal oscillator
- TTL compatible
- Single +5V power supply with low power mode
- Two multifunction programmable 16-bit counter/timers
- 1MHz 16x mode operation
- 10ns data bus release time
- "Watch Dog" timer for each receiver

ORDERING INFORMATION

PACKAGES	INDUSTRIAL V_{CC} = +5V ±10%, T_A = −40°C to +85°C	DWG #
48-Pin Plastic Dual In-Line Package (DIP)	SC28C94A1N	SOT240-1
52-Pin Plastic Leaded Chip Carrier (PLCC) Package	SC28C94A1A	SOT238-3

PIN CONFIGURATIONS

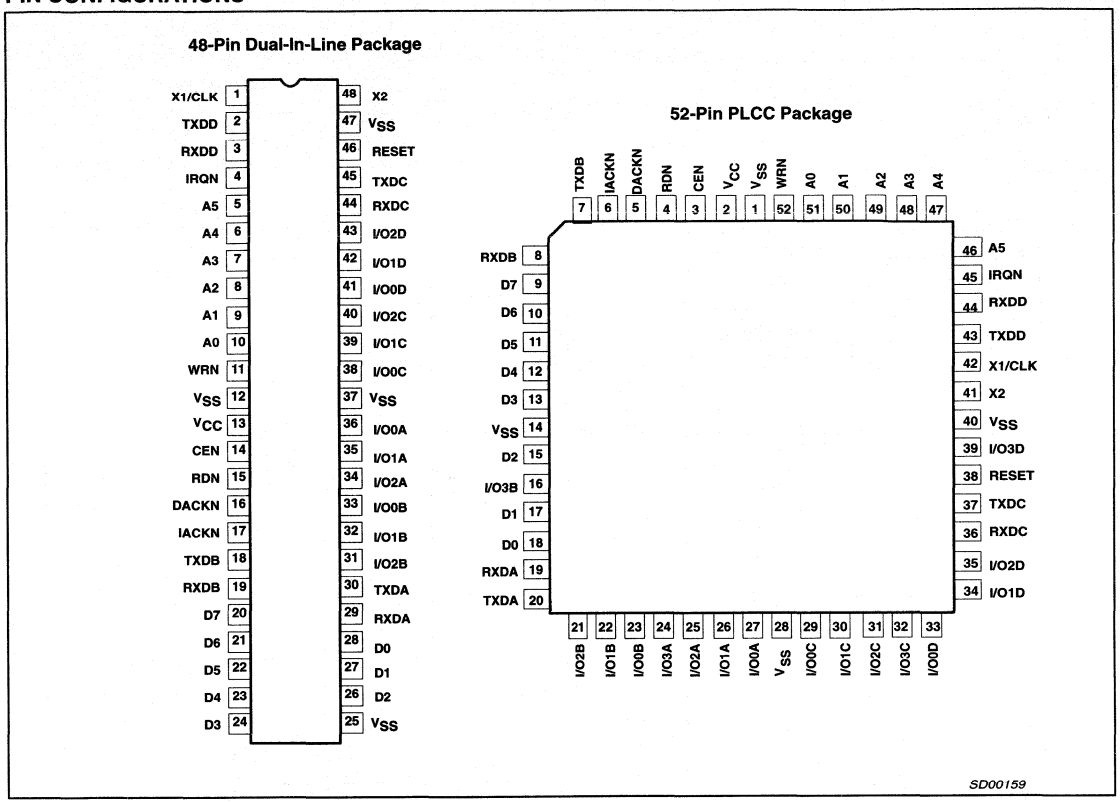


Figure 2. Pin Configurations (cont.)

BLOCK DIAGRAM

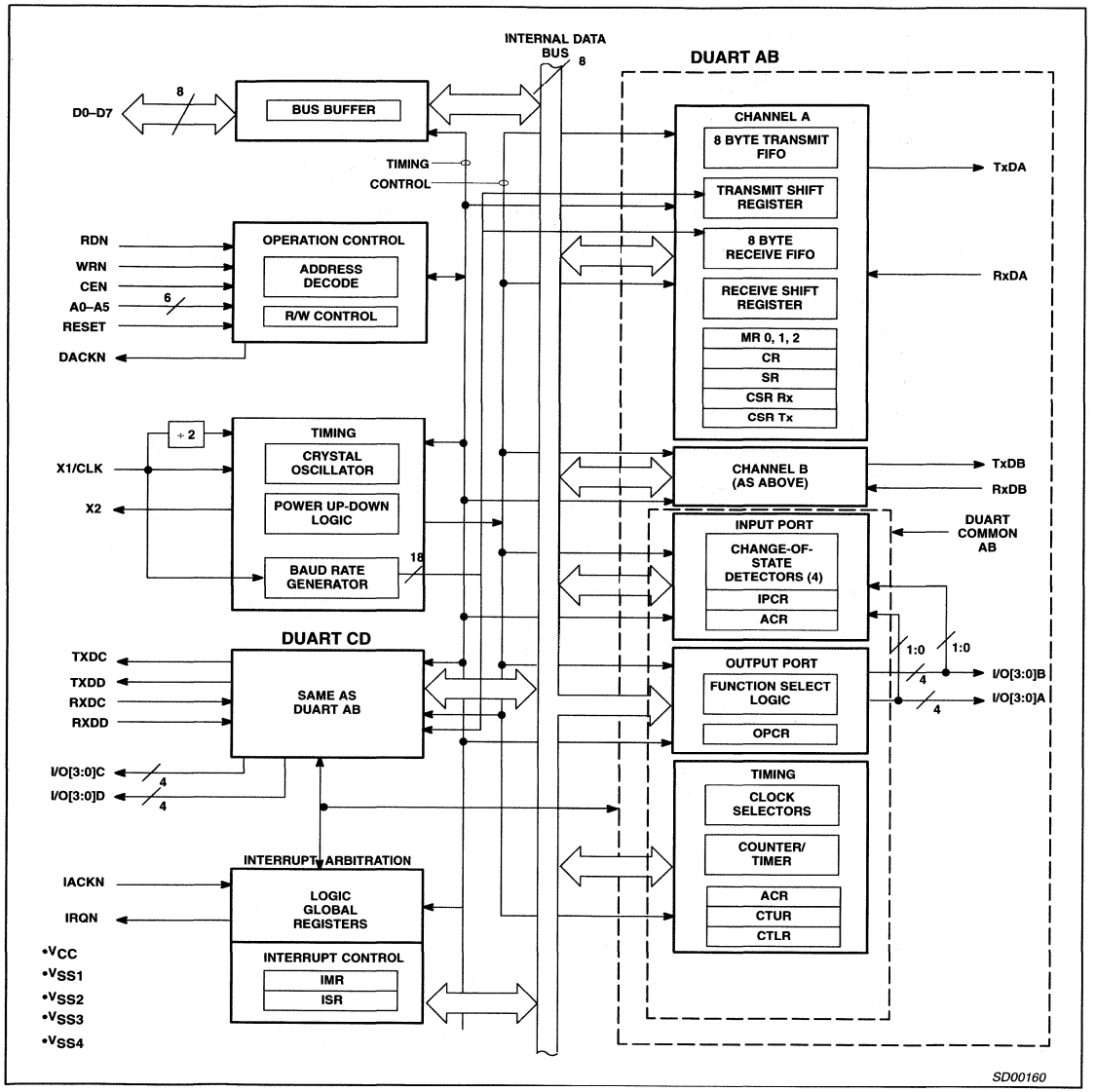


Figure 3. Block Diagram

PIN DESCRIPTION

MNEMONIC	TYPE	NAME AND FUNCTION
CEN	I	**Chip Select:** Active low input that, in conjunction with RDN or WRN, indicates that the host MPU is trying to access a QUART register. CEN must be inactive when IACKN is asserted.
A5:0	I	**Address Lines:** These inputs select a 28C94 register to be read or written by the host MPU.
D7:0	I/O	**8-bit Bidirectional Data Bus:** Used by the host MPU to read and write 28C94 registers.
RDN	I	**Read Strobe:** Active low input. When this line is asserted simultaneously with CEN, the 28C94 places the contents of the register selected by A5:0 on the D7:0 lines.
WRN	I	**Write Strobe:** Active low input. When this line is asserted simultaneously with CEN, the 28C94 writes the data on D7:0 into the register selected by A5:0.
DACKN	O	**Data ACKnowledge:** Active low, open-drain output to the host MPU, which is asserted subsequent to a read or write operation. For a read operation, assertion of DACKN indicates that register data is valid on D7:0. For a write operation, it indicates that the data on D7:0 has been captured into the indicated register. This signal corresponds to READYN on 80x86 processors and DTACKN on 680x0 processors.
IRQN	O	**Interrupt Request:** This active low open-drain output to the host MPU indicating that one or more of the enabled UART interrupt sources has reached an interrupt value which exceeds that pre-programmed by host software. The IRQN can be used directly as a 680x0 processor input; it must be inverted for use as an 80x86 interrupt input. This signal requires an external pull-up resistor.
IACKN	I	**Interrupt ACKnowledge:** Active low input indicates host MPU is acknowledging an interrupt requested. The 28C94 responds by placing an interrupt vector or interrupt vector modified on D7-D0 and asserting DACKN. This signal updates the CIR register in the interrupt logic. CEN must be high during this cycle.
TDa-d	O	**Transmit Data:** Serial outputs from the four UARTs.
RDa-d	I	**Receive Data:** Serial inputs to the four UARTs/
I/O0a-d	I/O	**Input/Output 0:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, Clear to Send inputs, 1X or 16X Transmit Clock outputs or general purpose outputs. Change-of-state detection is provided for these pins. I/O pins have approximately 1.5 Mohm pull–up device.
I/O1a-d	I/O	**Input/Output 1:** A multi-use input or output signal for each UART. These pins can be used as general purpose or 1X or 16X transmit clock inputs, or general purpose 1X or 16X receive clock outputs. Change-of-state detection is provided for these pins. In addition, I/O1a and I/O1c can be used as Counter/Timer inputs and I/O1b and I/O1d can be used as Counter/Timer outputs. I/O pins have approximately 1.5 Mohm pull–up device.
I/O2a-d	I/O	**Input/Output 2:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, 1X or 16X receive clock inputs, general purpose outputs, RTS output or 1X or 16X receive clock outputs. I/O pins have approximately 1.5 Mohm pull–up device.
I/O3a-d	I/O	**Input/Output 3:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, 1X or 16X transmit clock inputs, general purpose outputs, or 1X or 16X transmit clock outputs. I/O pins have approximately 1.5 Mohm pull–up device.
RESET	I	**Master Reset:** Active high reset for the 28C94 logic. Must be asserted at power-up, may be asserted at other times that the system is to be reset and restarted. OSC set to divide by 1, MR pointer set to 1, DACKN enabled, I/O pins to input. Registers reset: MR0, OPR, CIR. IRQN, DTACKN, IVR Interrupt Vector, Power Down, Test registers, FIFO pointers, Baud rate generator, Error Status, Watch Dog Timers, Change of State detectors, counter/timer to timer, Transmitter and Receiver controllers and all interrupt bits. If reset pin is not used, then first chip access should be to celar 'power-down' mode.
X1/CLK	I	**Crystal 1 or Communication Clock:** This pin is normally connected to one side of a 3.6864MHz or a 7.3728MHz crystal, or can be connected to an external clock up to 8MHz.
X2	O	**Crystal 2:** If a crystal is used, this pin should be connected to its other terminal. If an external clock is applied to X1, this pin should be left unconnected.
V_{CC}, V_{SS}		**Power and grounds:** respectively.

Dual universal asynchronous receiver/transmitter (DUART)

SC28L202

Designed for "Glueless operation in 68XXX and X86 environments"

DESCRIPTION

The 28L202 is a high performance functional upgrade for the Philips dual channel UARTS. The SCC2692 and SC26C92 operating at 3.3 or 5 volts supply with added features and deeper partitioned FIFOs. Its configuration on power up is similar that of the SC26C92. Its differences from the SC26C92 are: 256 character receiver, 256 character transmit FIFOs, CRC error detection, 3 and 5 volt compatibility, 8 I/O ports for each UART. IRDA compatibility, arbitrating interrupt system and overall faster buss and data speeds. It is fabricated in an advanced CMOS process that allows stand by current of less that one microampere.

Pin programming will allow the device to operate with either the Motorola or Intel bus interface by changing the function of some pins. (Reset is inverted, DACKN enabled for example).

The Philips Semiconductors 28L202 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS–LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of twenty-three fixed baud rates; a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver and transmitter is buffered by eight character FIFOs to minimize the potential of receiver overrun, transmitter underrun and to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote transmitter when the receiver buffer is full.

Also provided on the 28L202 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general-purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The 28L202 are available in two package versions: a 44-pin PLCC and 44-pin plastic quad flat pack (PQFP).

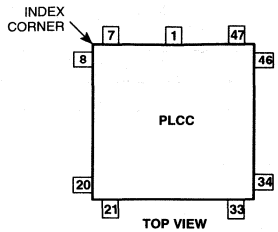
FEATURES

- 3.3 or 5.0 volt operation
- Dual full-duplex independent asynchronous receiver/transmitters
- 256 or larger character FIFOs for each receiver and transmitter
- Power up as 8 bit data no parity one stop bit 9600 baud
- Pin programming (PQFP package) to 68K or 80xxx bus interface
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- 16-bit programmable Counter/Timer
- Programmable baud rate for each receiver and transmitter selectable from:
  - 23 fixed rates: 50 to 230.4k baud
  - Other baud rates to MHz at 16X
  - Programmable user-defined rates derived from a programmable Counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loop back
  - Remote loop back
  - Multi-drop mode (also called 'wake-up' or '9-bit')
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on eight inputs
  - Inputs have typically >100k pull-up resistors
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate interrupt outputs that may be wire ORed.
  - Each FIFO can be programmed for four different interrupt levels.
  - Watch dog timer for each receiver
- Maximum data transfer rates:
  - 1X – 1Mb/sec, 16X – 1Mb/sec
- Automatic wake-up mode for multi-drop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver time-out mode
- Single +3.3V or +5V power supply
- Powers up to emulate SCC2692 and SC26C92

ORDERING INFORMATION

DESCRIPTION	INDUSTRIAL V_{CC} = +3.3 +5V ±10%, T_A = –40 TO +85°C	DRAWING NUMBER
44-Pin Plastic Leaded Chip Carrier (PLCC)	28L202A1A	SOT187–2
44-Pin Plastic Quad Flat Pack (PQFP)	28L202A1B	SOT307–2

PIN CONFIGURATION DIAGRAM

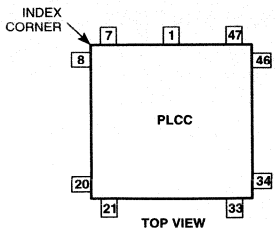


TOP VIEW

PIN	FUNCTION	PIN	FUNCTION
1	NC	27	D2
2	A0	28	D0
3	I/OB3	29	I/OA6
4	A1	30	I/OA4
5	I/OB1	31	I/OA2
6	A2	32	I/OA0
7	A3	33	TxDA
8	I/OB0	34	NC
9	WRN	35	RxDA
10	RDN	36	X1/CLK
11	RxDB	37	X2
12	I/M	38	RESET
13	TxDB	39	CEN
14	I/OA1	40	I/OB2
15	I/OA3	41	I/OB6
16	I/OA5	42	I/OB5
17	I/OA7	43	I/OB4
18	D1	44	V_{CC}
19	D3	45	A4
20	D5	46	A5
21	D7	47	I/OB7
22	V_{SS}	48	PRE
23	NC	49	V_{CC}
24	INTRN	50	V_{SS}
25	D6	51	NC
26	D4	52	NC

SD00680

PIN CONFIGURATION DIAGRAM



TOP VIEW

PIN	FUNCTION	PIN	FUNCTION
1	NC	27	D2
2	A0	28	D0
3	I/OB3	29	I/OA6
4	A1	30	I/OA4
5	I/OB1	31	I/OA2
6	A2	32	I/OA0
7	A3	33	TxDA
8	I/OB0	34	NC
9	R/WN	35	RxDA
10	DACKN	36	X1/CLK
11	RxDB	37	X2
12	I/M	38	RESETN
13	TxDB	39	CEN
14	I/OA1	40	I/OB2
15	I/OA3	41	IACKN
16	I/OA5	42	I/OB5
17	I/OA7	43	I/OB4
18	D1	44	V_{CC}
19	D3	45	A4
20	D5	46	A5
21	D7	47	I/OB7
22	V_{SS}	48	PRE
23	NC	49	V_{CC}
24	INTRN	50	V_{SS}
25	D6	51	NC
26	D4	52	NC

SD00681

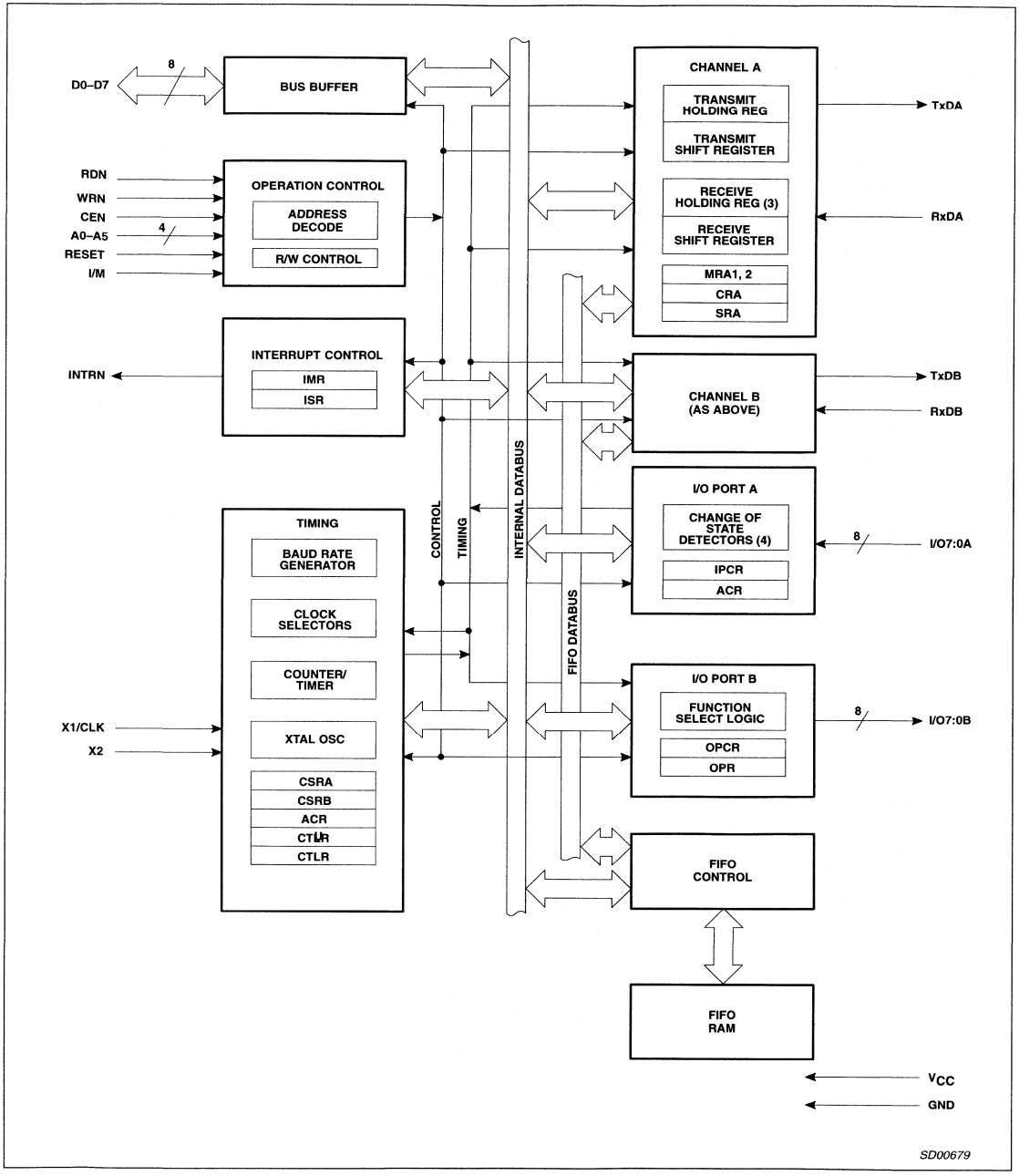


Figure 1. Block Diagram

PIN CONFIGURATION FOR 80XXX BUS INTERFACE (INTEL)

SYMBOL	PIN TYPE	NAME AND FUNCTION
I/M	I	**Bus Configuration**: When high or not connected configures the bus interface to the Conditions shown in this table.
D0–D7	I/O	**Data Bus**: Bi-directional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	I	**Chip Enable**: Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the WRN, RDN and A0–A3 inputs. When High, places the D0–D7 lines in the 3-State condition.
WRN	I	**Write Strobe**: When Low and CEN is also Low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	I	**Read Strobe**: When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0–A3	I	**Address Inputs**: Select the DUART internal registers and ports for read/write operations.
RESET	I	**Reset**: A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0 – OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Sets MR pointer to MR1.
INTRN	O	**Interrupt Request**: Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	I	**Crystal 1**: Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7).
X2	O	**Crystal 2**: Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If X1/CLK is driven from an external source, this pin must be left open.
RxDA	I	**Channel A Receiver Serial Data Input**: The least significant bit is received first. "Mark" is High; "space" is Low.
RxDB	I	**Channel B Receiver Serial Data Input**: The least significant bit is received first. "Mark" is High; "space" is Low.
TxDA	O	**Channel A Transmitter Serial Data Output**: The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loop back mode. "Mark" is High; "space" is Low.
TxDB	O	**Channel B Transmitter Serial Data Output**: The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loop back mode. 'Mark' is High; 'space' is Low.
I/O[7:0]A	O	**General-purpose input and output ports channel A**: The character of these pins is controlled by I/OPCR. They may be inputs or outputs and will present many internal clocks and interrupt signals: RTS, CTS, DTR, DSR etc. All have change of state detectors and the input is always active.
I/O[7:0}B	O	**General-purpose input and output ports channel B**: The character of these pins is controlled by I/OPCR. They may be inputs or outputs and will present many internal clocks and interrupt signals: RTS, CTS, DTR, DSR etc. All have change of state detectors and the input is always active.
V_{CC}	Pwr	**Power Supply**: +3.3 or +5V supply input 10%
GND	Pwr	**Ground**

PIN CONFIGURATION FOR 68XXX BUS INTERFACE (INTEL)

SYMBOL	PIN TYPE	NAME AND FUNCTION
I/M	I	**Bus Configuration**: When low configures the bus interface to the Conditions shown in this table.
D0–D7	I/O	**Data Bus**: Bi-directional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CSN	I	**Chip Enable**: Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the R/WN and A0–A3 inputs. When High, places the D0–D7 lines in the 3-State condition.
R/WN	I	**Read/Write**: Input Signal. When CSN is low R/WN high input a read cycle, when low a write cycle.
IACKN	I	**Interrupt Acknowledge**: Active low input indicates an interrupt acknowledge cycle. Usually asserted by the CPU in response to an interrupt request. When asserted places the interrupt vector on the bus and asserts DACKN.
DACKN	O	**Data Transfer Acknowledge**: A3–State active –low output asserted in a write, read, or interrupt acknowledge cycle to indicate proper transfer of data between the CPU and the DUART.
A0–A3	I	**Address Inputs**: Select the DUART internal registers and ports for read/write operations.
RESETN	I	**Reset**: A low level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Sets MR pointer to MR1.
INTRN	O	**Interrupt Request**: Active–Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	I	**Crystal 1**: Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7).
X2	O	**Crystal 2**: Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If X1/CLK is driven from an external source, this pin must be left open.
RxDA	I	**Channel A Receiver Serial Data Input**: The least significant bit is received first. "Mark" is High; "space" is Low.
RxDB	I	**Channel B Receiver Serial Data Input**: The least significant bit is received first. "Mark" is High; "space" is Low.
TxDA	O	**Channel A Transmitter Serial Data Output**: The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loop back mode. "Mark" is High; "space" is Low.
TxDB	O	**Channel B Transmitter Serial Data Output**: The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loop back mode. 'Mark' is High; 'space' is Low.
I/O[7:0]A	I/O	**General-purpose input and output ports channel A**: The character of these pins is controlled by I/OPCR. They may be inputs or outputs and will present many internal clocks and interrupt signals: RTS, CTS, DTR, DSR etc. All have change of state detectors and the input is always active.
I/O[7:0]B	I/O	**General-purpose input and output ports channel B**: The character of these pins is controlled by I/OPCR. They may be inputs or outputs and will present many internal clocks and interrupt signals: RTS, CTS, DTR, DSR etc. All have change of state detectors and the input is always active.
V_{CC}	Power	**Power Supply**: +3.3 or +5V supply input 10%
V_{SS}	Power	**Ground**

Dual Universal Asynchronous Receiver/Transmitter (DUART)

SC28L92

DESCRIPTION

The SC28L92 is a pin and function replacement for the SCC2692 and SC26C92 operating at 3.3 or 5 volts supply with added features and deeper FIFOs. Its configuration on power up is that of the 2692. Its differences from the 2692 are: 16 character receiver, 16 character transmit FIFOs, watch dog timer for each receiver, mode register 0 is added, extended baud rate and overall faster speeds, programmable receiver and transmitter interrupts. (Neither the SC26C92 nor The SCC2692 is being discontinued.)

Pin programming will allow the device to operate with either the Motorola or Intel bus interface The bit 3 of the MR0a register allows the device to operate in an 8 byte FIFO mode if strict compliance with the SC26C92 FIFO structure is required

The Philips Semiconductors SC28L92 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates; a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver and transmitter is buffered by 8 or 16 character FIFOs to minimize the potential of receiver overrun, transmitter underpin and to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote transmitter when the receiver buffer is full.

Also provided on the SC28L92 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SC28L92 is available in two package versions: a 44-pin PLCC and 44-pin plastic quad flat pack (PQFP).

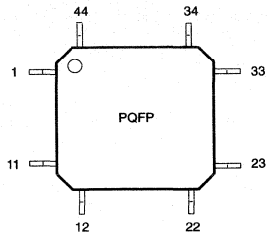
FEATURES

- 3.3 or 5.0 volt operation
- Dual full-duplex independent asynchronous receiver/transmitters
- 16 character FIFOs for each receiver and transmitter
- Pin programming for 68K or 80xxx bus interface
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- 16-bit programmable Counter/Timer
- Programmable baud rate for each receiver and transmitter selectable from:
  - 23 fixed rates: 50 to 230.4k baud
  - Other baud rates to MHz at 16X
  - Programmable user-defined rates derived from a programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loop back
  - Remote loop back
  - Multi-drop mode (also called 'wake-up' or '9-bit')
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - Inputs have typically >100k pull-up resistors
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate interrupt outputs that may be wire ORed.
  - Each FIFO can be programmed for four different interrupt levels
  - Watch dog timer for each receiver
- Maximum data transfer rates:
  1X – 1Mb/sec, 16X – 1Mb/sec
- Automatic wake-up mode for multi-drop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver time-out mode
- Single +3.3V or +5V power supply
- Powers up to emulate SCC2692 and S26C92

ORDERING INFORMATION

DESCRIPTION	INDUSTRIAL V_{CC} = +3.3 +5V ±10%, T_A = –40 to +85°C	DRAWING NUMBER
44-Pin Plastic Leaded Chip Carrier (PLCC)	SC28L92A1A	SOT187–2
44-Pin Plastic Quad Flat Pack (PQFP)	SC28L92A1B	SOT307-2

PIN CONFIGURATION DIAGRAM
80XXX PIN CONFIGURATION



Pin	Function	Pin	Function	Pin	Function
1	A3	16	GND	31	x2
2	IP0	17	GND	32	RESET
3	WRN	18	INTRN	33	CEN
4	RDN	19	D6	34	IP2
5	RxDB	20	D4	35	IP6
6	TxDB	21	D2	36	IP5
7	OP1	22	D0	37	IP4
8	OP3	23	NC	38	V_{CC}
9	OP5	24	OP6	39	V_{CC}
10	OP7	25	OP4	40	A0
11	I/M	26	OP2	41	IP3
12	D1	27	OP0	42	A1
13	D3	28	TxDA	43	IP1
14	D5	29	RxDA	44	A2
15	D7	30	x1/clk		

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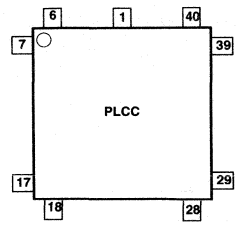

Pin	Function	Pin	Function	Pin	Function
1	NC	16	OP5	31	OP2
2	A0	17	OP7	32	OP0
3	IP3	18	D1	33	TxDA
4	A1	19	D3	34	NC
5	IP1	20	D5	35	RxDA
6	A2	21	D7	36	X1/CLK
7	A3	22	V_{SS}	37	X2
8	IP0	23	NC	38	RESET
9	WRN	24	INTRN	39	CEN
10	RDN	25	D6	40	IP2
11	RxDB	26	D4	41	IP6
12	I/M	27	D2	42	IP5
13	TxDB	28	D0	43	IP4
14	OP1	29	OP6	44	V_{CC}
15	OP3	30	OP4		

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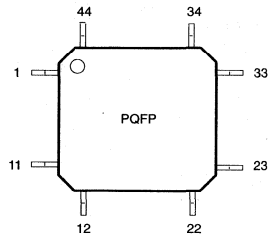
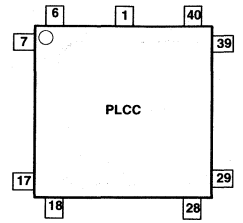
PIN CONFIGURATION DIAGRAM

68XXX PIN CONFIGURATION



Pin	Function	Pin	Function	Pin	Function
1	A3	16	GND	31	x2
2	IP0	17	GND	32	RESETN
3	R/WN	18	INTRN	33	CSN
4	DACKN	19	D6	34	IP2
5	RxDB	20	D4	35	IACKN
6	TxDB	21	D2	36	IP5
7	OP1	22	D0	37	IP4
8	OP3	23	NC	38	V_{CC}
9	OP5	24	OP6	39	V_{CC}
10	OP7	25	OP4	40	A0
11	I/M	26	OP2	41	IP3
12	D1	27	OP0	42	A1
13	D3	28	TxDA	43	IP1
14	D5	29	RxDA	44	A2
15	D7	30	x1/clk		

SD00673



Pin	Function	Pin	Function	Pin	Function
1	NC	16	OP5	31	OP2
2	A0	17	OP7	32	OP0
3	IP3	18	D1	33	TxDA
4	A1	19	D3	34	NC
5	IP1	20	D5	35	RxDA
6	A2	21	D7	36	X1/CLK
7	A3	22	V_{SS}	37	X2
8	IP0	23	NC	38	RESETN
9	R/WN	24	INTRN	39	CEN
10	DACKN	25	D6	40	IP2
11	RxDB	26	D4	41	IACKN
12	I/M	27	D2	42	IP5
13	TxDB	28	D0	43	IP4
14	OP1	29	OP6	44	V_{CC}
15	OP3	30	OP4		

SD00674

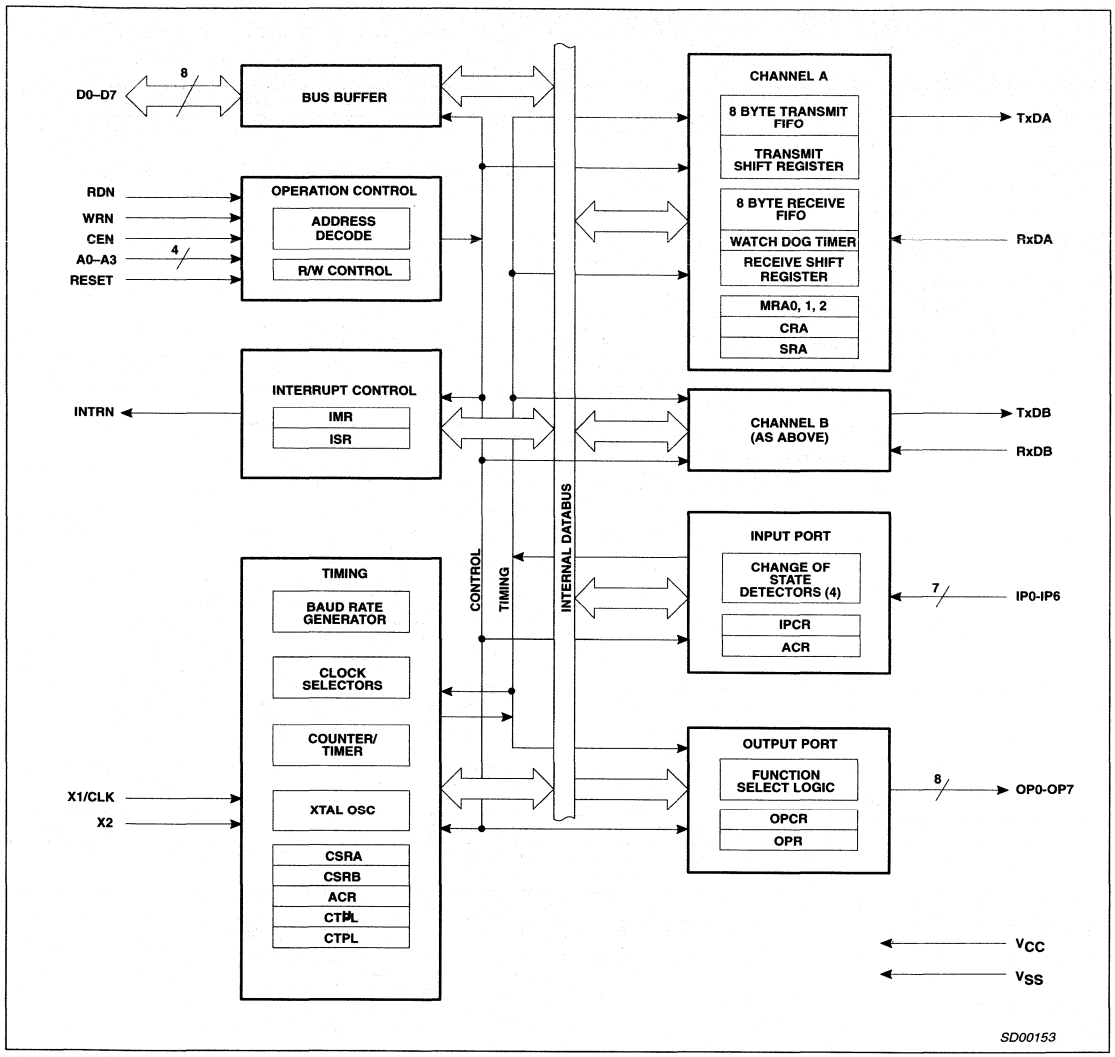


Figure 1. Block Diagram

PIN CONFIGURATION FOR 80XXX BUS INTERFACE (INTEL®)

SYMBOL	PIN TYPE	NAME AND FUNCTION
I/M	I	**Bus Configuration**: When high or not connected configures the bus interface to the Conditions shown in this table.
D0–D7	I/O	**Data Bus**: Bi-directional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	I	**Chip Enable**: Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the WRN, RDN and A0–A3 inputs. When High, places the D0–D7 lines in the 3-State condition.
WRN	I	**Write Strobe**: When Low and CEN is also Low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	I	**Read Strobe**: When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0–A3	I	**Address Inputs**: Select the DUART internal registers and ports for read/write operations.
RESET	I	**Reset**: A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Sets MR pointer to MR1.
INTRN	O	**Interrupt Request**: Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	I	**Crystal 1**: Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7).
X2	O	**Crystal 2**: Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If X1/CLK is driven from an external source, this pin must be left open.
RxDA	I	**Channel A Receiver Serial Data Input**: The least significant bit is received first. "Mark" is High; "space" is Low.
RxDB	I	**Channel B Receiver Serial Data Input**: The least significant bit is received first. "Mark" is High; "space" is Low.
TxDA	O	**Channel A Transmitter Serial Data Output**: The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loop back mode. "Mark" is High; "space" is Low.
TxDB	O	**Channel B Transmitter Serial Data Output**: The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loop back mode. 'Mark' is High; 'space' is Low.
OP0	O	**Output 0**: General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	O	**Output 1**: General-purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	O	**Output 2**: General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	O	**Output 3**: General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	O	**Output 4**: General purpose output or Channel A open-drain, active-Low, RxA interrupt ISR[1] output.
OP5	O	**Output 5**: General-purpose output or Channel B open-drain, active-Low, RxB interrupt ISR[5] output.
OP6	O	**Output 6**: General purpose output or Channel A open-drain, active-Low, TxA interrupt ISR[0] output.
OP7	O	**Output 7**: General-purpose output, or Channel B open-drain, active-Low, TxB interrupt ISR[4] output.
IP0	I	**Input 0**: General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	I	**Input 1**: General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	I	**Input 2**: General-purpose input or counter/timer external clock input.
IP3	I	**Input 3**: General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	I	**Input 4**: General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	I	**Input 5**: General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	I	**Input 6**: General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	Pwr	**Power Supply**: +3.3 or +5V supply input ±10%
GND	Pwr	**Ground**

PIN CONFIGURATION FOR 68XXX BUS INTERFACE (MOTOROLA®)

SYMBOL	PIN TYPE	NAME AND FUNCTION
I/M	I	**Bus Configuration**: When low configures the bus interface to the Conditions shown in this table.
D0–D7	I/O	**Data Bus**: Bi-directional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CSN	I	**Chip Enable**: Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the R/WN and A0–A3 inputs. When High, places the D0–D7 lines in the 3-State condition.
R/WN	I	**Read/Write**: Input Signal. When CSN is low R/WN high input indicates a read cycle; when low indicates a write cycle.
IACKN	I	**Interrupt Acknowledge**: Active low input indicating an interrupt acknowledge cycle. Usually asserted by the CPU in response to an interrupt request. When asserted places the interrupt vector on the bus and asserts DACKN.
DACKN	O	**Data Transfer Acknowledge**: A3-State active -low output asserted in a write, read, or interrupt acknowledge cycle to indicate proper transfer of data between the CPU and the DUART.
A0–A3	I	**Address Inputs**: Select the DUART internal registers and ports for read/write operations.
RESETN	I	**Reset**: A low level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Sets MR pointer to MR1.
INTRN	O	**Interrupt Request**: Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	I	**Crystal 1**: Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7).
X2	O	**Crystal 2**: Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If X1/CLK is driven from an external source, this pin must be left open.
RxDA	I	**Channel A Receiver Serial Data Input**: The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	I	**Channel B Receiver Serial Data Input**: The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	O	**Channel A Transmitter Serial Data Output**: The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loop back mode. "Mark" is High; "space" is Low.
TxDB	O	**Channel B Transmitter Serial Data Output**: The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loop back mode. 'Mark' is High; 'space' is Low.
OP0	O	**Output 0**: General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	O	**Output 1**: General-purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	O	**Output 2**: General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	O	**Output 3**: General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	O	**Output 4**: General purpose output or Channel A open-drain, active-Low, RxA interrupt ISR [1] output.
OP5	O	**Output 5**: General-purpose output or Channel B open-drain, active-Low, RxB interrupt ISR[5] output.
OP6	O	**Output 6**: General purpose output or Channel A open-drain, active-Low, TxA interrupt ISR[0] output.
OP7	O	**Output 7**: General-purpose output, or Channel B open-drain, active-Low, TxB interrupt ISR[4] output.
IP0	I	**Input 0**: General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	I	**Input 1**: General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	I	**Input 2**: General-purpose input or counter/timer external clock input.
IP3	I	**Input 3**: General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	I	**Input 4**: General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	I	**Input 5**: General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
V_{CC}	Pwr	**Power Supply**: +3.3 or +5V supply input ±10%
GND	Pwr	**Ground**

Universal asynchronous receiver/transmitter (UART) SCC2691

DESCRIPTION

The Philips Semiconductors SCC2691 Universal Asynchronous Receiver/Transmitter (UART) is a single-chip CMOS-LSI communications device that provides a full-duplex asynchronous receiver/transmitter. It is fabricated with Philips Semiconductors CMOS technology which combines the benefits of high density and low power consumption.

The operating speed of the receiver and transmitter can be selected independently as one of 18 fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the UART particularly attractive for dual-speed channel applications such as clustered terminal systems.

The receiver is quadruple buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full.

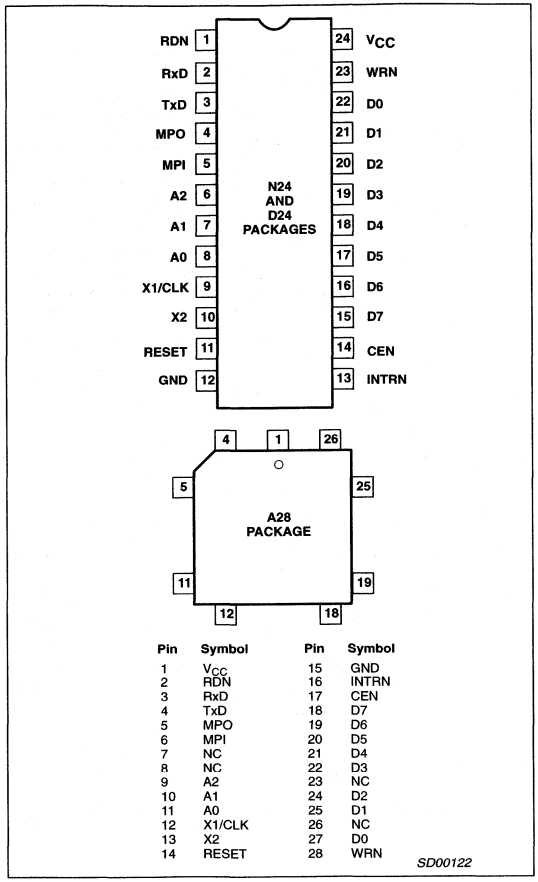
The UART provides a power-down mode in which the oscillator is frozen but the register contents are stored. This results in reduced power consumption on the order of several magnitudes.

The UART is fully TTL compatible and operates from a single +5V power supply.

FEATURES

- Full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data register
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- 16-bit programmable Counter/Timer
- Baud rate for the receiver and transmitter selectable from:
  - 22 fixed rates: 50 to 115.2K baud
  - Non-standard rates to 115.2kb
  - Non-standard user-defined rate derived from programmable timer/ counter
  - External 1X or 16X clock
- Parity, framing, and overrun detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote Loopback
- Multi-function programmable 16-bit counter/timer

PIN CONFIGURATIONS



Pin	Symbol	Pin	Symbol
1	V_{CC}	15	GND
2	RDN	16	INTRN
3	RxD	17	CEN
4	TxD	18	D7
5	MPO	19	D6
6	MPI	20	D5
7	NC	21	D4
8	NC	22	D3
9	A2	23	NC
10	A1	24	D2
11	A0	25	D1
12	X1/CLK	26	NC
13	X2	27	D0
14	RESET	28	WRN

Figure 1. Pin Configurations

- Single interrupt output with seven maskable interrupting conditions
- On-chip crystal oscillator
- Low power mode
- TTL compatible
- Single +5V power supply
- Commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature versions available
- SOL, PLCC and 300 mil wide DIP packages available

ORDERING INFORMATION

PACKAGES	COMMERCIAL V_{CC} = +5V ±10%, T_A = 0°C to +70°C	INDUSTRIAL V_{CC} = +5V ±10%, T_A = –40°C to +85°C	DWG #
24-Pin Plastic Dual In-Line Package (DIP)	SCC2691AC1N24	SCC2691AE1N24	SOT222–1
28-Pin Plastic Leaded Chip Carrier (PLCC) Package	SCC2691AC1A28	SCC2691AE1A28	SOT261-3
24-Pin Plastic Small Outline Large (SOL) Package	SCC2691AC1D24		SOT137-1

BLOCK DIAGRAM

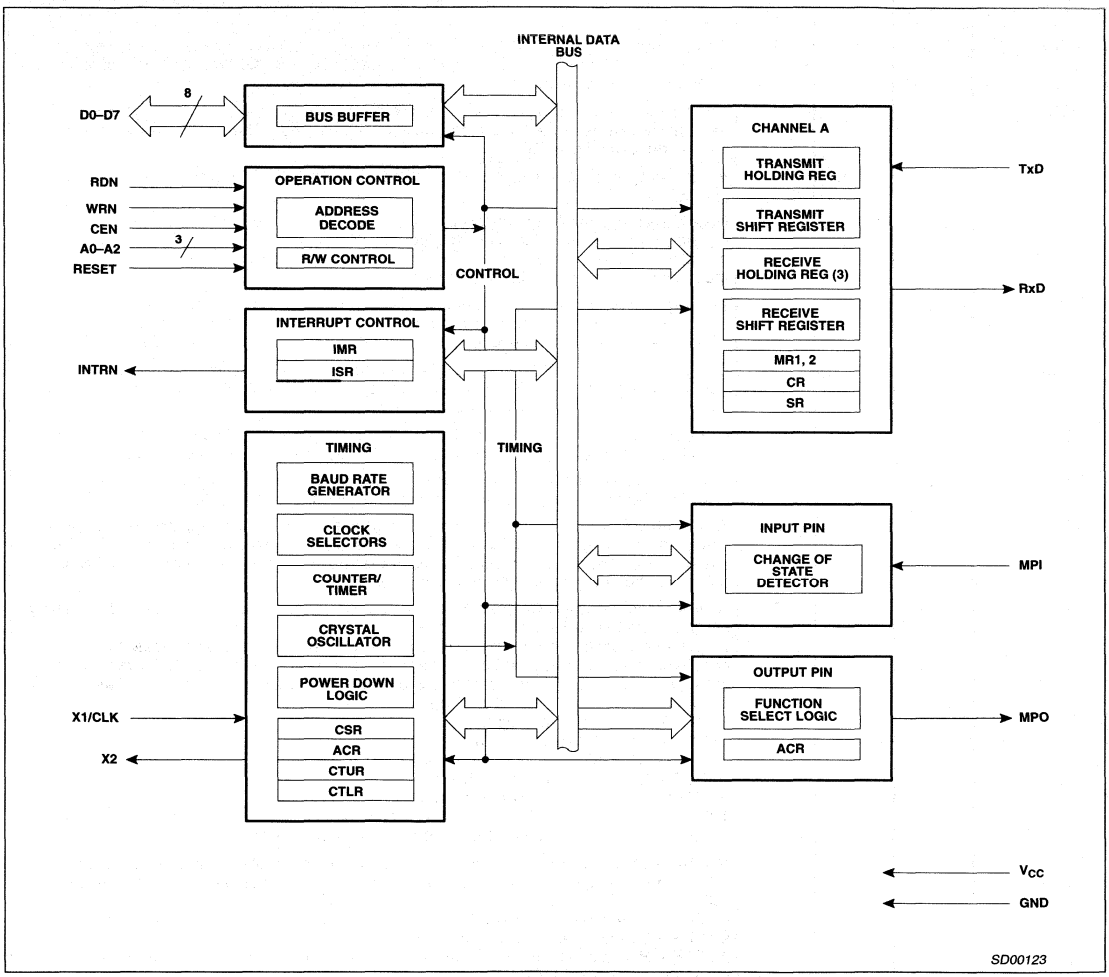


Figure 2. Block Diagram

PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
D0–D7	22–15	27, 25, 24, 22–18	I	**Data Bus:** Active-high 8-bit bidirectional 3-State data bus. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the UART take place over this bus. The direction of the transfer is controlled by the WRN and RDN inputs when the CEN input is low. When the CEN input is high, the data bus is in the 3-State condition.
CEN	14	17	I	**Chip Enable:** Active-low input. When low, data transfers between the CPU and the UART are enabled on D0–D7 as controlled by the WRN, RDN and A0–A2 inputs. When CEN is high, the UART is effectively isolated from the data bus and D0–D7 are placed in the 3-State condition.
WRN	23	28	I	**Write Strobe:** Active-low input. A low on this pin while CEN is low causes the contents of the data bus to be transferred to the register selected by A0–A2. The transfer occurs on the trailing (rising) edge of the signal.
RDN	1	2	I	**Read Strobe:** Active-low input. A low on this pin while CEN is low causes the contents of the register selected by A0–A2 to be placed on the data bus. The read cycle begins on the leading (falling) edge of RDN.
A0–A2	8–6	11–9	I	**Address Inputs:** Active-high address inputs to select the UART registers for read/write operations.
RESET	11	14	I	**Reset:** Master reset. A high on this pin clears the status register (SR), the interrupt mask register (IMR), and the interrupt status register (ISR), sets the mode register pointer to MR1, and places the receiver and transmitter in the inactive state causing the TxD output to go to the marking (high) state. Clears Test modes.
INTRN	13	16	O	**Interrupt Request:** This active-low output is asserted upon occurrence of one or more of seven maskable interrupting conditions. The CPU can read the interrupt status register to determine the interrupting condition(s). This open-drain output requires a pull-up resistor.
X1/CLK	9	12	I	**Crystal 1:** Crystal connection or an external clock input. A crystal of a clock the appropriate frequency (nominally 3.6864 MHz) must be supplied at all times. For crystal connections see Figure 7 (included in CD-ROM version), Clock Timing.
X2	10	13	I	**Crystal 2:** Crystal connection. See Figure 7 (included in CD-ROM version). If a crystal is not used it is best to keep this pin not connected although it is permissible to ground it.
RxD	2	3	I	**Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified, this input is sampled on the rising edge of the clock.
TxD	3	4	O	**Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the marking (high) condition when the transmitter is idle or disabled and when the UART is operating in local loopback mode. If external transmitter is specified, the data is shifted on the falling edge of the transmitter clock.
MPO	4	5	O	**Multi-Purpose Output:** One of the following functions can be selected for this output pin by programming the auxiliary control register: **RTSN** – Request to send active-low output. This output is asserted and negated via the command register. By appropriate programming of the mode registers, RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted or when the receiver FIFO and shift register are full. **C/TO** – The counter/timer output. **TxC1X** – The 1X clock for the transmitter. **TxC16X** – The 16X clock for the transmitter. **RxC1X** – The 1X clock for the receiver. **RxC16X** – The 16X clock for the receiver. **TxRDY** – The transmitter holding register empty signal. Active-low output. (Open drain) **RxRDY/FFULL** – The receiver FIFO not empty/full signal. Active-low output. (Open drain)
MPI	5	6	I	**Multi-Purpose Input:** This pin can serve as an input for one of the following functions: **GPI** – General purpose input. The current state of the pin can be determined by reading the ISR. **CTSN** – Clear-to-send active-low input. **CTCLK** – Counter/timer external clock input. **RTCLK** – Receiver and/or transmitter external clock input. This may be a 1X or 16X clock as programmed by CSR[3:0] or CSR[7:4]. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
V_{CC}	24	1	I	**Power Supply:** +5V supply input.
GND	12	15	I	**Ground**

Dual asynchronous receiver/transmitter (DUART) SCC2692

DESCRIPTION

The Philips Semiconductors SCC2692 Dual Universal Asynchronous Receiver/Transmitter (DUART) which is compatible with the SCN2681. It is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the receiver buffer is full.

Also provided on the SCC2692 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

FEATURES

- Dual full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data register
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- 16-bit programmable Counter/Timer
- Programmable baud rate for each receiver and transmitter selectable from:
  - 22 fixed rates: 50 to 115.2k baud
  - Non-standard rates to 115.2Kb
  - Non-standard user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
  - Multidrop mode (also called 'wake-up' or '9-bit')
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - Inputs have typically >100k pull-up resistors
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates: 1X – 1MB/sec, 16X – 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver timeout mode
- Commercial and industrial temperature range versions
- TTL compatible
- Single +5V power supply

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL	INDUSTRIAL	DWG #
	V_{CC} = +5V ±10%, T_A = 0 to +70°C	V_{CC} = +5V ±10%, T_A = -40 to +85°C	
40-Pin Plastic Dual In-Line Package (DIP)[1]	SCC2692AC1N40	SCC2692AE1N40	SOT129-1
28-Pin Plastic Dual In-Line Package (DIP)[1]	SCC2692AC1N28	SCC2692AE1N28	SOT117-1
44-Pin Plastic Leaded Chip Carrier (PLCC) Package	SCC2692AC1A44	SCC2692AE1A44	SOT187-2
44–Pin Plastic Quad Flat Pack (PQFP)	SCC2692AC1B44	SCC2692AE1B44	SOT307–2

NOTE:
1. For availability, please contact factory.

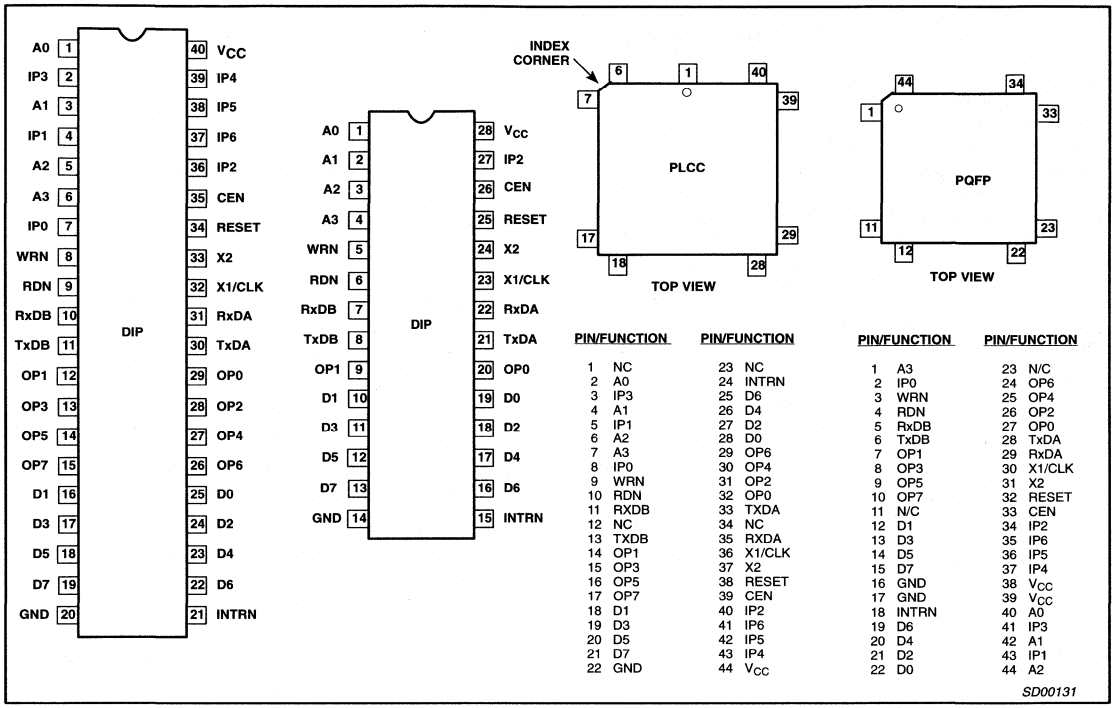


Figure 1. Pin Configurations

BLOCK DIAGRAM

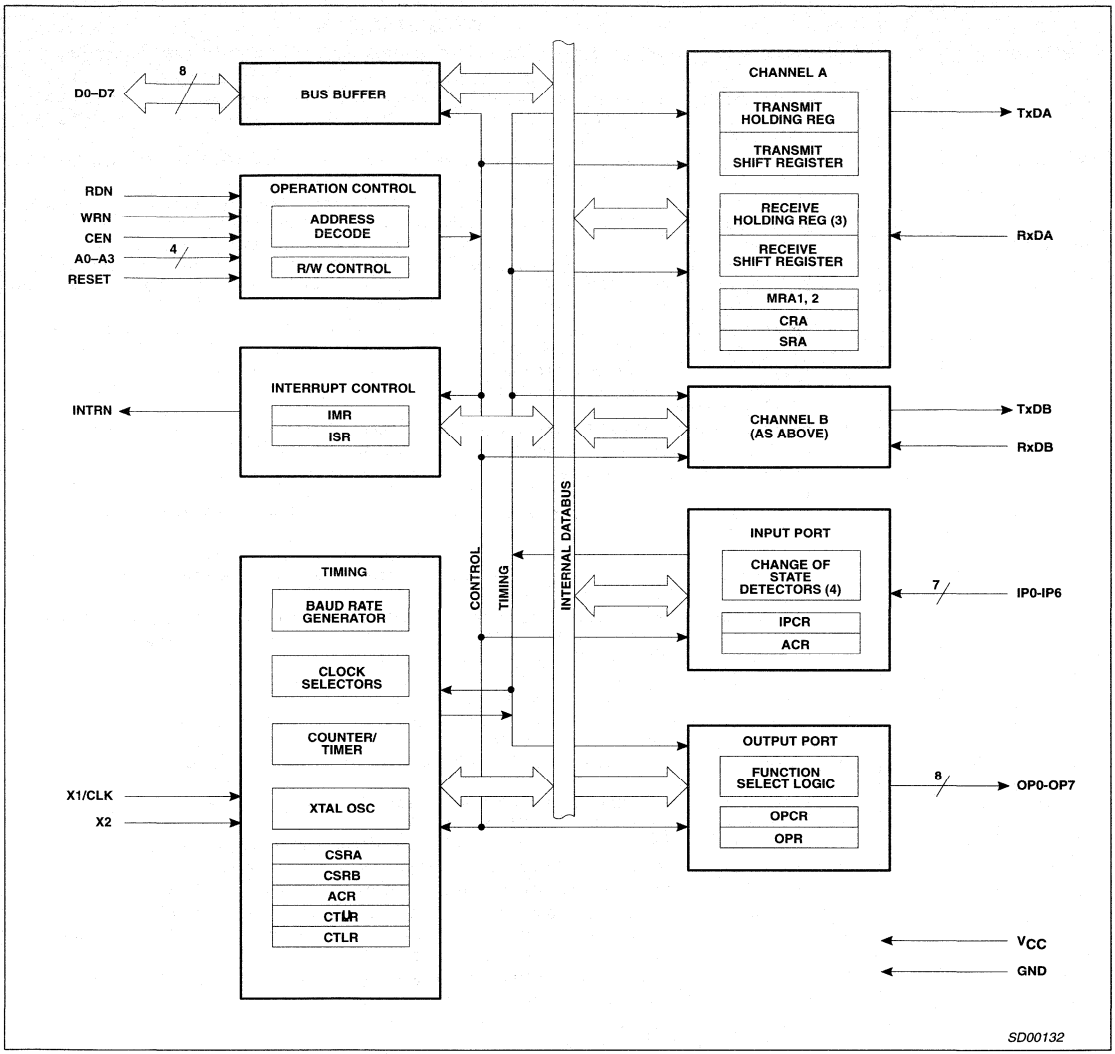


Figure 2. Block Diagram

PIN DESCRIPTION

SYMBOL	APPLICABLE		TYPE	NAME AND FUNCTION
	40,44	28		
D0-D7	X	X	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	X	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When High, places the D0-D7 lines in the 3-State condition.
WRN	X	X	I	**Write Strobe:** When Low and CEN is also Low, the contents of the data bus are loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	X	I	**Read Strobe:** When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0-A3	X	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	X	I	**Reset:** A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0-OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Resets Test modes, MR pointer set to MR1.
INTRN	X	X	O	**Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	X	I	**Crystal 1:** Crystal connection or an external clock input. A crystal of a clock the appropriate frequency (nominally 3.6864 MHz) must be supplied at all times. For crystal connections see Figure 7 (included in CD-ROM version), Clock Timing.
X2	X	X	I	**Crystal 2:** Crystal connection. See Figure 7 (included in CD-ROM version). If a crystal is not used it is best to keep this pin not connected although it is permissible to ground it.
RxDA	X	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	X	X	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	X	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	X	X	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	X	X	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	X	X	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	X		O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	X		O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	X		O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYAN/FFULLAN output.
OP5	X		O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYBN/FFULLBN output.
OP6	X		O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYAN output.
OP7	X		O	**Output 7:** General purpose output, or Channel B open-drain, active-Low, TxRDYBN output.
IP0	X		I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP1	X		I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP2	X	X	I	**Input 2:** General purpose input or counter/timer external clock input. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP3	X		I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP4	X		I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP5	X		I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP6	X		I	**Input 6:** General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
V_{CC}	X	X	I	**Power Supply:** +5V supply input.
GND	X	X	I	**Ground**

Enhanced octal universal asynchronous receiver/transmitter (Octal UART) SCC2698B

DESCRIPTION

The SCC2698B Enhanced Octal Universal Asynchronous Receiver/Transmitter (Octal UART) is a single chip MOS-LSI communications device that provides eight full-duplex asynchronous receiver/transmitter channels in a single package. It is fabricated with CMOS technology which combines the benefits of high density and low power consumption.

The operating speed of each receiver and transmitter can be selected independently as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the Octal UART particularly attractive for dual-speed channel applications such as clustered terminal systems.

The receiver is quadruple buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full.

The UART provides a power-down mode in which the oscillator is frozen but the register contents are stored. This results in reduced power consumption on the order of several magnitudes. The Octal UART is fully TTL compatible and operates from a single +5V power supply.

The SCC2698B is an upwardly compatible version of the 2698A Octal UART. In PLCC packaging, it is enhanced by the addition of receiver ready or FIFO full status outputs, and transmitter empty status outputs for each channel on 16 multipurpose I/O pins. The multipurpose I/O pins of the SCC2698B were inputs only on the SCC2698A.

FEATURES

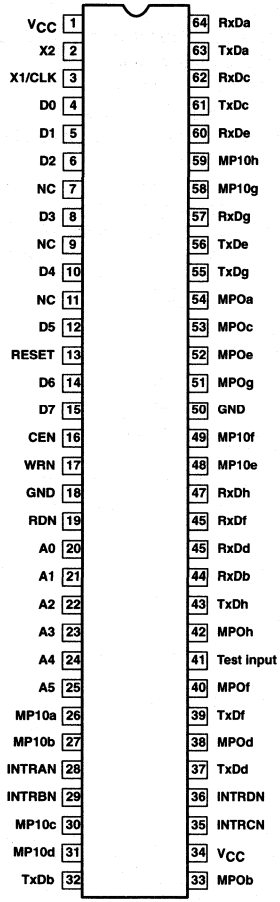
- Eight full-duplex independent asynchronous receiver/transmitters
- Quadruple buffered receiver data register
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Baud rate for the receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4K baud
    Non-standard rates to 115.2K baud
  - User-defined rates from the programmable counter/timer associated with each of four blocks
  - External 1x or 16x clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex), automatic echo, local loop back, remote loopback
- Four multi-function programmable 16-bit counter/timers
- Four interrupt outputs with eight maskable interrupting conditions for each output
- Receiver ready/FIFO full and transmitter ready status available on 16 multi-function pins in PLCC package
- On-chip crystal oscillator
- TTL compatible
- Single +5V power supply with low power mode
- Eight multi-purpose output pins
- Sixteen multi-purpose I/O pins
- Sixteen multi-purpose Input pins with pull-up resistors

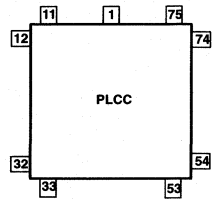
ORDERING INFORMATION

PACKAGES	COMMERCIAL	INDUSTRIAL	DWG #
	V_{CC} = +5V ±5%, T_A = 0°C to +70°C	V_{CC} = +5V ±5%, T_A = –40°C to +85°C	
84-Pin Plastic Leaded Chip Carrier (PLCC)	SCC2698BC1A84	SCC2698BE1A84	SOT189-3

NOTE: Pin Grid Array (PGA) package version is available from Philips Components Military Division.

PIN CONFIGURATIONS





Pin	Function	Pin	Function	Pin	Function
1	TxDa	29	A3	57	RxDd
2	MPP2g	30	MPP2b	58	RxDf
3	RxDa	31	A4	59	RxDh
4	MPP2h	32	A5	60	MPI1e
5	V_{CC}	33	MPI0a	61	MPI0e
6	X2	34	MPI0b	62	MPI1f
7	X1/CLK	35	INTRAN	63	MPI0f
8	D0	36	INTRBN	64	MPP1e
9	D1	37	MPI0c	65	GND
10	D2	38	MPI1c	66	MPP1f
11	D3	39	MPI0d	67	MPOg
12	D4	40	MPI1d	68	MPP2e
13	D5	41	TxDb	69	MPOe
14	MPI1a	42	MPP1c	70	MPP2f
15	RESET	43	MPOb	71	MPOc
16	D6	44	MPP1d	72	MPOa
17	D7	45	V_{CC}	73	TxDg
18	CEN	46	INTRCN	74	TxDe
19	WRN	47	INTRDN	75	RxDg
20	GND	48	MPP2c	76	MPI0g
21	MPI1b	49	TxDd	77	MPI0h
22	RDN	50	MPP2d	78	MPI1g
23	A0	51	MPOd	79	RxDe
24	MPP1a	52	TxDf	80	MPIh
25	A1	53	MPOf	81	TxDc
26	MPP1b	54	MPOh	82	MPP1g
27	A2	55	TxDh	83	RxDc
28	MPP2a	56	RxDb	84	MPP1h

SD00184

Figure 1. Pin Configurations

BLOCK DIAGRAM

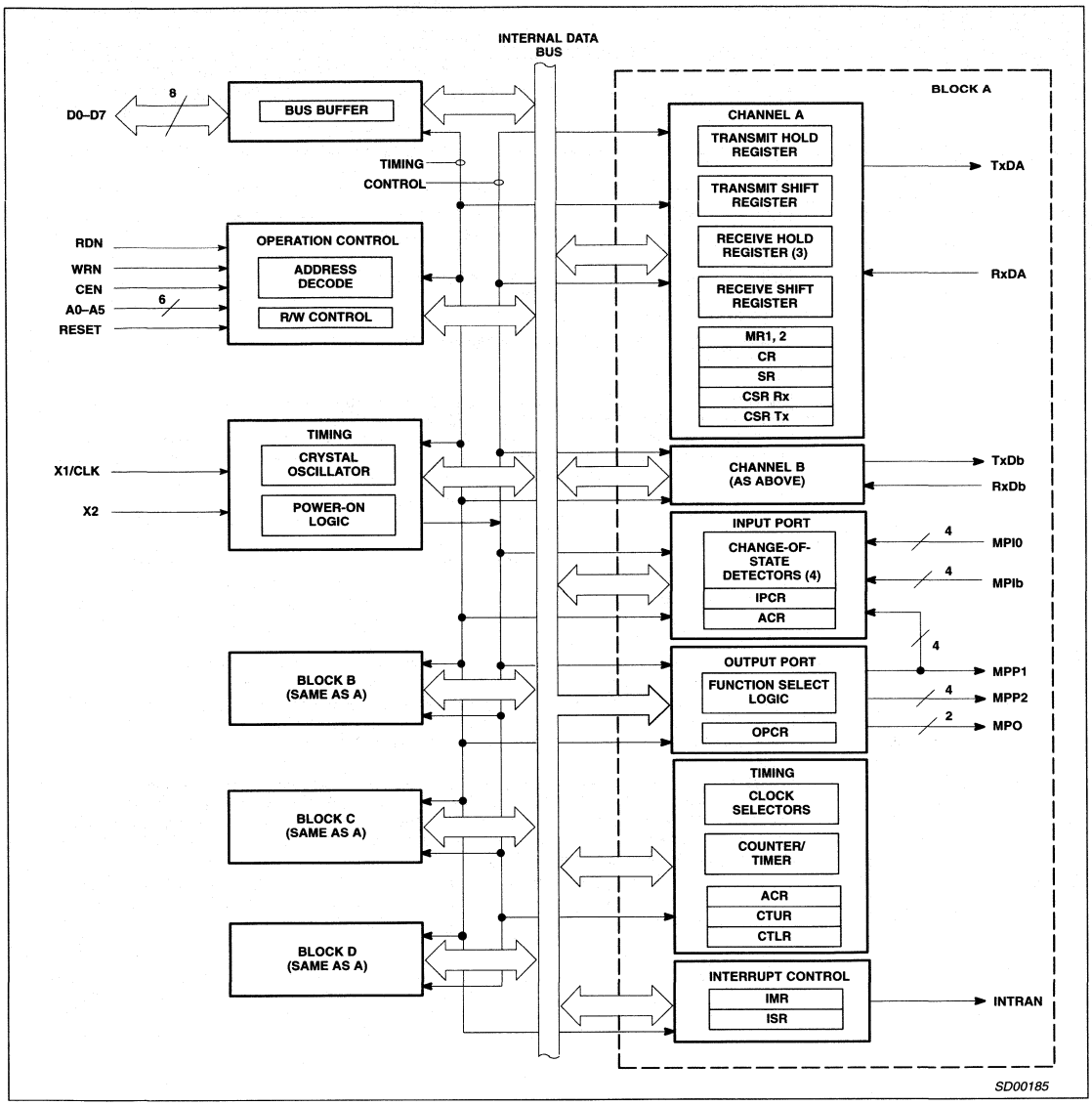


Figure 2. Block Diagram

PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
D0–D7	8–13, 16, 17	I/O	**Data Bus:** Active–High 8-bit bidirectional 3-State data bus. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the Octal UART take place over this bus. The direction of the transfer is controlled by the WRN and RDN inputs when the CEN input is low. When the CEN input is High, the data bus is in the 3-State condition.
CEN	18	I	**Chip Enable:** Active-Low input. When Low, data transfers between the CPU and the Octal UART are enabled on D0–D7 as controlled by the WRN, RDN and A0–A5 inputs. When CEN is High, the Octal UART is effectively isolated from the data bus and D0–D7 are placed in the 3-State condition.
WRN	19	I	**Write Strobe:** Active-Low input. A Low on this pin while CEN is Low causes the contents of the data bus to be transferred to the register selected by A0–A5. The transfer occurs on the trailing (rising) edge of the signal.
RDN	22	I	**Read Strobe:** Active-Low input. A Low on this pin while CEN is Low causes the contents of the register selected by A0–A5 to be placed on the data bus. The read cycle begins on the leading (falling) edge of RDN.
A0–A5	23, 25, 27, 29, 31, 32	I	**Address Inputs:** Active-High address inputs to select the Octal UART registers for read/write operations.
RESET	15	I	**Reset:** Master reset. A High on this pin clears the status register (SR), clears the interrupt mask register (IMR), clears the interrupt status register (ISR), clears the output port configuration register (OPCR), places the receiver and transmitter in the inactive state causing the TxD output to go to the marking (High) state, and stops the counter/timer. Clears power-down mode and interrupts. Clears Test Modes, sets MR pointer to MR1.
INTRAN–INTRDN	35, 36, 46, 47	O	**Interrupt Request:** This active-Low open drain output is asserted on occurrence of one or more of eight maskable interrupting conditions. The CPU can read the interrupt status register to determine the interrupting condition(s).
X1/CLK	7	I	**Crystal 1:** Crystal or external clock input. When using the crystal oscillator, this pin serves as the connection for one side of the crystal. If a crystal is not used, an external clock is supplied at this input. An external clock (or crystal) is required even if the internal baud rate generator is not utilized. This clock is used to drive the internal baud rate generator, as an optional input to the timer/counter, and to provide other clocking signals required by the chip.
X2	6	I	**Crystal 2:** Connection for other side of crystal. If an external source is used instead of a crystal, this connection should be left open (see Figure 7, included in CD-ROM version).
RxDa–RxDh	3, 56, 83, 57, 79, 58, 75, 59	I	**Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified, this input is sampled on the rising edge of the clock. If internal clock is used, the RxD input is sampled on the rising edge of the RxC1x signal as seen on the MPO pin.
TxDa–TxDh	1, 41, 81, 49, 74, 52, 73, 55	O	**Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the marking (High) condition when the transmitter is idle or disabled and when the Octal UART is operating in local loopback mode. If external transmitter is specified, the data is shifted on the falling edge of the transmitter clock. If internal clock is used, the TxD output changes on the falling edge of the TxC1x signal as seen on the MPO pin.
MPOa–MPOh	72, 43, 71, 51, 69, 53, 67, 54	O	**Multi-Purpose Output:** Each of the four DUARTS has two MPO pins (one per UART). One of the following eight functions can be selected for this output pin by programming the OPCR (output port configuration register). Note that reset conditions MPO pins to RTSN. **RTSN** – Request to send active-Low output. This output is asserted and negated via the command register. By appropriate programming of the mode registers, (MR1[7])=1 RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted or when the receiver FIFO and shift register are full. RTSN is an internal signal which normally represents the condition of the receiver FIFO not full, i.e., the receiver can request more data to be sent. However, it can also be controlled by the transmitter empty and the commands 8h and 9h written to the CR (command register). **C/TO** – The counter/timer output. **TxC1X** – The 1X clock for the transmitter. **TxC16X** – The 16X clock for the transmitter. **RxC1X** – The 1X clock for the receiver. **RxC16X** – The 16X clock for the receiver. **TxRDY** – Transmitter holding register empty signal. **RxRDY/FFULL** – Receiver FIFO not empty/full signal.
MPI0a–MPI0h	33, 34, 37, 39, 61, 63, 76, 77	I	**Multi-Purpose Input 0:** This pin (one in each UART) is programmable. Its state can always be read through the IPCR bit 0, or the IPR bit 0. **CTSN:** By programming MR2[4] to a 1, this input controls the clear-to-send function for the transmitter. It is active low. This pin is provided with a change-of-state detector.

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
MPI1a–MPI1h	14, 21, 38, 40, 60, 62, 78, 80	I	**Multi-Purpose Input 1:** This pin (one for each unit) is programmable. Its state can always be determined by reading the IPCR bit 1 or IPR bit 1. **C/TCLK** – This input will serve as the external clock for the counter/timer when ACR[5] is set to 0. This occurs only for channels a, c, e, and g since there is one counter/timer for each DUART block. This pin is provided with a change-of-state detector.
MPP1a–MPP1h	24, 26, 42, 44, 64, 66, 82, 84	I/O	**Multi-Purpose Pin 1:** This pin (one for each UART) is programmed to be an input or an output according to the state of OPCR[7]. (0 = input, 1 = output). The state of the multi-purpose pin can always be determined by reading the IPR. When programmed as an input, it will be the transmitter clock (TxCLK). It will be 1x or 16x according to the clock select registers (CSR[3.0]). When programmed as an output, it will be the status register TxRDY bit. These pins have a small pull-up device.
MPP2a–MPP2h	28, 30, 48, 50, 68, 70, 2, 4	I/O	**Multi-Purpose Pin 2:** This pin (one for each UART) is programmed to be an input or an output according to the state of OPCR[7]. (0 = input, 1 = output). The state of the multi-purpose pin can always be determined by reading the IPR. When programmed as an input, it will be the receiver clock (RxCLK). It will be 1x or 16x according to the clock select registers (CSR[7:4). When programmed as an output, it will be the ISR status register RxRDY/FIFO full bit. These pins have a small pull-up device.
Test Input	–	I	**Test Input:** This pin is used as an input for test purposes at the factory while in test mode. This pin can be treated as 'N/C' by the user. It can be tied high, or left open.
V_{CC}	5, 45	I	**Power Supply:** +5V supply input.
GND	20, 65	I	**Ground**

Dual asynchronous receiver/transmitter (DUART) SCC68692

DESCRIPTION

The Philips Semiconductors SCC68692 Dual Universal Asynchronous Receiver/Transmitter (DUART) is compatible with SCN68681. It is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It is compatible with other S68000 family devices and can also interface easily with other microprocessors. The DUART can be used in a polled or interrupt driven systems.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruple buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the receiver buffer is full.

Also provided on the SCC68692 are a multipurpose 6-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

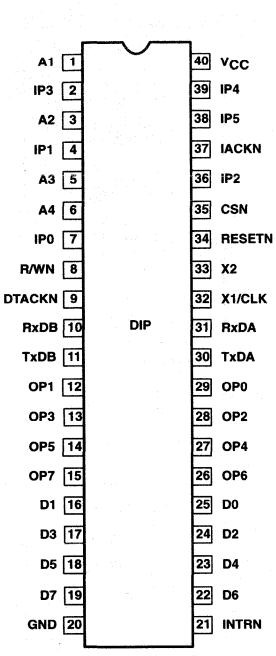
FEATURES

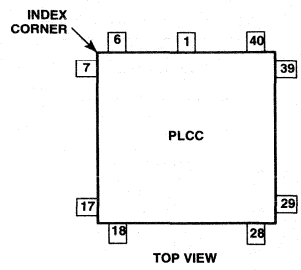
- S68000 bus compatible
- Dual full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data register
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- 16-bit programmable Counter/Timer
- Programmable baud rate for each receiver and transmitter selectable from:
  - 22 fixed rates: 50 to 115.2k baud
  - Non-standard rates to 115.2kb
  - Non-standard user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
  - Multidrop mode (also called 'wake-up' or '9-bit')
- Multi-function 6-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - Inputs have typically >100k pull-up resistors
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Interrupt vector output on interrupt acknowledge
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates: 1X – 1MB/sec, 16X – 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver timeout mode
- Commercial and Industrial temperature range versions
- TTL compatible
- Single +5V power supply

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL	INDUSTRIAL	DWG #
	V_{CC} = +5V ±10%, T_A = 0 to +70°C	V_{CC} = +5V ±10%, T_A = -40 to +85°C	
40-Pin (600 mils wide) Ceramic Dual In-Line Package (Cerdip)	SCC68692C1F40	SCC68692E1F40	0590B
40-Pin (600 mils wide) Plastic Dual In-Line Package (DIP)	SCC68692C1N40	SCC68692E1N40	SOT129-1
44-Pin Plastic Leaded Chip Carrier (PLCC)	SCC68692C1A44	SCC68692E1A44	SOT187-2

PIN CONFIGURATIONS





PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A1	24	INTRN
3	IP3	25	D6
4	A2	26	D4
5	IP1	27	D2
6	A3	28	D0
7	A4	29	OP6
8	IP0	30	OP4
9	R/WN	31	OP2
10	DTACKN	32	OP0
11	RxDB	33	TxDA
12	NC	34	NC
13	TxDB	35	RxDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESETN
17	OP7	39	CSN
18	D1	40	IP2
19	D3	41	IACKN
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	VCC

SD00144

Figure 1. Pin Configurations

BLOCK DIAGRAM

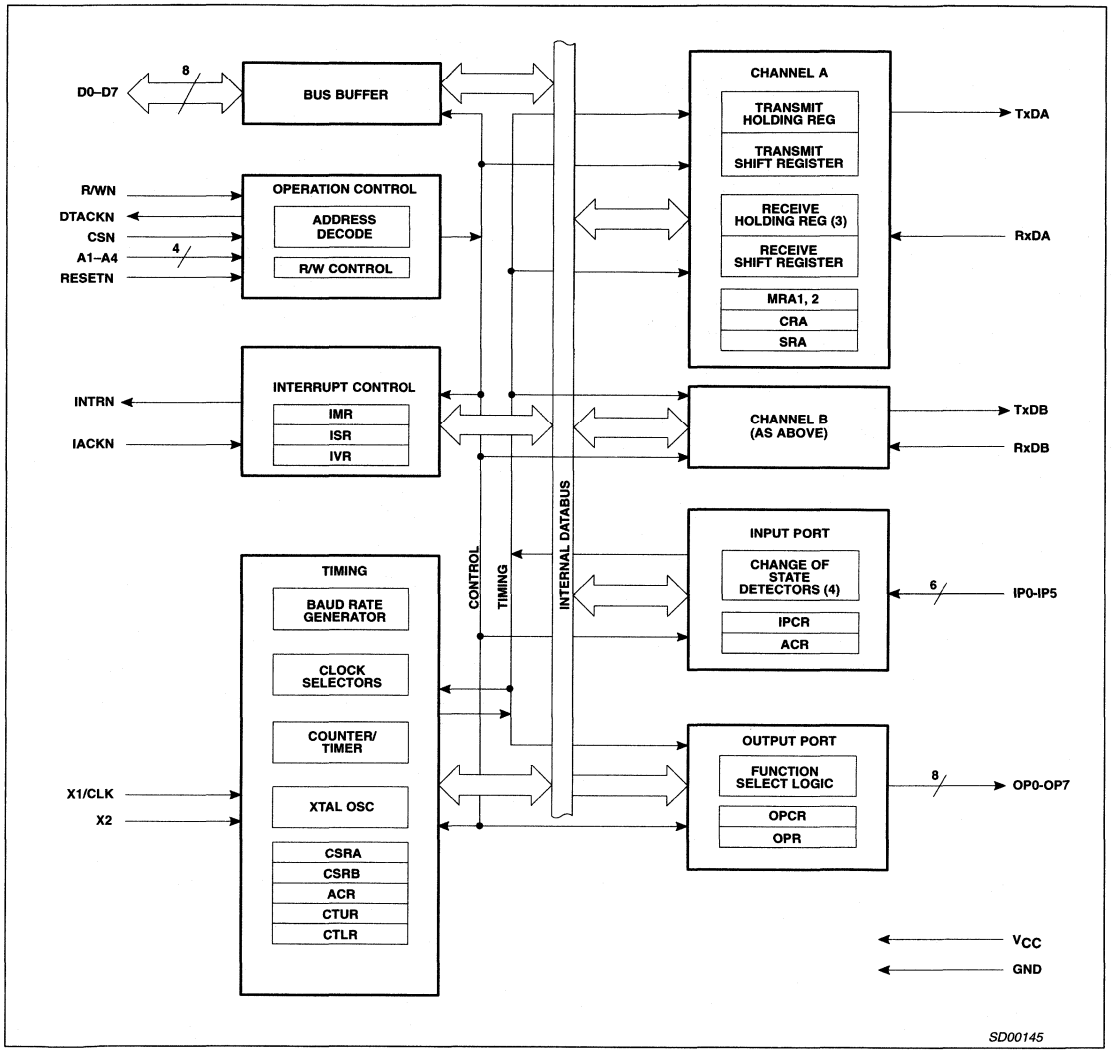


Figure 2. Block Diagram

PIN DESCRIPTION

SYMBOL	PIN NO.	TYPE	NAME AND FUNCTION
D0–D7	25,16,24,17 23,18,22,19	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CSN	35	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the R/WN and A1–A4 inputs. When CEN is High, the DUART places the D0–D7 lines in the 3-State condition.
R/WN	8	I	**Read/Write:** A High input indicates a read cycle and a low input indicates a write cycle, when a cycle is initiated by assertion of the CSN input.
A1–A4	1,2,5,6	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESETN	34	I	**Reset:** A Low level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to hex 0F, puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Resets Test Mode, sets MR pointer to MR1.
DTACKN	9	O	**Data Transfer Acknowledge:** 3-State active-Low output asserted in write, read, or interrupt cycles to indicate proper transfer of data between the CPU and the DUART.
INTRN	21	O	**Interrupt Request:** Active-Low, open-drain output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
IACKN	37	I	**Interrupt Acknowledge:** Active-Low input indicating an interrupt acknowledge cycle. In response, the DUART will place the interrupt vector on the data bus and will assert DTACKN if it has an interrupt pending.
X1/CLK	32	I	**Crystal 1:** Crystal connection or an external clock input. A crystal of a clock the appropriate frequency (nominally 3.6864 MHz) must be supplied at all times. For crystal connections see Figure 9 (included in CD-ROM version), Clock Timing.
X2	33	I	**Crystal 2:** Crystal connection. See Figure 9 (included in CD-ROM version). If a crystal is not used it is best to keep this pin not connected although it is permissible to ground it.
RxDA	31	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	10	I	**Channel B Receive Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	30	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	11	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	29	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	12	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	28	O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	13	O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	27	O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYAN/FFULLAN output.
OP5	14	O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYBN/FFULLBN output.
OP6	26	O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYAN output.
OP7	15	O	**Output 7:** General purpose output or Channel B open-drain, active-Low, TxRDYBN output.
IP0	7	I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP1	4	I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP2	36	I	**Input 2:** General purpose input or Channel B receiver external clock input (RxCB), or counter/timer external clock input. When external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP3	2	I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP4	39	I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP5	38	I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
V_{CC}	40	I	**Power Supply:** +5V supply input.
GND	20	I	**Ground**

Dual asynchronous receiver/transmitter (DUART) SCN2681

DESCRIPTION

The Philips Semiconductors SCN2681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

Also provided on the SCN2681 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SCN2681 is available in three package versions: 40-pin and 28–pin, both 0.6" wide DIPs; a compact 24-pin 0.4" wide DIP; and a 44-pin PLCC.

FEATURES

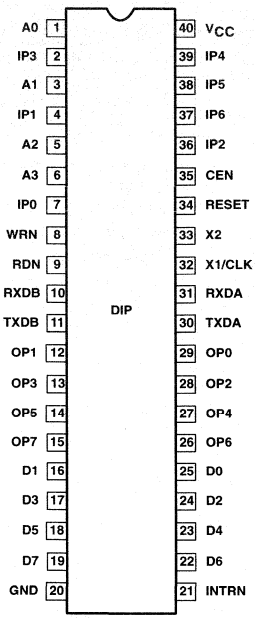
- Dual full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 22 fixed rates: 50 to 115.2k baud
- 16-bit programmable Counter/Timer
  - Non-standard rates to 115.2Kb
  - One user-defined rate derived from programmable timer/counter
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - 100kΩ typical pull-up resistor
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer: 1X – 1MB/sec, 16X – 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Single +5V power supply
- Commercial and industrial temperature ranges available
- DIP and PLCC packages

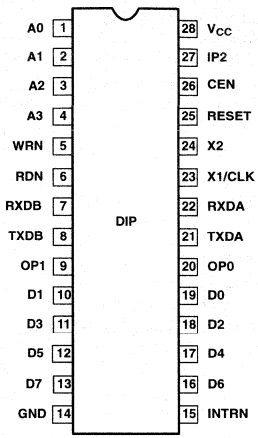
ORDERING INFORMATION

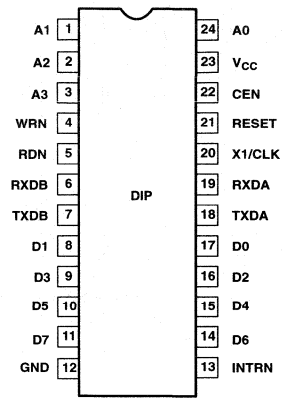
DESCRIPTION	ORDER CODE			
	Commercial		Industrial	
	V_{CC} = +5V ±5%, T_A = 0°C to +70°C		V_{CC} = +5V ±10%, T_A = -40°C to +85°C	
	Plastic DIP	Plastic LCC	Plastic DIP	Plastic LCC
24-Pin[1]	SCN2681AC1N24	Not available	SCN2681AE1N24	Not available
28-Pin[2]	SCN2681AC1N28	Not available	SCN2681AE1N28	Not available
40-Pin[2]	SCN2681AC1N40	Not available	SCN2681AE1N40	Not available
44-Pin	Not available	SCN2681AC1A44	Not available	SCN2681AE1A44

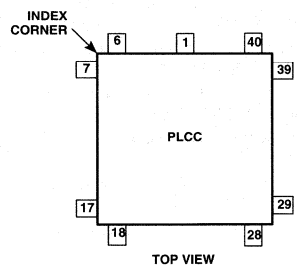
NOTES:
1. 400mil-wide Dual In-Line Package
2. 600mil-wide Dual In-Line Package

PIN CONFIGURATIONS









PIN	FUNCTION	PIN	FUNCTION
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RXDB	33	TXDA
12	NC	34	NC
13	TXDB	35	RXDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	VCC

SD00084

Figure 1. Pin Configurations

PIN DESCRIPTION

SYMBOL	APPLICABLE			TYPE	NAME AND FUNCTION
	40/44	28	24		
D0–D7	X	X	X	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	X	X	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When High, places the D0-D7 lines in the 3-State condition.
WRN	X	X	X	I	**Write Strobe:** When Low and CEN is also Low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	X	X	I	**Read Strobe:** When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0–A3	X	X	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	X	X	I	**Reset:** A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Clears Test modes, sets MR pointer to MR1.
INTRN	X	X	X	O	**Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	X	X	I	**Crystal 1:** Crystal connection or an external clock input. A crystal of a clock the appropriate frequency (nominally 3.6864 MHz) must be supplied at all times. For crystal connections see Figure 7 (included in CD-ROM version), Clock Timing.
X2	X	X		I	**Crystal 2:** Crystal connection. See Figure 7 (included in CD-ROM version). If a crystal is not used it is best to keep this pin not connected although it is permissible to ground it.
RxDA	X	X	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	X	X	X	I	**Channel B Receive Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	X	X	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	X	X	X	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
OP0	X	X		O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	X	X		O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	X			O	**Output 2:** General purpose output or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	X			O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	X			O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYA/FFULLA output.
OP5	X			O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYB/FFULLB output.
OP6	X			O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYA output.
OP7	X			O	**Output 7:** General purpose output or Channel B open-drain, active-Low, TxRDYB output.
IP0	X			I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP1	X			I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP2	X	X		I	**Input 2:** General purpose input or counter/timer external clock input. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP3	X			I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP4	X			I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.

PIN DESCRIPTION (Continued)

SYMBOL	APPLICABLE			TYPE	NAME AND FUNCTION
	40/44	28	24		
IP5	X			I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP6	X			I	**Input 6:** General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
V_{CC}	X	X		I	**Power Supply:** +5V supply input.
GND	X	X		I	**Ground**

BLOCK DIAGRAM

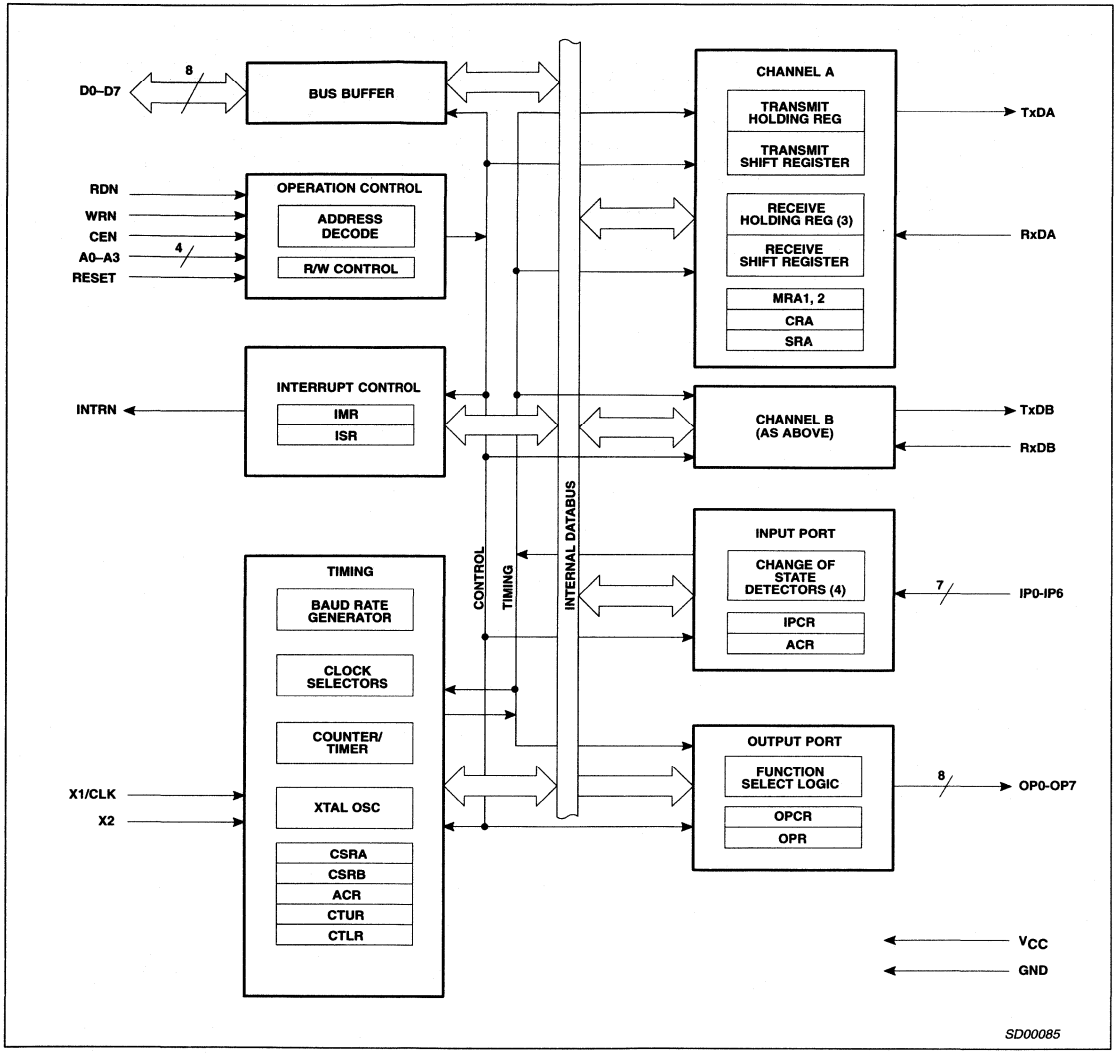


Figure 2. Block Diagram

Dual asynchronous receiver/transmitter (DUART) SCN2681T

DESCRIPTION

The Philips Semiconductors SCN2681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. The SCN2681T features a faster bus cycle time than the standard SCN2681. The quick bus cycle eliminates or reduces the need for wait states with fast CPUs and permits high throughput in I/O intensive systems. Higher external clock rates may be used with the transmitter, receiver and counter timer which in turn provide greater versatility in baud rate generation. The SCN2681T interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruple buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the receiver buffer is full.

Also provided on the SCN2681T are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

For a complete functional description and programming information for the SCN2681T, refer to the SCN2681 product specification.

FEATURES

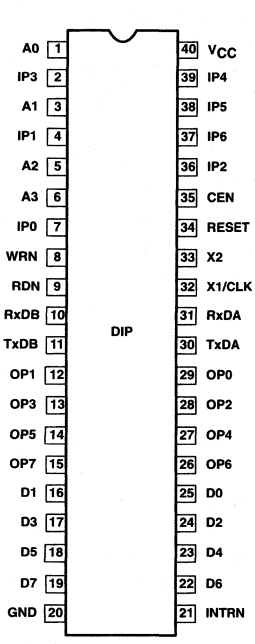
- Fast bus cycle times reduce or eliminate CPU wait states
- Dual full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- 16-bit programmable Counter/Timer
- Programmable baud rate for each receiver and transmitter selectable from:
  - 22 fixed rates: 50 to 115.2k baud
  - Non-standard rates to 115.2
  - Non-standard user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - 100kΩ typical pull-up resistors
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates:
  1X – 1MB/sec transmitter and receiver; 16X – 500kB/sec receiver and 250kB/sec transmitter
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Single +5V power supply
- Commercial and industrial temperature ranges available

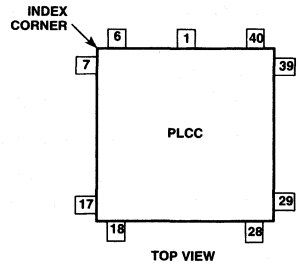
ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0°C to +70°C	DWG #
40-Pin Plastic Dual In-Line Package (600mil-wide DIP)	SCN2681TC1N40	SOT129-1
44-Pin Plastic Lead Chip Carrier (PLCC)	SCN2681TC1A44	SOT187-2

NOTE: For a full register description and programming information see the SCN2681.

PIN CONFIGURATIONS





PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RxDB	33	TxDA
12	NC	34	NC
13	TxDB	35	RxDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	V_{CC}

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Figure 1. Pin Configurations

NOTE:
Refer to SCN2681 for functional description.

BLOCK DIAGRAM

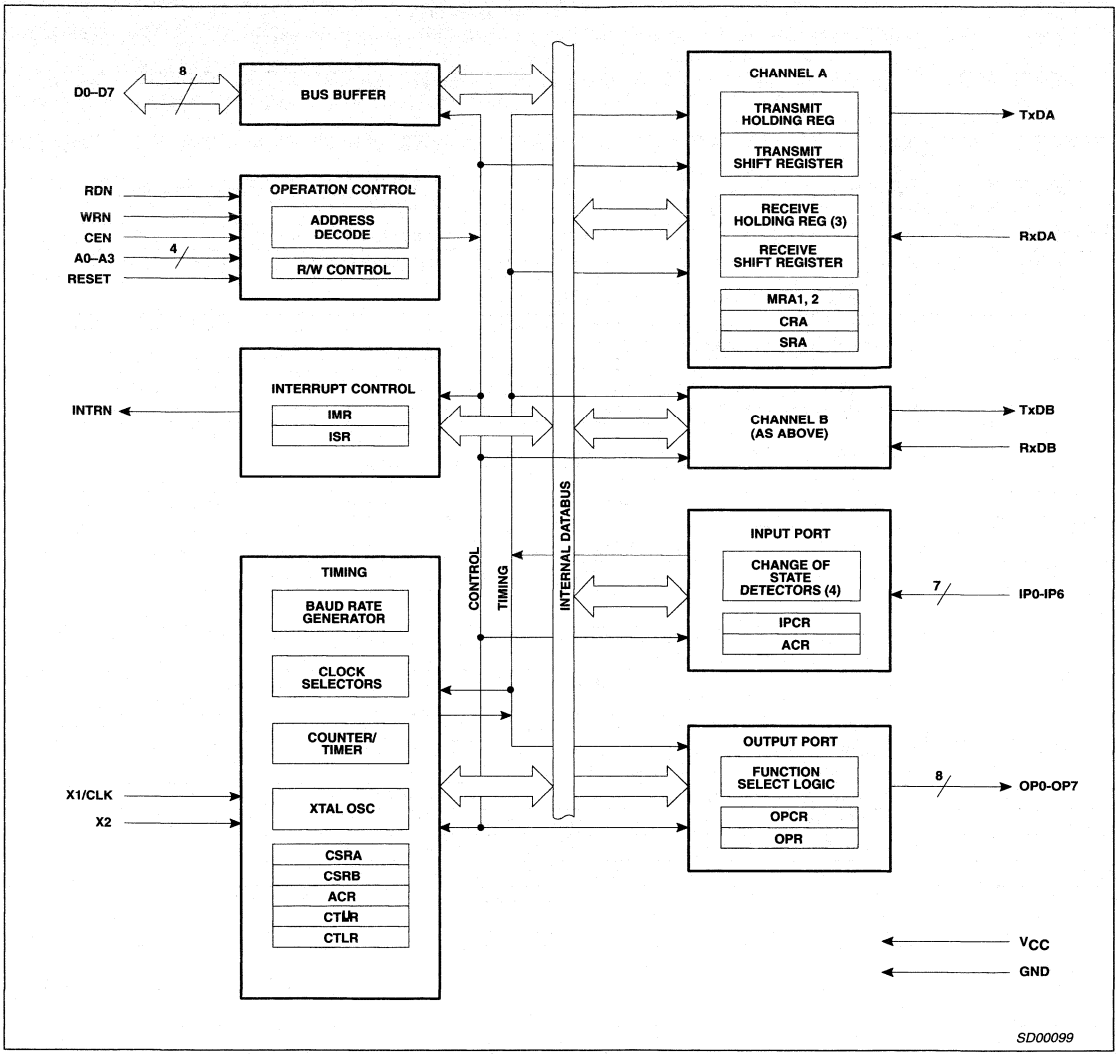


Figure 2. Block Diagram

PIN DESCRIPTION

MNEMONIC	TYPE	NAME AND FUNCTION
D0–D7	I/O	**Data Bus:** Bidirectional three-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	I	**Chip Enable:** Active low input signal. When low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the WRN, RDN, and A0–A3 inputs. When CEN is high, the DUART places the D0–D7 lines in the three-state condition.
WRN	I	**Write Strobe:** When low and CEN is also low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	I	**Read Strobe:** When low and CEN is also low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0–A3	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	I	**Reset:** A high level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the high state, stops the counter/timer, and puts channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (high) state. Clears Test modes, sets MR pointer to MR1.
INTRN	O	**Interrupt Request:** Active-low, open-drain output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	I	**Crystal 1:** Crystal connection or an external clock input. A crystal of a clock the appropriate frequency (nominally 3.6864 MHz) must be supplied at all times. For crystal connections see Figure 7 (included in CD-ROM version), Clock Timing.
X2	I	**Crystal 2:** Crystal connection. See Figure 7 (included in CD-ROM version). If a crystal is not used it is best to keep this pin not connected although it is permissible to ground it.
RxDA	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
RxDB	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
TxDA	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
TxDB	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
OP0	O	**Output 0:** General purpose output, or channel A request to send (RTSAN, active-low). Can be deactivated automatically on receive or transmit.
OP1	O	**Output 1:** General purpose output, or channel B request to send (RTSBN, active-low). Can be deactivated automatically on receive or transmit.
OP2	O	**Output 2:** General purpose output, or channel A transmitter 1X or 16X clock output, or channel A receiver 1X clock output.
OP3	O	**Output 3:** General purpose output, or open-drain, active-low counter/timer output, or channel B transmitter 1X clock output, or channel B receiver 1X clock output.
OP4	O	**Output 4:** General purpose output, or channel A open-drain, active-low, RxRDYA/FFULLA output.
OP5	O	**Output 5:** General purpose output, or channel B open-drain, active-low, RxRDYB/FFULLB output.
OP6	O	**Output 6:** General purpose output, or channel A open-drain, active-low, TxRDYA output.
OP7	O	**Output 7:** General purpose output, or channel B open-drain, active-low TxRDYB output.
IP0	I	**Input 0:** General purpose input, or channel A clear to send active-low input (CTSAN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP1	I	**Input 1:** General purpose input, or channel B clear to send active-low input (CTSBN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP2	I	**Input 2:** General purpose input, or counter/timer external clock input. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP3	I	**Input 3:** General purpose input, or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP4	I	**Input 4:** General purpose input, or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP5	I	**Input 5:** General purpose input, or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP6	I	**Input 6:** General purpose input, or channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
V_{CC}	I	**Power Supply:** +5V supply input.
GND	I	**Ground**

Dual asynchronous receiver/transmitter (DUART) SCN68681

DESCRIPTION

The Philips Semiconductors SCN68681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It is compatible with other S68000 family devices, and can also interface easily with other microprocessors. The DUART can be used in polled or interrupt driven systems.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

Also provided on the SCN68681 are a multipurpose 6-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

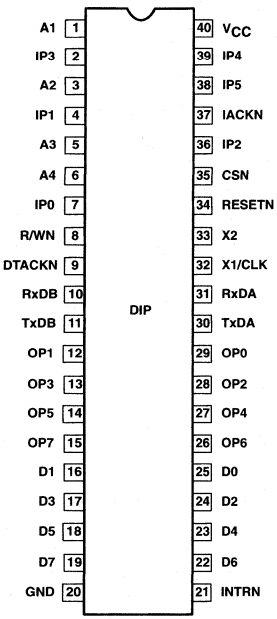
FEATURES

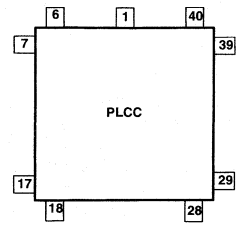
- S68000 bus compatible
- Dual full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 22 fixed rates: 50 to 115.2k baud
  - Non-standard rates to 115.2kb
  - Non-standard user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- 16-bit programmable Counter/Timer
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 6-bit input port
  - Can serve as clock or control inputs
  - Change-of-state detection on four inputs
  - 100kΩ typical pull-up resistors
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Interrupt vector output on interrupt acknowledge
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates:
  1X - 1MB/sec, 16X - 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Single +5V power supply
- Commercial and industrial temperature ranges available
- DIP and PLCC packages

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL	INDUSTRIAL	DWG #
	V_{CC} = +5V +5%, T_A = 0°C to +70°C	V_{CC} = +5V +10%, T_A = 40°C to +85°C	
40-Pin Ceramic Dual In-Line Package (cerdip)	Not available	SCN68681E1F40	0590B
40-Pin Plastic Dual In-Line Package (DIP)	SCN68681C1N40	SCN68681E1N40	SOT129-1
44-Pin Plastic Leaded Chip Carrier (PLCC)	SCN68681C1A44	SCN68681E1A44	SOT187-2

PIN CONFIGURATIONS





PIN/FUNCTION

1	NC	16	OP5	31	OP2
2	A1	17	OP7	32	OP0
3	IP3	18	D1	33	TxDA
4	A2	19	D3	34	NC
5	IP1	20	D5	35	RxDA
6	A3	21	D7	36	X1/CLK
7	A4	22	GND	37	X2
8	IP0	23	NC	38	RESETN
9	R/WN	24	INTRN	39	CSN
10	DTACKN	25	D6	40	IP2
11	RxDB	26	D4	41	IACKN
12	NC	27	D2	42	IP5
13	TxDB	28	D0	43	IP4
14	OP1	29	OP6	44	V_{CC}
15	OP3	30	OP4		

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Figure 1. Pin Configurations

BLOCK DIAGRAM

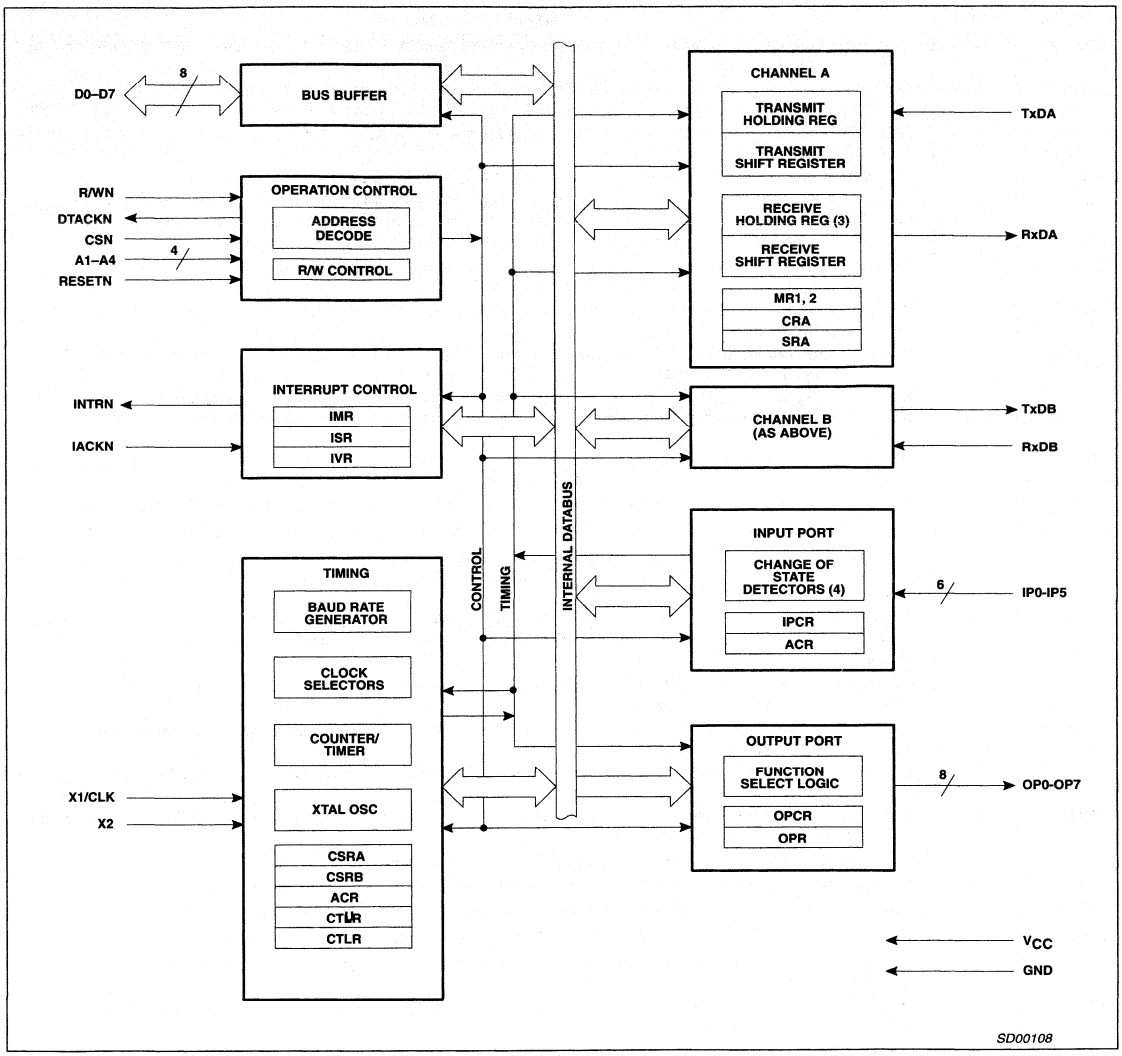

Figure 2. Block Diagram

PIN DESCRIPTION

SYMBOL	TYPE	NAME AND FUNCTION
D0-D7	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CSN	I	**Chip Select:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the R/WN, RDN and A1-A4 inputs. When High, places the D0-D7 lines in the 3-State condition.
R/WN	I	**Read/Write:** A High input indicates a read cycle and a Low input indicates a write cycle, when a cycle is initiated by assertion of the CSN input.
A1-A4	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESETN	I	**Reset:** A Low level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to hex 0F, puts OP0-OP7 in the High state, stops the counter/timer, and puts Channel A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Clears Test modes, sets MR pointer to MR1.
DTACKN	O	**Data Transfer Acknowledge:** Three-state active Low output asserted in write, read, or interrupt cycles to indicate proper transfer of data between the CPU and the DUART.
INTRN	O	**Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
IACKN	I	**Interrupt Acknowledge:** Active-Low input indicating an interrupt acknowledge cycle. In response, the DUART will place the interrupt vector on the data bus and will assert DTACKN if it has an interrupt pending.
X1/CLK	I	**Crystal 1:** Crystal connection or an external clock input. A crystal of a clock the appropriate frequency (nominally 3.6864 MHz) must be supplied at all times. For crystal connections see Figure 9 (included in CD-ROM version), Clock Timing.
X2	I	**Crystal 2:** Crystal connection. See Figure 9 (included in CD-ROM version). If a crystal is not used it is best to keep this pin not connected although it is permissible to ground it.
RxDA	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYA/FFULLA output.
OP5	O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYB/FFULLB output.
OP6	O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYA output.
OP7	O	**Output 7:** General purpose output, or Channel B open-drain, active-Low, TxRDYB output.
IP0	I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP1	I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN). Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP2	I	**Input 2:** General purpose input, or Channel B receiver external clock input (RxCB), or counter/timer external clock input. When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP3	I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP4	I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
IP5	I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock. Pin has an internal V_{CC} pull-up device supplying 1 to 4 μA of current.
V_{CC}	I	**Power Supply:** +5V supply input.
GND	I	**Ground:**

Section 3
Synchronous Communications Controllers

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Synchronous Communication Product Line

Device	Technology Description	Package Type(s)	Icc mA @ Vcc = 5V	Temp Range deg C	Speed	Key Features
SCN2651	NMOS Programmable Communication Interface (PCI)	PDIP28 PLCC28	150	0 to +70 –40 to +85	0–1Mbps data rate 16 internal baud rates (50 to 19.2K) external BRG	• Synchronous/asynchronous operation (full/half duplex) • 5–8 bit character (1, 1.5, 2 stop bits in asynchronous mode) • Odd, even, no parity in asynchronous mode • Single or dual SYN, transparent and non-transparent auto SYN/DLE insertion/deletion in synchronous operations • Double buffer transmit and receive operation
SCN2661 **SCN68661**	NMOS Enhanced Programmable Communication Interface (PCI)	PDIP28 PLCC28	150	0 to +70 –40 to +85	19 internal baud rates (50 to 38.4K)	• Functionally it is an enhanced version of SCN2651 • Available in three different baud rate versions • Enhanced for BREAK detect and external jam sync, DLE detect, SYN1 stripping, drop RTS, stop bit search and data bus timing/drivers
SCN2652 **SCN68652**	NMOS Enhanced Programmable Communication Interface (PCI)	PDIP40 PLCC44	150	0 to +70 –40 to +85	0–2Mbps data rate	• Supports synchronous Bit Oriented (SDLC, ADCCP, HDLC) and Character Oriented (DDCMP, DISYNC) Protocols • SYNC Generation, detection in BCP and Auto Zero insertion/deletion in BOP modes • Programmable 8 or 16 bit data bus • Full/half duplex transmit and receive operation
SCC26562 **SCN68562**	NMOS DUAL Universal Serial Communication Controller (DUSCC)	PDIP48 PLCC52	275	0 to +70	0–4Mbps data rate 16 internal baud rates (50 to 38.4K) Internal DPLL and counters	• Dual channel synchronous and asynchronous operation • Bit Oriented (HDLC, SDLC, X.25/75) and Character Oriented (BISYNC, DDCMP) Protocols • Parity and Frame Check Sequence (FCS) generation/checking • Poll, Interrupt, Vectored Interrupt, Modified Vector Interrupt, DMA and Wait Data Transfer modes • Data coding/encoding modes: NRZ, NRZI, FM0, FM1, Manchester • On-chip oscillator (16MHz), 16 bit counter/timer, DPLL • Modern control inputs/outputs and external synchronous pin • 4 byte receiver and transmitter FIFOs and Rx/Tx shift registers for each channel • Rx overrun and Tx underrun controls • Full/half duplex transmit and receive operation
SC26C562 **SC68C562**	CMOS DUAL Universal Serial Communication Controller (CDUSCC)	PDIP48 PLCC52	80	PDIP48 0 to +70 PLCC52 0 to +70 –40 to +85	0–1Mbps data rate 19 internal baud rates (50 to 64K) Internal DPLL and counters	• Functionally it is an enhancement of SCN26562/68562 • Faster transmit/receive data rate (10MHz) • 16 byte deep Tx/Rx FIFOs • 170ns bus cycle • More and higher internal BRG selections • Better control over individual interrupt conditions • Supports X.21 pattern recognition • Provides more Tx/Rx status information

CMOS dual universal serial communications controller (CDUSCC) SC26C562

DESCRIPTION

The Philips Semiconductors SC26C562 Dual Universal Serial Communications Controller (CDUSCC) is a single-chip CMOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SC26C562 interfaces to synchronous bus MPUs and is capable of program-polled, interrupt driven, block-move or DMA data transfers.

The SC26C562 (CDUSCC) is (PIN) hardware and (REGISTER) software compatible with the existing SCN26562 (DUSCC). CDUSCC will automatically configure to the NMOS DUSCC register map (default mode) on power up.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides sixteen common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the CDUSCC well-suited for dual-speed channel applications. Data rates up to 10Mbits per second are supported.

The transmitter and receiver each contain a sixteen-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to sixteen characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

The SC26C562 CDUSCC is optimized to interface with processors using a synchronous bus interface, such as the 8086, and iAPX86 family. For systems using an asynchronous bus, such as the 68000 and 68010, refer to the SC68C562 documentation.

Refer to the CMOS Dual Universal Serial Communication Controller (CDUSCC) User's Manual for a complete operational description.

FEATURES

General Features

- Dual full-duplex synchronous/ asynchronous receiver and transmitter
- Multi-protocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: Single SYNC, dual SYNC, BiSYNC, DDCMP
  - ASYNC: 5-8 bits plus optional parity
- Sixteen character receive and transmit FIFOs with interrupt threshold control
- FIFO'ed status bits
- Watchdog timer
- 0 to 10 Mbit/sec data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 19 fixed rates: 50 to 64K baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- or half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Compatible with Synchronous and Asynchronous bus DMA controllers
  - Half- or full-duplex operation
  - Single or dual address data transfers
  - Automatic frame termination on counter/ timer terminal count or DMA DONE (EOPN)
- Transmit path clear status
- High speed data bus interface: 160ns bus cycle
- DPLL operation up to 312.5kHz with internal clock
- Interrupt capabilities
  - Vector output (fixed or modified by status)
  - Individual interrupt enable bits
  - Programmable internal priorities
  - Maskable interrupt conditions
  - 80XX/X compatible
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general purpose I/O pins per channel
  - CTS and DCD programmable auto-enables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits

- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X Rx and Tx clock factors
- Parity, overrun and framing error detection
- False start bit detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmit and receive up to 10Mbps at 1x or 1Mbps at 16x data rates

Bit-Oriented Protocol

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Transmit 7 or 8 bit ABORT
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

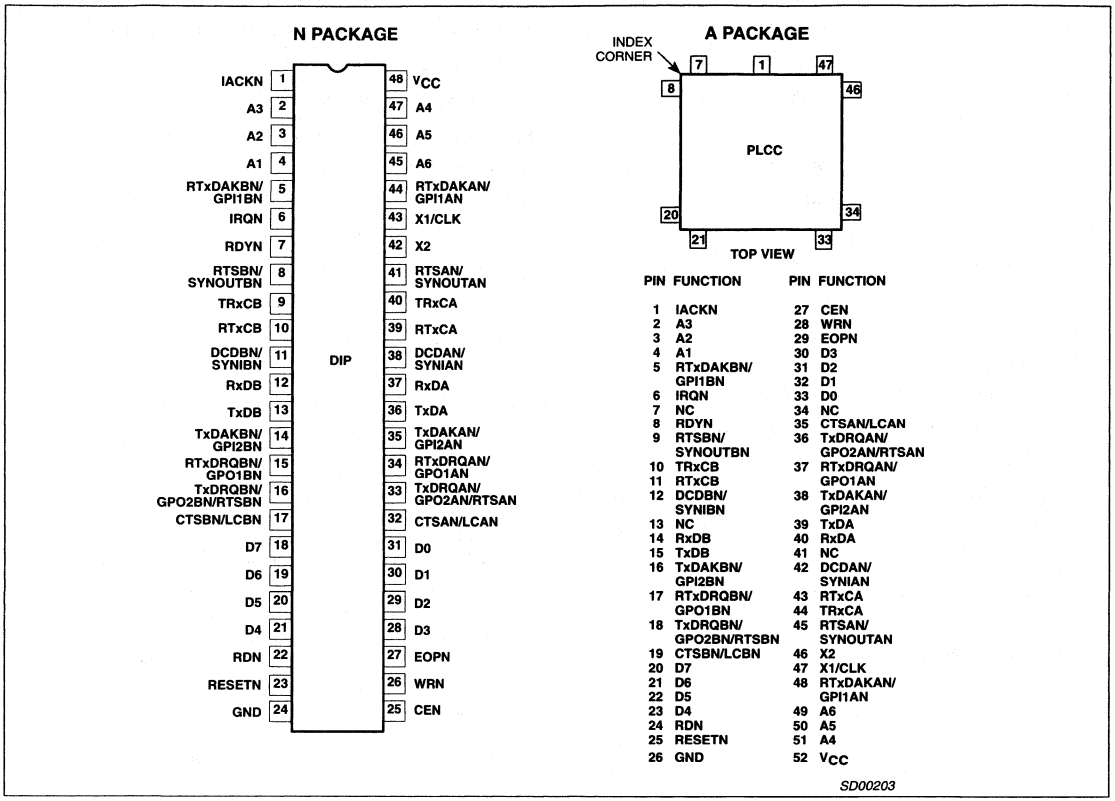
Character-Oriented Protocols

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK line-fill or underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun and underrun error detection
- Optional SYNC exclusion from FCS
- BISYNC features
  - EBCDIC or ASCII header, text and control messages
  - SYN, DLE stripping
  - EOM (end of message) detection and transmission
  - Auto transparency mode switching
  - Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
  - Control character sequence detection for both transparent and normal text
  - Parity generation for data and LRC characters

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL	INDUSTRIAL	DWG #
	Serial Data Rate = 10Mbps Maximum	Serial Data Rate = 8Mbps Maximum	
48-Pin Plastic Dual In-Line Package (DIP)	SC26C562C1N	Not available	SOT240-1
52-Pin Plastic Leaded Chip Carrier (PLCC) Package	SC26C562C1A	SC26C562A8A	SOT238-3

PIN CONFIGURATIONS



PIN	FUNCTION	PIN	FUNCTION
1	IACKN	27	CEN
2	A3	28	WRN
3	A2	29	EOPN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
		32	D1
6	IRQN	33	D0
7	NC	34	NC
8	RDYN	35	CTSAN/LCAN
9	RTSBN/ SYNOUTBN	36	TxDRQAN/ GPO2AN/RTSAN
10	TRxCB	37	RTxDRQAN/ GPO1AN
11	RTxCB		
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
		44	TRxCA
18	TxDRQBN/ GPO2BN/RTSBN	45	RTSAN/ SYNOUTAN
19	CTSBN/LCBN	46	X2
20	D7	47	X1/CLK
21	D6	48	RTxDAKAN/ GPI1AN
22	D5		
23	D4	49	A6
24	RDN	50	A5
25	RESETN	51	A4
26	GND	52	VCC

Figure 1. Pin Configurations

BLOCK DIAGRAM

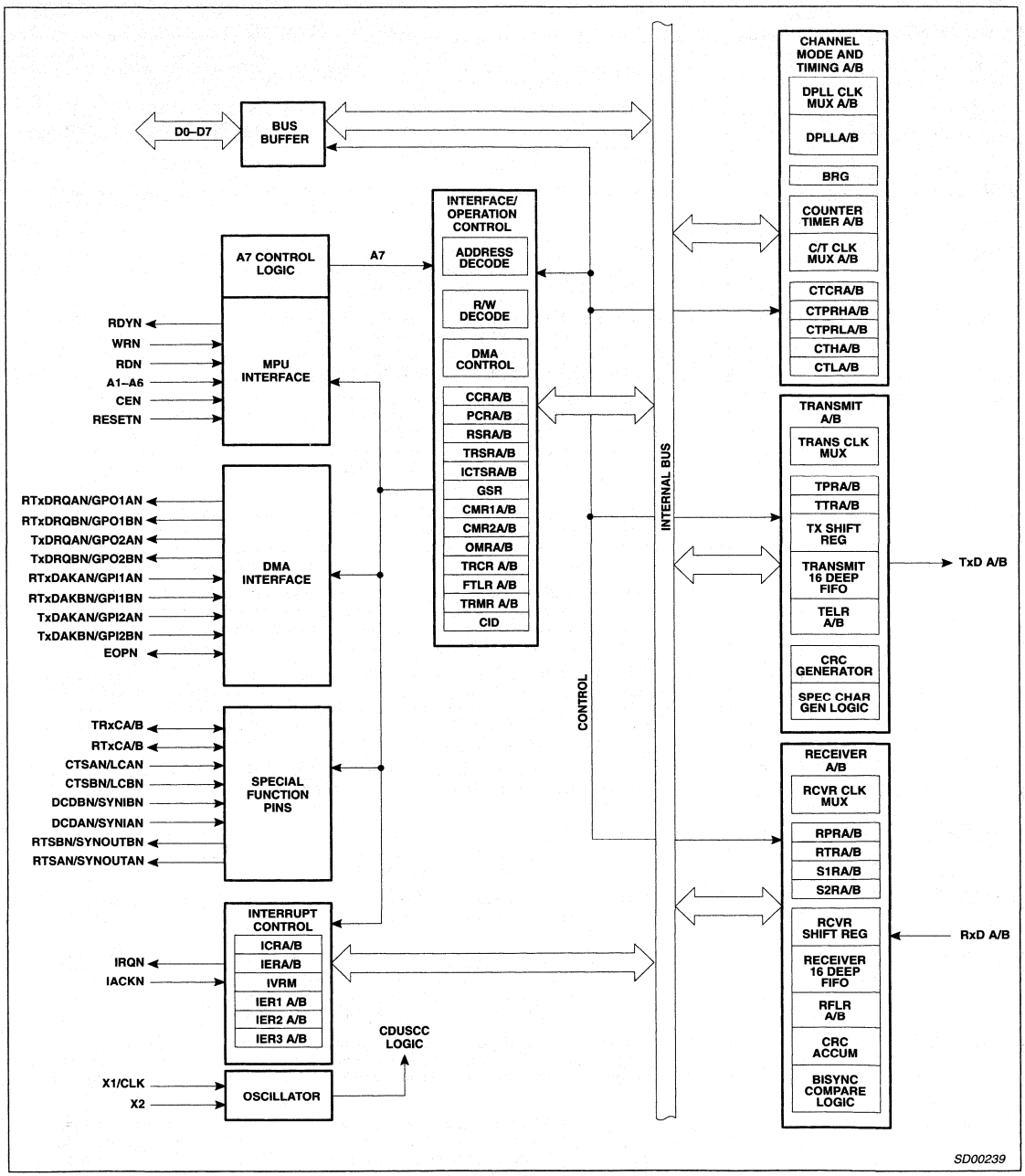


Figure 2. Block Diagram

PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A1–A6	4-2, 47-45	4-2, 51-49	I	**Address Lines:** Active-high. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0–D7	31-28, 21-18	33-30, 23-20	I/O	**Bidirectional Data Bus:** Active-high, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command and status transfers between the CPU and the CDUSCC take place over this bus. The data bus is enabled when CSN and RDN, or CSN and WRRN are low during interrupt acknowledge cycles and single address DMA acknowledge cycles.
RDN	22	24	I	**Read Strobe:** Active-low input. When active and CSN is also active, causes the content of the addressed register to be present on the data bus. RDN is ignored unless CSN is active.
WRN	26	28	I	**Write Strobe:** Active-low input. When active and CSN is also active, the content of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of WRN. WRN is ignored unless CEN is active.
CSN	25	27	I	**Chip Select:** Active-low input. When active, data transfers between the CPU and the CDUSCC are enabled on D0–D7 as controlled by RDN or WRN and A1–A6 inputs. When CSN is high, the data lines are placed in the 3-State condition (except during interrupt acknowledge cycles and single address DMA transfers).
RDYN	7	8	O	**Ready:** Active-low, open drain. Used to synchronize data transfers between the CPU and the CDUSCC. It is valid only during read and write cycles where the CDUSCC is configured in 'wait on Rx', 'wait on Tx' or 'wait on Tx or Rx' modes, otherwise it is always inactive. RDYN becomes active on the leading edge of RDN and WRN if the requested operation cannot be performed (viz, no data in RxFIFO in the case of a read or no room in the TxFIFO in the case of a write).
IRQN	6	6	O	**Interrupt Request:** Active-low, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the CDUSCC to output an interrupt vector on the data bus.
IACKN	1	1	I	**Interrupt Acknowledge:** Active-low. When IACKN is asserted, the CDUSCC responds by either forcing the bus into high-impedance, placing a vector number, call instruction or zero on the data bus. The vector number can be modified or unmodified by the status. If no interrupt is pending, IACKN is ignored and the data bus placed in high-impedance.
X1/CLK	43	47	I	**Crystal or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, an external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals. When a crystal is used, a capacitor must be connected from this pin to ground.
X2	42	46	O	**Crystal 2:** Connection for other side of crystal. When a crystal is used, a capacitor must be connected from this pin to ground. If an external clock is used on X1, this pin should be left floating.
RESETN	23	25	I	**Master Reset:** Active-low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1 of the CDUSCC Users' Guide. Reset is asynchronous, i.e., no clock is required.
RxDA, RxDB	37, 12	40, 14	I	**Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	36, 13	39, 15	O	**Channel A (B) Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is in the marking (high) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	39, 10	43, 11	I/O	**Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X).
TRxCA, TRxCB	40, 9	44, 10	I/O	**Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X), or the internal system clock (X1 ÷ 2).

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
CTSA/BN, LCA/BN	32, 17	35, 19	I/O	**Channel A (B) Clear-to-Send Input or Loop Control Output:** Active-low. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The CDUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the BOP loop mode, this pin becomes a loop control output which is asserted and negated by CDUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.
DCDA/BN, SYNIA/BN	38, 11	42, 12	I	**Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-low input, it acts as an enable for the receiver or can be used as a general purpose input. For the DCD function, the CDUSCC detects logic level transitions on this pin and can be programmed to generate an interrupt when a transition occurs. As an active-low external sync input, it is used in COP mode to obtain character synchronization for the receiver without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in X.21.
RTxDRQA/BN, GPO1A/BN	34, 15	37, 17	O	**Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-low. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	36, 18	O	**Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-low. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to-Send output, which can be asserted and negated under program control.
RTxDAKA/BN, GPI1A/BN	44, 5	48, 5	I	**Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-low. For half-duplex single address operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO when the receiver is enabled or load transmitter FIFO when the transmitter is enabled) is beginning. For full-duplex single address DMA operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.
TxDAKA/BN, GPI2A/BN	35, 14	38, 16	I	**Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-low. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the CDUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.
EOPN	27	29	I/O	**Done (EOP):** Active-low, open-drain. EOPN can be used and is active in both DMA and non-DMA modes. As an input, EOPN indicates the last DMA transfer cycle to the TxFIFO. As an output, EOPN indicates either the last DMA transfer from the RxFIFO or that the transmitted character count has reached terminal count.
RTSA/BN, SYNOUTA/BN	41, 8	45, 9	O	**Channel A (B) Sync Detect or Request-to-Send:** Active-low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
V_{CC}	48	34, 52	I	**+5V Power Input**
GND	24	26, 13, 41, 7	I	**Signal and Power Ground Input**

CMOS Dual universal serial communications controller (CDUSCC) SC68C562

DESCRIPTION

The Philips Semiconductors SC68C562 Dual Universal Serial Communications Controller (CDUSCC) is a single-chip CMOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SC68C562 interfaces to the 68000 MPUs via asynchronous bus control signals and is capable of program-polled, interrupt driven, block-move or DMA data transfers.

The SC68C562 is hardware (pin) and software (Register) compatible with SCN68562 (NMOS version). It will automatically configure to NMOS DUSCC register map on power-up or reset.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides 16 common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock.

This makes the CDUSCC well suited for dual speed channel applications. Data rates up to 10Mb/s are supported.

Each transmitter and each receiver is serviced by a 16 byte FIFO. The receiver FIFO also stores 9 status bits for each character received; the transmit FIFO is able to store transmitter commands with each byte. This permits reading and writing of up to 16 bytes at a time, thus minimizing the

potential for transmitter underrun, receiver overrun and reducing interrupt or DMA overhead.

In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full. Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs are general purpose in nature, they can be optionally programmed for other functions. This document contains the electrical specifications for the SC68C562. Refer to the CMOS Dual Universal Serial Communications Controller (CDUSCC) User Manual for a complete operational description of this product.

FEATURES

- Full hardware and software upward compatibility with previous NMOS device

General Features

- Dual full-duplex synchronous/ asynchronous receiver and transmitter
- Low power CMOS process
- Multiprotocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: BISYNC, DDCMP
  - ASYNC: 5–8 bits plus optional parity
- Sixteen character receiver and transmitter FIFOs
- 0 to 10MHz data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 19 fixed rates: 50 to 64k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- and half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Compatible with the Philips Semiconductors SCB68430 Direct Memory Access Interface (DMAI) and other DMA controllers
  - Single- or dual-address dual transfers
  - Half- or full-duplex operation
  - Automatic frame termination on counter/timer terminal count or DMA DONE
- Transmit path clear status
- Interrupt capabilities
  - Daisy chain option
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Interrupt at any FIFO fill level
  - Maskable interrupt conditions
- FIFO'd status bits
- Watchdog timer
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general I/O pins per channel
  - CTS and DCD programmable auto-enables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments

- 1X or 16X Rx and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2-bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmits up to 10Mb/s at 1X and receive up to 1Mb/s at 16X data rates

Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK line fill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection

BISYNC Features

- EBCDIC or ASCII header, text and control messages
- SYN, DLE stripping
- EOM (end of message) detection and transmission
- Auto transparent mode switching
- Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
- Control character sequence detection for both transparent and normal text

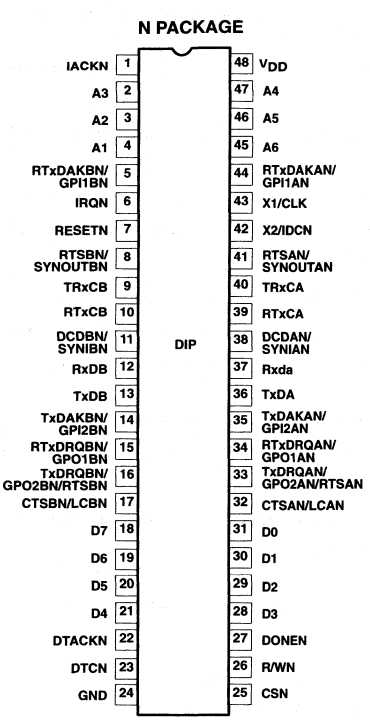
Bit-Oriented Protocol Features

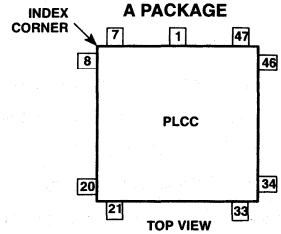
- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS FLAGs line fill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0 to +70°C Serial Data Rate = 10Mbps Maximum	V_{CC} = +5V ±10%, T_A = –40 to +85°C Serial Data Rate = 8Mbps Maximum	DWG #
48-Pin Plastic Dual In-Line Package (DIP)	SC68C562C1N	Not available	SOT240-1
52-Pin Plastic Leaded Chip Carrier (PLCC) Package	SC68C562C1A	SC68C562A8A	SOT238-3

PIN CONFIGURATIONS

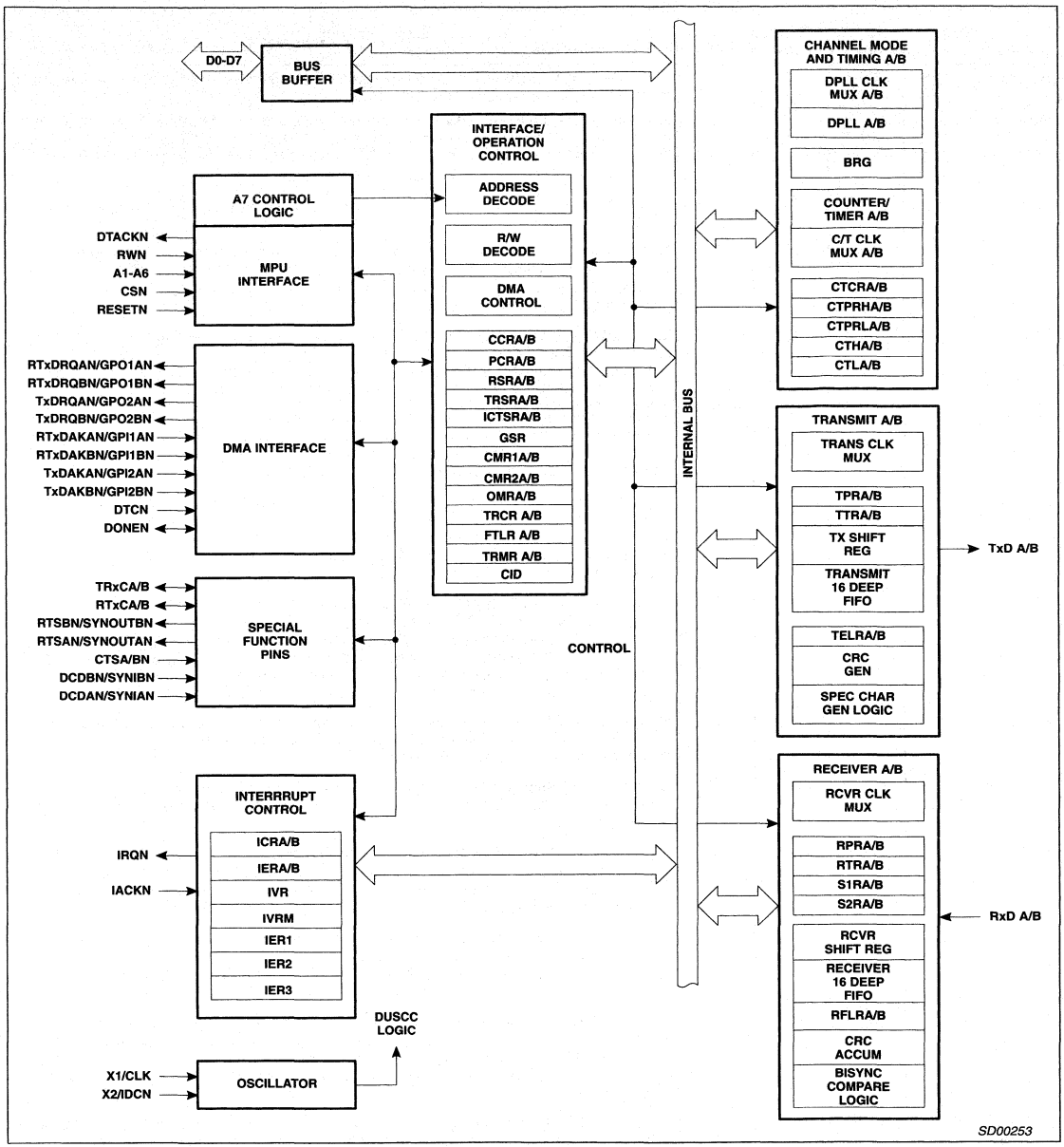




Pin	Function	Pin	Function
1	IACKN	27	CSN
2	A3	28	R/WN
3	A2	29	DONEN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
		32	D1
6	IRQN	33	D0
7	NC	34	NC
8	RESETN	35	CTSAN/LCAN
9	RTSBN/ SYNOUTBN	36	TxDRQAN/ GPO2AN/RTSAN
10	TRxCB	37	RTxDRQAN/ GPO1AN
11	RTxCB		
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
		44	TRxCA
18	TxDRQBN/ GPO2BN/RTSBN	45	RTSAN/ SYNOUTAN
19	CTSBN/LCBN	46	X2/IDCN
20	D7	47	X1/CLK
21	D6	48	RTxDAKAN/ GPI1AN
22	D5		
23	D4	49	A6
24	DTACKN	50	A5
25	DTCN	51	A4
26	GND	52	V_{DD}

SD00222

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A1–A6	4-2, 47-45	4-2, 51-49	I	**Address Lines:** Active-high. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0–D7	31-28, 21-18	33-30, 23-20	I/O	**Bidirectional Data Bus:** Active-high, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command and status transfers between the CPU and the CDUSCC take place over this bus. The data bus is enabled when CSN and R/WN or during interrupt acknowledge cycles and single address DMA acknowledge cycles.
R/WN	26	28	I	**Read/Write:** A high input indicates a read cycle and a low indicates a write cycle when CEN is active.
CSN	25	27	I	**Chip Select:** Active-low input. When active, data transfers between the CPU and the CDUSCC are enabled on D0–D7 as controlled by R/WN and A1–A6 inputs. When CSN is high, the data lines are placed in the 3-State condition (except during interrupt acknowledge cycles and single address DMA transfers).
IRQN	6	6	O	**Interrupt Request:** Active-low, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the CDUSCC to output an interrupt vector on the data bus.
IACKN	1	1	I	**Interrupt Acknowledge:** Active-low. When IACKN is asserted, the CDUSCC responds by either forcing the bus into high-impedance, placing a vector number, call instruction or zero on the data bus. The vector number can be modified or unmodified by the status. If no interrupt is pending, IACKN is ignored and the data bus placed in high-impedance.
X1/CLK	43	47	I	**Crystal or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, an external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals. When a crystal is used, a capacitor must be connected from this pin to ground.
X2/IDCN	42	46	O	**Crystal or Interrupt Daisy Chain:** When a crystal is used as the timing source, the crystal is connected between pins X1 and X2. This pin can be programmed to provide an interrupt daisy chain active-low output which propagates the IACKN signal to lower priority devices, if no active interrupt is pending. This pin should be left floating when an external clock is used on X1 and X2 is not used as an interrupt daisy chain output. When a crystal is used, a capacitor must be connected from this pin to ground.
RESETN	7	8	I	**Master Reset:** Active-low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1 of the CDUSCC Users' Guide. Reset is asynchronous, i.e., no clock is required.
RxDA, RxDB	37, 12	40, 14	I	**Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	36, 13	39, 15	O	**Channel A (B) Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is in the marking (high) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	39, 10	43, 11	I/O	**Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X).
TRxCA, TRxCB	40, 9	44, 10	I/O	**Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X), or the internal system clock (X1 ÷ 2).
CTSA/BN, LCA/BN	32, 17	35, 19	I/O	**Channel A (B) Clear-to-Send Input or Loop Control Output:** Active-low. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The CDUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the BOP loop mode, this pin becomes a loop control output which is asserted and negated by CDUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
DCDA/BN, SYNIA/BN	38, 11	42, 12	I	**Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-low input, it acts as an enable for the receiver or can be used as a general purpose input. For the DCD function, the CDUSCC detects logic level transitions on this pin and can be programmed to generate an interrupt when a transition occurs. As an active-low external sync input, it is used in COP mode to obtain character synchronization for the receiver without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in X.21.
RTxDRQA/BN, GPO1A/BN	34, 15	37, 17	O	**Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-low. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	36, 18	O	**Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-low. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to-Send output, which can be asserted and negated under program control.
RTxDAKA/BN, GPI1A/BN	44, 5	48, 5	I	**Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-low. For half-duplex single address operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO when the receiver is enabled or load transmitter FIFO when the transmitter is enabled) is beginning. For full-duplex single address DMA operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.
TxDAKA/BN, GPI2A/BN	35, 14	38, 16	I	**Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-low. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the CDUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.
DONEN	27	29	I/O	**Done:** Active-low, open-drain. DONEN can be used and is active in both DMA and non-DMA modes. As an input, DONEN indicates the last DMA transfer cycle to the TxFIFO. As an output, DONEN indicates either the last DMA transfer from the RxFIFO or that the transmitted character count has reached terminal count.
RTSA/BN, SYNOUTA/BN	41, 8	45, 9	O	**Channel A (B) Sync Detect or Request-to-Send:** Active-low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
DTACKN	22	24	O	**Data Transfer Acknowledge:** Active-low, 3-state. DTACKN is asserted on a write cycle to indicate that the data on the bus has been latched, and on a read cycle or interrupt acknowledge cycle to indicate valid data is on the bus. In a write bus cycle, input data is latched by the assertion (falling edge) of DTACKN or by the negation (rising edge) of CSN, whichever occurs first. The signal is negated when completion of the cycle is indicated by negation of CSN or IACKN input, and returns to the inactive state (3-state) a short period after it is negated. In single address DMA mode, input data is latched by the assertion (falling edge) of DTCN or by the negation (rising edge) of the DMA acknowledge input, whichever occurs first. DTACK is negated when completion of the cycle is indicated by the assertion of DTCN or negation of DMA acknowledge inputs (whichever occurs first), and returns to the inactive state (3-state) a short period after it is negated. When inactive, DTACKN requires an external pull-up resistor.
DTC	23	25	I	**Device Transfer Complete:** Active-low. DTCN is asserted by the DMA controller to indicate that the requested data transfer is complete.
V_{CC}	48	34, 52	I	**+5V Power Input**
GND	24	26, 13, 41, 7	I	**Signal and Power Ground Input**

Programmable communications interface (PCI) SCN2651

DESCRIPTION

The Philips Semiconductors SCN2651 PCI is a universal synchronous/asynchronous data communications controller chip designed for microcomputer systems. It interfaces directly to the Philips Semiconductors SCN2650 microprocessor and may be used in a polled or interrupt driven system environment. The SCN2651 accepts programmed instructions from the microprocessor and supports many serial data communication disciplines, synchronous and asynchronous, in the full or half-duplex mode.

The PCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The SCN2651 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode.

The PCI is constructed using Philips Semiconductors n-channel silicon gate depletion load technology and is packaged in a 28-pin DIP.

FEATURES

- Synchronous operation
  - 5- to 8-bit characters
  - Single or double SYN operation
  - Internal character synchronization
  - Transparent or non-transparent mode
  - Automatic SYN or DLE-SYN insertion
  - SYN or DLE stripping
  - Odd, even, or no parity
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps (1X clock)
- Asynchronous operation
  - 5- to 8-bit characters
  - 1, 1-1/2 or 2 stop bits
  - Odd, even, or no parity
  - Parity, overrun and framing error detection
  - Line break detection and generation
  - False start bit detection
  - Automatic serial echo mode
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps
    (1X clock)
    DC to 62.5kbps (16X clock)
    DC to 15.625kbps
    (64X clock)

PIN CONFIGURATIONS

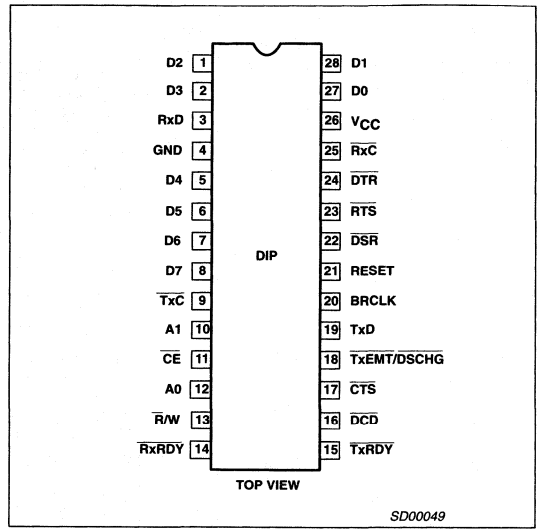


Figure 1. Pin Configurations

OTHER FEATURES

- Internal or external baud rate clock
- 16 internal rates – 50 to 19,200 baud
- Double buffered transmitter and receiver
- Full or half duplex operation
- TTL compatible inputs and outputs
- Single 5V power supply
- No system clock required
- 28-pin dual in-line package

APPLICATIONS

- Intelligent terminals
- Network processors
- Front-end processors
- Remote data concentrators
- Computer to computer links
- Serial peripherals

ORDERING CODE

PACKAGES	V_{CC} = 5V ±5%		DWG #
	Commercial 0°C to +70°C	Industrial -40°C to +85°C	
28-Pin Plastic Dual In-Line Package (DIP)	SCN2651CC1N28	Not available	SOT117-2

BLOCK DIAGRAM

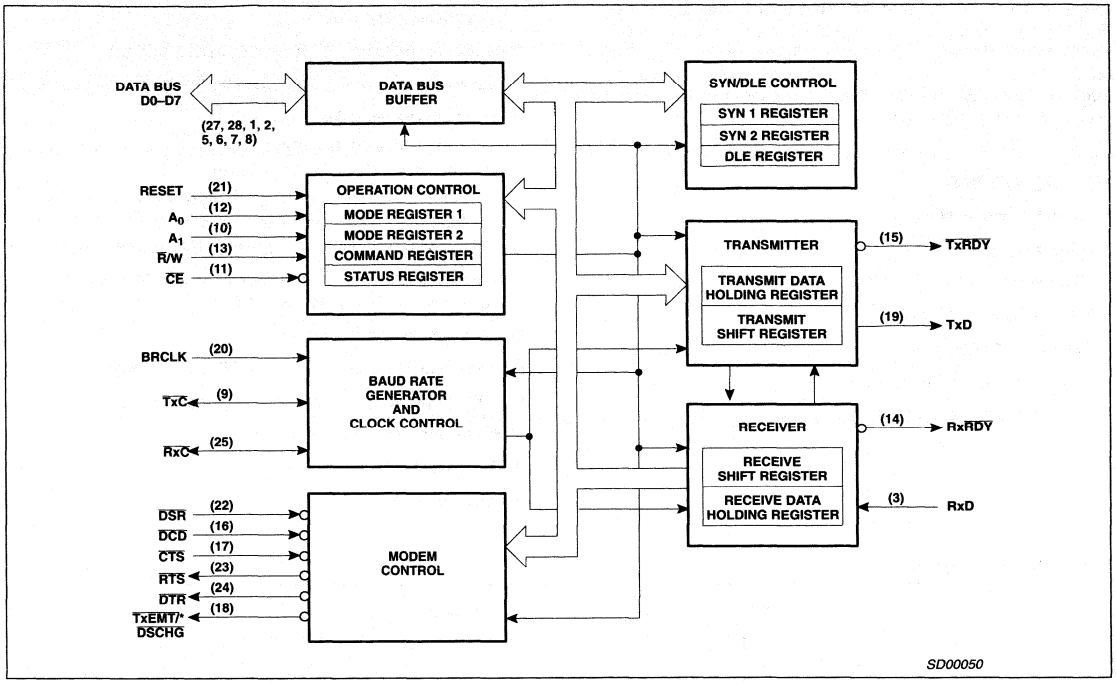


Figure 2. Block Diagram

PIN DESCRIPTION

Pin No.	Symbol	Name and Function	Type
27, 28, 1, 2, 5-8	D0 – D_7	8-Bit data bus	I/O
21	RESET	Reset	I
12, 10	A_0–A_1	Internal register select lines	I
13	R/W	Read or write command	I
11	CE	Chip enable input	I
22	DSR	Data set ready	I
24	DTR	Data terminal ready	O
23	RTS	Request to send	O
17	CTS	Clear to send	I
16	DCD	Data carrier detected	I
18	TxEMT/DSCHG	Transmitter empty or data set change	O
9	TxC	Transmitter clock	I/O
25	RxC	Receiver clock	I/O
19	TxD	Transmitter data	O
3	RxD	Receiver data	I
15	TxRDY	Transmitter ready	O
14	RxRDY	Receiver ready	O
20	BRCLK	Baud rate generator clock	I
26	V_{CC}	+5V supply	I
4	GND	Ground	I

Multi-protocol communications controller (MPCC) SCN2652/SCN68652

DESCRIPTION

The SCN2652/68652 Multi-Protocol Communications Controller (MPCC) is a monolithic n-channel MOS LSI circuit that formats, transmits and receives synchronous serial data while supporting bit-oriented or byte control protocols. The chip is TTL compatible, operates from a single +5V supply, and can interface to a processor with an 8 or 16-bit bidirectional data bus.

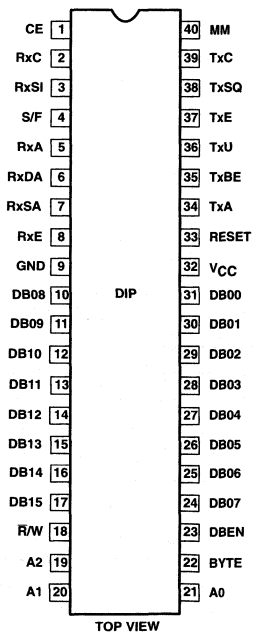
APPLICATIONS

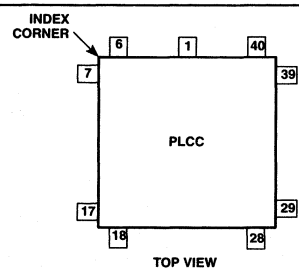
- Intelligent terminals
- Line controllers
- Network processors
- Front end communications
- Remote data concentrators
- Communication test equipment
- Computer to computer links

FEATURES

- DC to 2Mbps data rate
- Bit-oriented protocols (BOP): SDLC, ADCCP, HDLC
- Byte-control protocols (BCP): DDCMP, BISYNC (external CRC)
- Programmable operation
  - 8 or 16-bit tri-state data bus
  - Error control – CRC or VRC or none
  - Character length – 1 to 8 bits for BOP or 5 to 8 bits for BCP
  - SYNC or secondary station address comparison for BCP-BOP
  - Idle transmission of SYNC/FLAG or MARK for BCP-BOP
- Automatic detection and generation of special BOP control sequences, i.e., FLAG, ABORT, GA
- Zero insertion and deletion for BOP
- Short character detection for last BOP data character
- SYNC generation, detection, and stripping for BCP
- Maintenance mode for self-testing
- TTL compatible
- Single +5V supply

PIN CONFIGURATION





Pin	Function	Pin	Function
1	NC	23	NC
2	CE	24	A0
3	RxC	25	BYTE
4	RxSI	26	DBEN
5	S/F	27	DB07
6	RxA	28	DB06
7	RxDA	29	DB05
8	RxSA	30	DB04
9	RxE	31	DB03
10	GND	32	DB02
11	DB08	33	DB01
12	NC	34	NC
13	DB09	35	DB00
14	DB10	36	V_{CC}
15	DB11	37	RESET
16	DB12	38	TxA
17	DB13	39	TxBE
18	DB14	40	TxU
19	DB15	41	TxE
20	R/W	42	TxSQ
21	A2	43	TxC
22	A1	44	MM

NOTE: DB00 is least significant bit, highest number (that is, DB15, A2) is most significant bit.

SD00057

Figure 1. Pin Configuration

ORDERING CODE

PACKAGES	V_{CC} = 5V ±5%		DWG #
	Commercial 0°C to +70°C	Industrial -40°C to +85°C	
40-Pin Ceramic Dual In-Line Package (DIP)	SCN2652AC2F40 / SCN68652AC2F40		0590B
40-Pin Plastic Dual In-Line Package (DIP)	SCN2652AC2N40 / SCN68652AC2N40	Contact Factory	SOT129-1
44-Pin Square Plastic Lead Chip Carrier (PLCC)	SCN2652AC2A44 / SCN68652AC2A44	Contact Factory	SOT187-2

BLOCK DIAGRAM

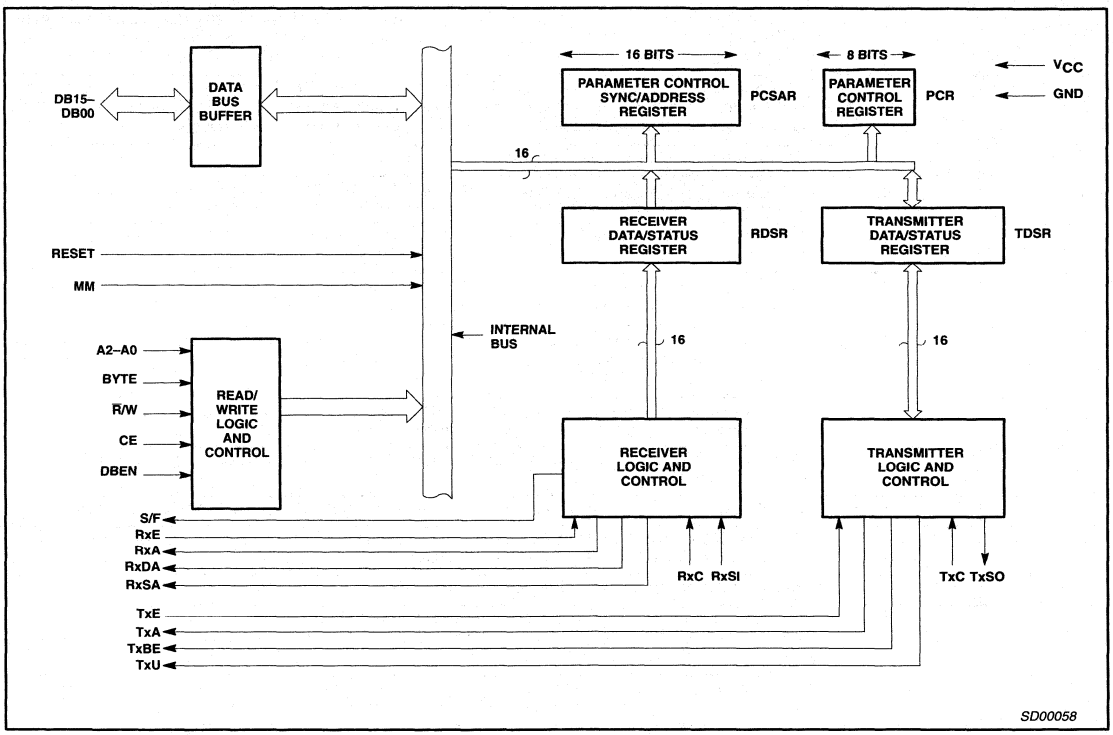


Figure 2. Block Diagram

PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
DB15–DB00	17–10 24–31	I/O	**Data Bus:** DB07–DB00 contain bidirectional data while DB15–DB08 contain control and status information to or from the processor. Corresponding bits of the high and low order bytes can be wire OR'ed onto an 8-bit bus. The data bus is floating if either CE or DBEN are low.
A2–A0	19–21	I	**Address Bus:** A2–A0 select internal registers. The four 16-bit registers can be addressed on a word or byte basis. See Register Address section.
BYTE	22	I	**Byte:** Single byte (8-bit) data bus transfers are specified when this input is high. A low level specifies 16-bit data bus transfers.
CE	1	I	**Chip Enable:** A high input permits a data bus operation when DBEN is activated.
$\overline{R}$/W	18	I	**Read/Write:** $\overline{R}$/W controls the direction of data bus transfer. When high, the data is to be loaded into the addressed register. A low input causes the contents of the addressed register to be presented on the data bus.
DBEN	23	I	**Data Bus Enable:** After A2–A0, CE, BYTE and $\overline{R}$/W are set up, DBEN may be strobed. During a read, the 3-state data bus (DB) is enabled with information for the processor. During a write, the stable data is loaded into the addressed register and TxBE will be reset if TDSR was addressed.
RESET	33	I	**Reset:** A high level initializes all internal registers (to zero) and timing.
MM	40	I	**Maintenance Mode:** MM internally gates TxSO back to RxSI and TxC to RxC for off line diagnostic purposes. The RxC and RxSI inputs are disabled and TxSO is high when MM is asserted.
RxE	8	I	**Receiver Enable:** A high level input permits the processing of RxSI data. A low level disables the receiver logic and initializes all receiver registers and timing.
RxA	5	O	**Receiver Active:** RxA is asserted when the first data character of a message is ready for the processor. In the BOP mode this character is the address. The received address must match the secondary station address if the MPCC is a secondary station. In BCP mode, if strip-SYNC ($PCSAR_{13}$) is set, the first non-SYNC character is the first data character; if strip-SYNC is zero, the character following the second SYNC is the first data character. In the BOP mode, the closing FLAG resets RxA. In the BCP mode, RxA is reset by a low level at RxE.
RxDA*	6	O	**Receiver Data Available:** RxDA is asserted when an assembled character is in $RDSR_L$ and is ready to be presented to the processor. This output is reset when $RDSR_L$ is read.
RxC	2	I	**Receiver Clock:** RxC (1X) provides timing for the receiver logic. The positive going edge shifts serial data into the RxSR from RxSI.
S/F	4	O	**SYNC/FLAG:** S/F is asserted for one RxC clock time when a SYNC or FLAG character is detected.
RxSA*	7	O	**Receiver Status Available:** RxSA is asserted when there is a zero to one transition of any bit in $RDSR_H$ except for RSOM. It is cleared when $RDSR_H$ is read.
RxSI	3	I	**Receiver Serial Input:** RxSI is the received serial data. Mark = '1', space = '0'.
TxE	37	I	**Transmitter Enable:** A high level input enables the transmitter data path between $TDSR_L$ and TxSO. At the end of a message, a low level input causes TxSO = 1(mark) and TxA = 0 after the closing FLAG (BOP) or last character (BCP) is output on TxSO.
TxA	34	O	**Transmitter Active:** TxA is asserted after TSOM ($TDSR_8$) is set and TxE is raised. This output will reset when TxE is low and the closing FLAG (BOP) or last character (BCP) has been output on TxSO.
TxBE*	35	O	**Transmitter Buffer Empty:** TxBE is asserted when theTDSR is ready to be loaded with new control information or data. The processor should respond by loading theTDSR which resets TxBE.
TxU*	36	O	**Transmitter Underrun:** TxU is asserted during a transmit sequence when the service of TxBE has been delayed for one character time. This indicates the processor is not keeping up with the transmitter. Line fill depends on $PCSAR_{11}$. TxU is reset by RESET or setting of TSOM ($TDSR_8$), synchronized by the falling edge of TxC.
TxC	39	I	**Transmitter Clock:** TxC (1X) provides timing for the transmitter logic. The positive going edge shifts data out of the TxSR to TxSO.
TxSO	38	O	**Transmitter Serial Output:** TxSO is the transmitted serial data. Mark = '1', space = '0'.
V_{CC}	32	I	**+5V:** Power supply.
GND	9	I	**Ground:** 0V reference ground.

*Indicates possible interrupt signal

Dual universal serial communications controller (DUSCC) SCN26562

DESCRIPTION

The Philips Semiconductors SCN26562 Dual Universal Serial Communications Controller (DUSCC) is a single-chip MOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SCN26562 interfaces to synchronous bus MPUs and is capable of program-polled, interrupt driven, block-move or DMA data transfers.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multi-function counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides 16 common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4Mbits per second are supported.

The transmitter and receiver each contain a four-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to four characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

This document contains the electrical specifications for the SCN26562. See SCN26562/SCN68562 User's Guide for complete functional description.

FEATURES

General Features

- Dual full-duplex synchronous/asynchronous receiver and transmitter
- Multiprotocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: BISYNC, DDCMP
  - ASYNC: 5–8 bits plus optional parity
- Four character receiver and transmitter FIFOs
- 0 to 4Mbit/sec data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 16 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- and half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Single- or dual-address dual transfers
  - Half- or full-duplex operation
  - Automatic frame termination on counter/timer terminal count or DMA EOPN input
- Interrupt capabilities
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Maskable interrupt conditions
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general purpose pins per channel
  - CTS and DCD programmable auto-enables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2-bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmits up to 4Mbit/sec data rate Receives up to 2Mbit/sec data rate

Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK line-fill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection

BISYNC Features

- EBCDIC or ASCII header, text and control messages
- SYN, DLE stripping
- EOM (end of message) detection and transmission
- Auto transparent mode switching
- Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
- Control character sequence detection for both transparent and normal text

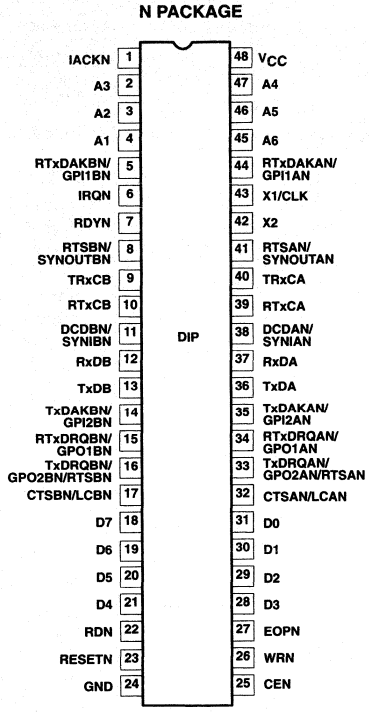
Bit-Oriented Protocol Features

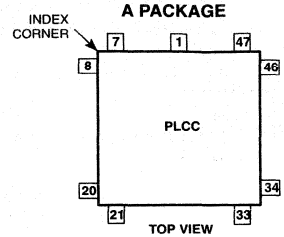
- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and detection
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS FLAGs line-fill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±5%, T_A = 0°C to +70°C Serial Data Rate = 4Mbps Maximum	DWG #
48-Pin Plastic Dual In-Line Package (DIP)	SCN26562C4N48	SOT240-1
52-Pin Plastic Leaded Chip Carrier (PLCC) Package	SCN26562C4A52	SOT238-3

PIN CONFIGURATIONS





PIN	FUNCTION	PIN	FUNCTION
1	IACKN	27	CEN
2	A3	28	WRN
3	A2	29	EOPN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
6	IRQN	32	D1
7	NC	33	D0
8	RDYN	34	NC
9	RTSBN/ SYNOUTBN	35	CTSAN/LCAN
10	TRxCB	36	TxDRQAN/ GPO2AN/RTSAN
11	RTxCB	37	RTxDRQAN/ GPO1AN
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
18	TxDRQBN/ GPO2BN/RTSBN	44	TRxCA
19	CTSBN/LCBN	45	RTSAN/ SYNOUTAN
20	D7	46	X2
21	D6	47	X1/CLK
22	D5	48	RTxDAKAN/ GPI1AN
23	D4	49	A6
24	RDN	50	A5
25	RESETN	51	A4
26	GND	52	V_{CC}

SD00203

Figure 1. Pin Configurations

BLOCK DIAGRAM

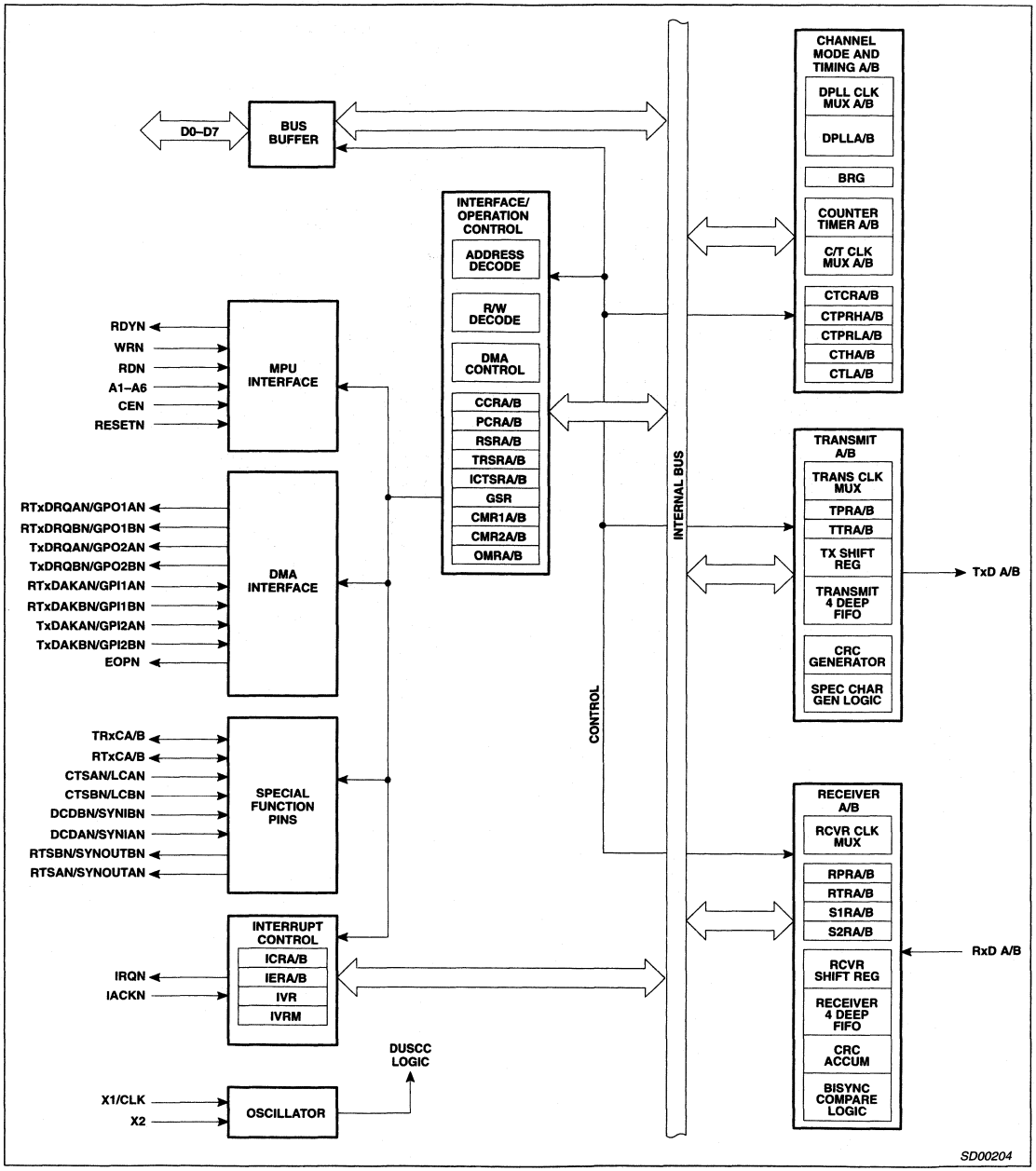


Figure 2. Block Diagram

PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A1–A6	4–2, 47–45	4–2, 51–49	I	Address lines.
D0–D7	31–28, 21–18	33–30, 23–20	I/O	Bidirectional data bus.
RDN	22	24	I	Read strobe.
WRN	26	28	I	Write strobe.
CEN	25	27	I	Chip select.
RDYN	7	8	O	Ready.
IRQN	6	6	O	Interrupt request.
IACKN	1	1	I	Interrupt acknowledge.
X1/CLK	43	47	I	Crystal 1 or external clock.
X2	42	46	I	Crystal 2.
RESETN	23	25	I	Master reset.
RxDA, RxDB	37, 12	40, 14	I	Channel A (B) receiver serial data.
TxDA, TxDB	36, 13	39, 15	O	Channel A (B) transmitter serial data.
RTxCA, RTxCB	39, 10	43, 11	I/O	Channel A (B) receiver/transmitter clock.
TRxCA, TRxCB	40, 9	44, 10	I/O	Channel A (B) transmitter/receiver clock.
CTSA/BN, LCA/BN	32, 17	35, 19	I/O	Channel A (B) clear-to-send input or loop control output.
DCDA/BN, SYNIA/BN	38, 11	42, 12	I	Channel A (B) data carrier detected or external sync.
RTxDRQA/BN, GPO1A/BN	34, 15	37, 17	O	Channel A (B) receiver/transmitter DMA service request or general purpose output.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	36, 18	O	Channel A (B) transmitter DMA service request, general purpose output or request-to-send.
RTxDAKA/BN, GPI1A/BN	44, 5	48, 5	I	Channel A (B) receiver/transmitter DMA acknowledge or general purpose input 1.
TxDAKA/BN, GPI2A/BN	35, 14	38, 16	I	Channel A (B) transmitter DMA acknowledge or general purpose input 2.
EOPN	27	29	I/O	DMA transfer complete.
RTSA/BN, SYNOUTA/BN	41, 8	45, 9	O	Channel A (B) request-to-send or Sync detect.
V_{CC}	48	52	I	Power input.
GND	24	26	I	Signal and power ground.

Enhanced programmable communications interface (EPCI) SCN2661/SCN68661

DESCRIPTION

The Philips Semiconductors SCN2661 EPCI is a universal synchronous/asynchronous data communications controller chip that is an enhanced version of the SCN2651. It interfaces easily to all 8-bit and 16-bit microprocessors and may be used in a polled or interrupt driven system environment. The SCN2661 accepts programmed instructions from the microprocessor while supporting many serial data communications disciplines —synchronous and asynchronous — in the full- or half-duplex mode. Special support for BISYNC is provided.

The EPCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The SCN2661 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. Each version of the EPCI (A, B, C) has a different set of baud rates.

FEATURES

- Synchronous operation
  - 5- to 8-bit characters plus parity
  - Single or double SYN operation
  - Internal or external character synchronization
  - Transparent or non-transparent mode
  - Transparent mode DLE stuffing (Tx) and detection (Rx)
  - Automatic SYN or DLE-SYN insertion SYN, DLE and DLESYN stripping
  - Odd, even, or no parity
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps (1X clock)
- Asynchronous operation
  - 5- to 8-bit characters plus parity
  - 1, 1-1/2 or 2 stop bits transmitted
  - Odd, even, or no parity
  - Parity, overrun and framing error detection
  - Line break detection and generation
  - False start bit detection
  - Automatic serial echo mode (echoplex)
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps
    (1X clock)
    DC to 62.5kbps (16X clock)
    DC to 15.625kbps
    (64X clock)

OTHER FEATURES

- Internal or external baud rate clock
- 3 baud rate sets
- 16 internal rates for each set
- Double-buffered transmitter and receiver

PIN CONFIGURATIONS

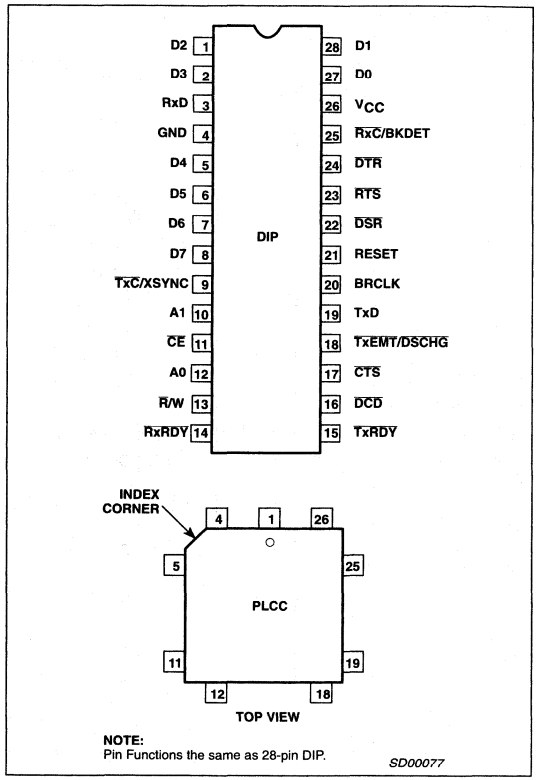


Figure 1. Pin Configurations

- Dynamic character length switching
- Full- or half-duplex operation
- TTL compatible inputs and outputs
- RxC and TxC pins are short-circuit protected
- Single +5V power supply
- No system clock required

APPLICATIONS

- Intelligent terminals
- Network processors
- Front-end processors
- Remote data concentrators
- Computer-to-computer links
- Serial peripherals
- BISYNC adaptors

ORDERING CODE

PACKAGES	V_{CC} = +5V ±5%		DWG #
	Commercial 0°C to +70°C	Industrial -40°C to +85°C	
28-Pin Ceramic Dual In-Line Package (cerdip) 0.6" Wide	SCN2661BC1F28 SCN2661CC1F28	SCN2661BA1F28 SCN2661CA1F28	0589B
28-Pin Plastic Dual In-Line Package (DIP) 0.6" Wide	SCN2661AC1N28 SCN2661BC1N28 SCN2661CC1N28	Contact Factory	SOT117-2
28-Pin Plastic Lead Chip Carrier (PLCC)	SCN2661AC1A28 SCN2661BC1A28 SCN2661CC1A28	Contact Factory	SOT261-3

BLOCK DIAGRAM

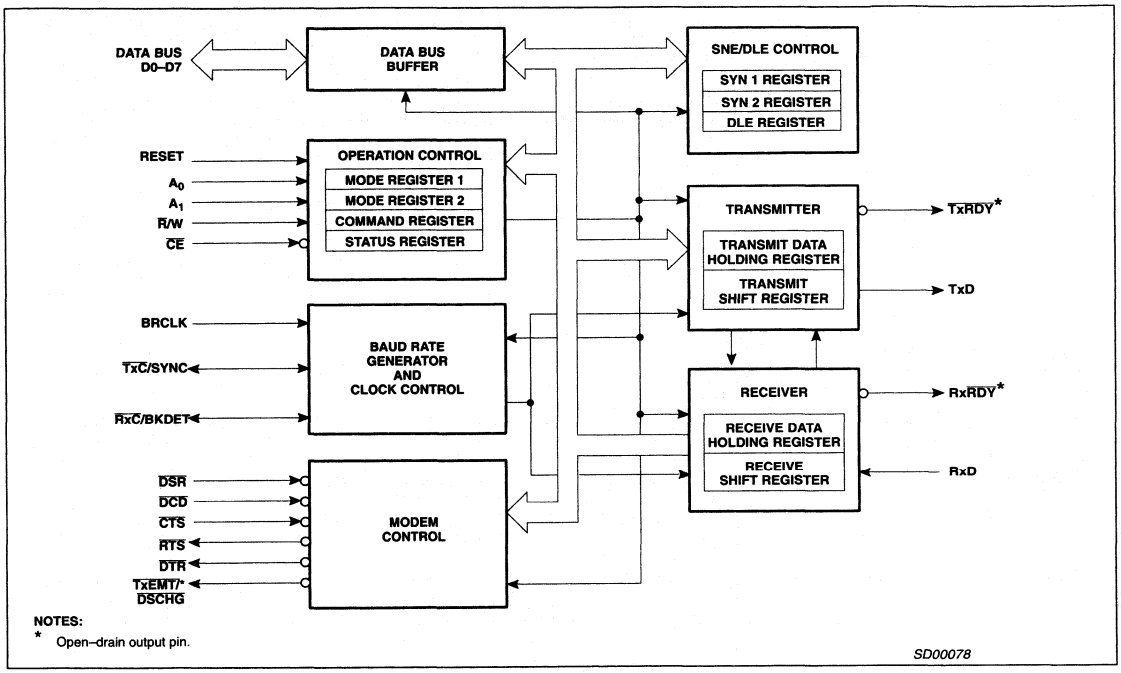


Figure 2. Block Diagram

Table 1. CPU-Related Signals

PIN NAME	PIN NO.	INPUT/ OUTPUT	FUNCTION
RESET	21	I	A High on this input performs a master reset on the 68661. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
A0, A1	12,10	I	Address lines used to select internal EPCI registers.
R/W	13	I	Read command when Low, write command when High.
CE	11	I	Chip enable command. When Low, indicates that control and data lines to the EPCI are valid and that the operation specified by the R/W, A1 and A0 inputs should be performed. When High, places the D0–D7 lines in the 3-State condition.
D0–D7	27,28,1,2,5–8	I/O	8-bit, 3-State data bus used to transfer commands, data and status between EPCI and the CPU. D0 is the least significant bit, D7 the most significant bit.
TxRDY	15	O	This output is the complement of status register bit SR0. When Low, it indicates that the transmit data holding register (THR) is ready to accept a data character from the CPU. It goes High when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open-drain output which can be used as an interrupt to the CPU.
RxRDY	14	O	This output is the complement of status register bit SR1. When Low, it indicates that the receive data holding register (RHR) has a character ready for input to the CPU. It goes High when the RHR is read by the CPU, and also when the receiver is disabled. It is an open-drain output which can be used as an interrupt to the CPU.
TxEMT/DSCHG	18	O	This output is the complement of status register bit SR2. When Low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the DSR or DCD inputs has occurred. This output goes High when the status register is ready by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open-drain output which can be used as an interrupt to the CPU. See Status Register (SR2) for details.

Table 2. Device-Related Signals

PIN NAME	PIN NO.	INPUT/ OUTPUT	FUNCTION
BRCLK	20	I	Clock input to the internal baud rate generator (see Table 1, included in CD-ROM version). Not required if external receiver and transmitter clocks are used.
RxC/BKDET	25	I/O	Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin can be a 1X/16X clock or a break detect output pin.
TxC/XSYNC	9	I/O	Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, this pin can be a 1X/16X clock output or an external jam synchronization input.
RxD	3	I	Serial data input to the receiver. "Mark" is High, "space" is Low.
TxD	19	O	Serial data output from the transmitter. "Mark" is High, "Space" is Low. Held in mark condition when the transmitter is disabled.
DSR	22	I	General purpose input which can be used for data set ready or ring indicator condition. Its complement appears as status register bit SR7. Causes a Low output on TxEMT/DSCHG when its state changes if CR2 or CR0 = 1.
DCD	16	I	Data carrier detect input. Must be Low in order for the receiver to operate. Its complement appears as status register bit SR6. Causes a Low output on TxEMT/DSCHG when its state changes if CR2 or CR0 = 1. If DCD goes High while receiving, the RxC is internally inhibited.
CTS	17	I	Clear to send input. Must be Low in order for the transmitter to operate. If it goes High during transmission, the character in the transmit shift register will be transmitted before termination.
DTR	24	O	General purpose output which is the complement of command register bit CR1. Normally used to indicate data terminal ready.
RTS	23	O	General purpose output which is the complement of command register bit CR5. Normally used to indicate request to send. See Command Register (CR5) for details.

Dual universal serial communications controller (DUSCC) SCN68562

DESCRIPTION

The Philips Semiconductors SCN68562 Dual Universal Serial Communications Controller (DUSCC) is a single-chip MOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SCN68562 interfaces to the 68000 MPUs via asynchronous bus control signals and is capable of program-polled, interrupt driven, block-move or DMA data transfers. The operating mode and data format of each channel can be programmed independently.

Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides 16 common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4Mbits per second are supported.

The transmitter and receiver each contain a four-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to four characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs are provided. These inputs and outputs can be optionally programmed for other functions.

FEATURES

General Features

- Dual full-duplex synchronous/asynchronous receiver and transmitter
- Multiprotocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: BISYNC, DDCMP
  - ASYNC: 5–8 bits plus optional parity
- Four character receiver and transmitter FIFOs

PIN CONFIGURATIONS

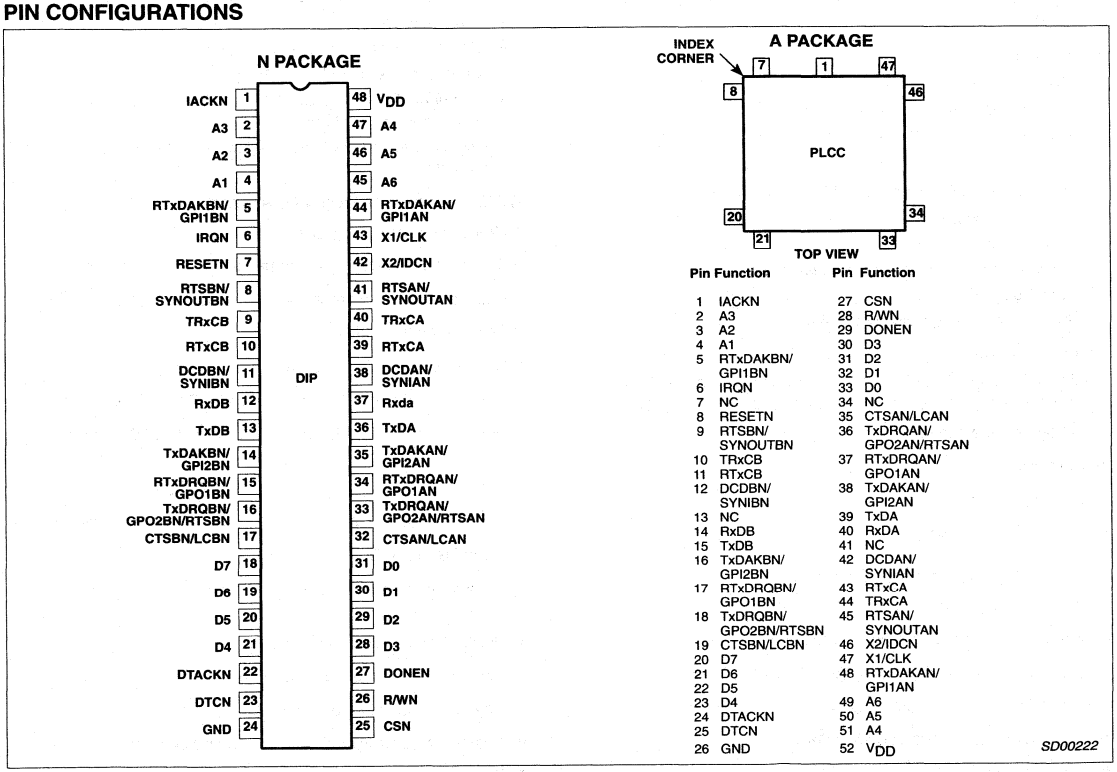


Figure 1. Pin Configurations

- 0 to 4MHz data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 16 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- and half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Compatible with the Philips Semiconductors SCB68430 Direct Memory Access Interface (DMAI) and other DMA controllers
  - Single- or dual-address dual transfers
  - Half- or full-duplex operation
  - Automatic frame termination on counter/timer terminal count or DMA DONE
- Interrupt capabilities
  - Daisy chain option
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Maskable interrupt conditions
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general I/O pins per channel
  - CTS and DCD programmable autoenables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X Rx and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2-bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmits up to 4Mbs and receive up to 2Mbps data rates

Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK line-fill on underrun
- Idle in MARK or SYNs
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BISYNC Features

- EBCDIC or ASCII header, text and control messages
- SYN, DLE stripping
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- Auto transparent mode switching
- Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
- Control character sequence detection for both transparent and normal text

Bit-Oriented Protocol Features

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for 1 field
- Zero insertion and deletion
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- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS FLAGs line-fill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±5%, T_A = 0°C to +70°C Serial Data Rate = 4Mbps Maximum	DWG #
48-Pin Plastic Dual In-Line Package (DIP)	SCN68562C4N48	SOT240-1
52-Pin Plastic Leaded Chip Carrier (PLCC) Package	SCN68562C4A52	SOT238-3

NOTE: See SCN26562/SCN68562 User's Guide for detailed description of all the features.

BLOCK DIAGRAM

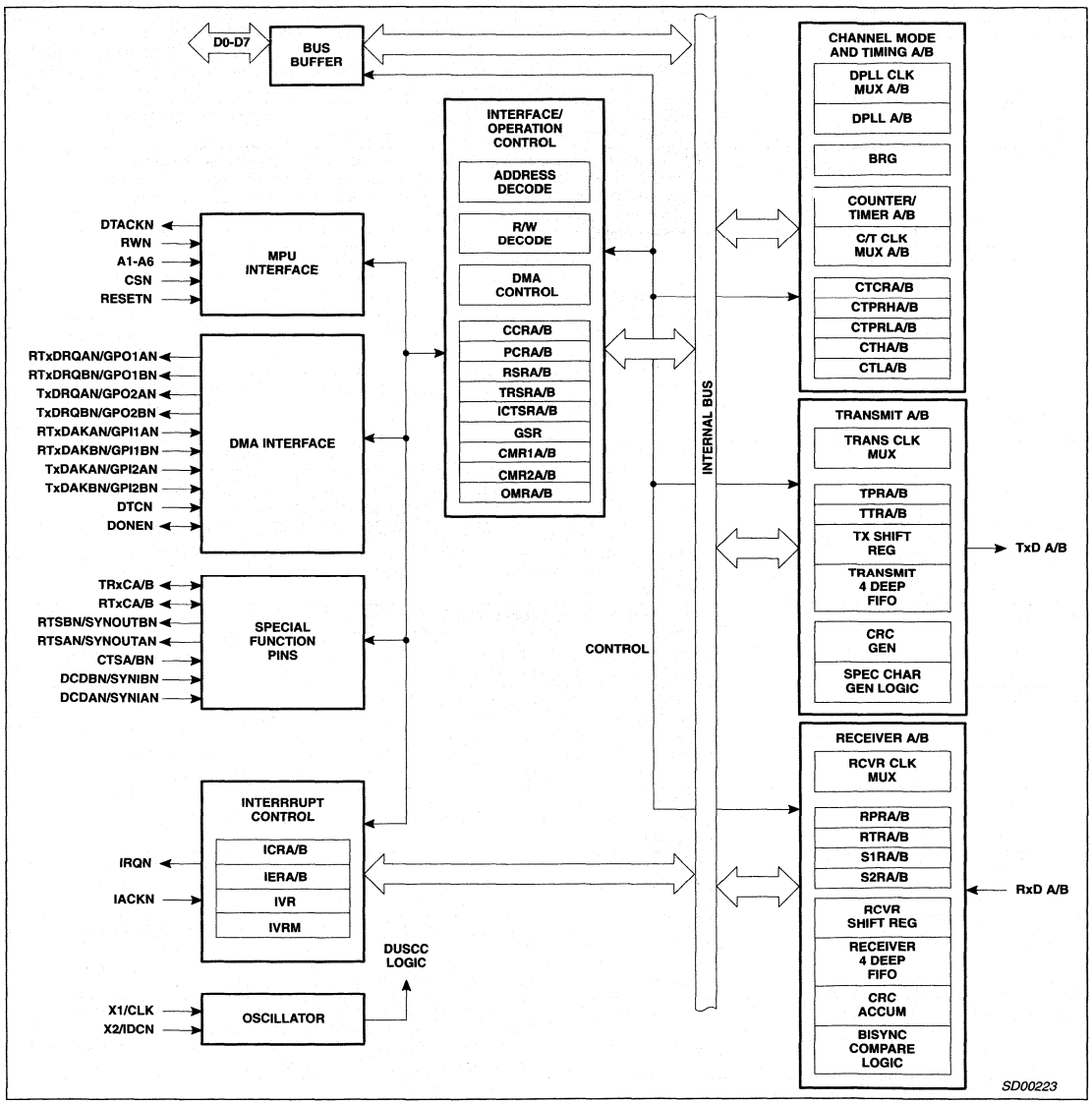


Figure 2. Block Diagram

PIN DESCRIPTION

In this data sheet, signals are discussed using the terms 'active' and 'inactive' or 'asserted' and 'negated' independent of whether the signal is active in the High (logic 1) or Low (logic 0) state. N at the end of a pin name signifies the signal associated with the pin is active-Low (see individual pin description for the definition of the active level of each signal.) Pins which are provided for both channels are designated by A/B after the name of the pin and the active-Low state indicator, N, if applicable. A similar method is used for registers provided for both channels: these are designated by either an underline or by A/B after the name.

MNEMONIC	DIP PIN NO.	TYPE	NAME AND FUNCTION
A1 – A6	4-2, 45-47	I	**Address Lines:** Active-High. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0 – D7	31-28, 21-18	I/O	**Bidirectional Data Bus:** Active High, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the DUSCC take place over this bus. The data bus is enabled when CSN is Low, during interrupt acknowledge cycles and single-address DMA acknowledge cycles.
R/WN	26	I	**Read/Write:** A High input indicates a read cycle and a Low input indicates a write cycle when a cycle is initiated by assertion of the CSN input.
CSN	25	I	**Chip Select:** Active-Low input. When Low, data transfers between the CPU and the DUSCC are enabled on D0 – D7 as controlled by the R/WN and A1 – A6 inputs. When CSN is High, the DUSCC is isolated from the data bus (except during interrupt acknowledge cycles and single-address DMA transfers) and D0 – D7 are placed in the 3-State condition.
DTACKN	22	O	**Data Transfer Acknowledge:** Active-Low, 3-State. DTACKN is asserted on a write cycle to indicate that the data on the bus has been latched, and on a read cycle or interrupt acknowledge cycle to indicate valid data is on the bus. The signal is negated when completion of the cycle is indicated by negation of the CSN or IACKN input, and returns to the inactive state (3-State) a short period after it is negated. In a single address DMA mode, data is latched with the falling edge of DTCN. DTACKN is negated when completion of the cycle is indicated by the assertion of DTCN or negation of DMA acknowledge inputs (whichever occurs first), and returns to the inactive state (3-State) a short period after it is negated. When negated, DTACKN becomes an open-drain output and requires an external pull-up resistor.
IRQN	6	O	**Interrupt Request:** Active-Low, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the DUSCC to output an interrupt vector on the data bus.
IACKN	1	I	**Interrupt Acknowledge:** Active-Low. When IACKN is asserted, the DUSCC responds by placing the contents of the interrupt vector register (modified or unmodified by status) on the data bus and asserting DTACKN. If no active interrupt is pending, DTACKN is not asserted.
X1/CLK	43	I	**Crystal or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, and external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals.
X2/IDCN	42	O	**Crystal or Interrupt Daisy Chain:** When a crystal is used as the timing source, the crystal is connected between pins X1 and X2. This pin can be programmed to provide and interrupt daisy chain active-Low output which propagates the IACKN signal to lower priority devices, if no active interrupt is pending. This pin should be grounded when an external clock is used on X1 and X2, is not used as an interrupt daisy chain output.
RESETN	7	I	**Master Reset:** Active-Low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1 of the CDUSCC Users' Guide. Reset in asynchronous, i.e., no clock is required.
RxDA, RxDB	37, 12	I	**Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	36, 13	O	**Channel A (B) Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the marking (High) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	39, 10	I/O	**Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X). The maximum external receiver/transmitter clock frequency is 4MHz.

PIN DESCRIPTION (Continued)

MNEMONIC	DIP PIN NO.	TYPE	NAME AND FUNCTION
TRxCA, TRxCB	40, 9	I/O	**Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X), or the internal system clock (X1/2). The maximum external receiver/transmitter clock frequency is 4MHz.
CTSA/BN, LCA/BN	32, 17	I/O	**Channel A (B) Clear-To-Send Input or Loop Control Output:** Active-Low. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the COP loop mode, this pin becomes a loop control output which is asserted and negated by DUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.
DCDA/BN, SYNIA/BN	38, 11	I	**Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-Low input, it acts as an enable for the receiver or can be used as a general purpose input for the DCD function, the DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. As an active-Low external sync input, it is used in COP modes to obtain character synchronization without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in X.21.
RTxDRQA/BN, GPO1A/BN	34, 15	O	**Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-Low. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	O	**Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-Low. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to -Send output, which can be asserted and negated under program control (see Detailed Operation).
RTxDAKA/BN, GPI1A/BN	44, 5	I	**Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-Low. For half-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO or load transmitter FIFO) is beginning. For full-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.
TxDAKA/BN, GP12A/BN	35, 14	I	**Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-Low. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the DUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.
DTCN	23	I	**Device Transfer Complete:** Active-Low. DTCN is asserted by the DMA controller to indicate that the requested data transfer is complete.
DONEN	27	I/O	**Done:** Active-Low, open-drain. See Detailed Operation for a description of the function of this pin.
RTSA/BN, SYNOUTA/BN	41, 8	O	**Channel A (B) Sync Detect or Request-to-Send:** Active-Low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
V_{DD}	48	I	+5V ± 10% power input.
GND	24	I	Signal and power ground input.

Section 4
Line Drivers Receivers/Modems

CONTENTS

MC145406 EIA-232-D/V.28 driver/receiver 165

EIA-232-D/V.28 driver/receiver | MC145406

DESCRIPTION

The MC145406 is a silicon-gate CMOS IC that combines 3 drivers and 3 receivers to fulfill the electrical specifications of standards EIA-232-D and CCITT V.28. The drivers feature true TTL input compatibility, slew-rate limited output, 300Ω power-off source impedance, and output typically switching to within 25% of the supply rails. The receivers can handle up to ±25V while presenting 3 to 7kΩ impedance. Hysteresis in the receiver aids reception of noisy signals. By combining both drivers and receivers in a single CMOS chip, the MC145406 provides efficient, low-power solutions for EIA-232-D and V.28 applications.

APPLICATIONS

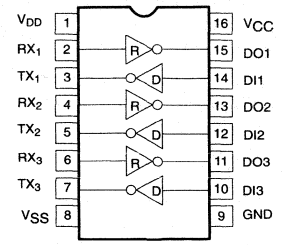
- Modem interface
- Voice/data telephone interface
- Lap-top computers
- UART interface

FEATURES

- **Drivers**
- ±5 to ±12V supply range
- 300Ω power-off source impedance
- Output current limiting
- TTL compatible
- Maximum slew rate = 30V/µs

PIN CONFIGURATION

D and N Packages



NOTE:
D = Driver
R = Receiver

SL00057

Figure 1. Pin Configuration

- **Receivers**
- ±25V input voltage range over the full supply range
- 3 to 7kΩ input impedance
- Hysteresis on input switchpoint
- **General**
- Very low supply currents for long battery life
- Operation is independent of power supply sequencing

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line (DIP) Package	0 to +70°C	MC145406N	SOT38-4
16-Pin Small Outline Large (SOL) Package	0 to +70°C	MC145406D	SOT162-1

BLOCK DIAGRAM

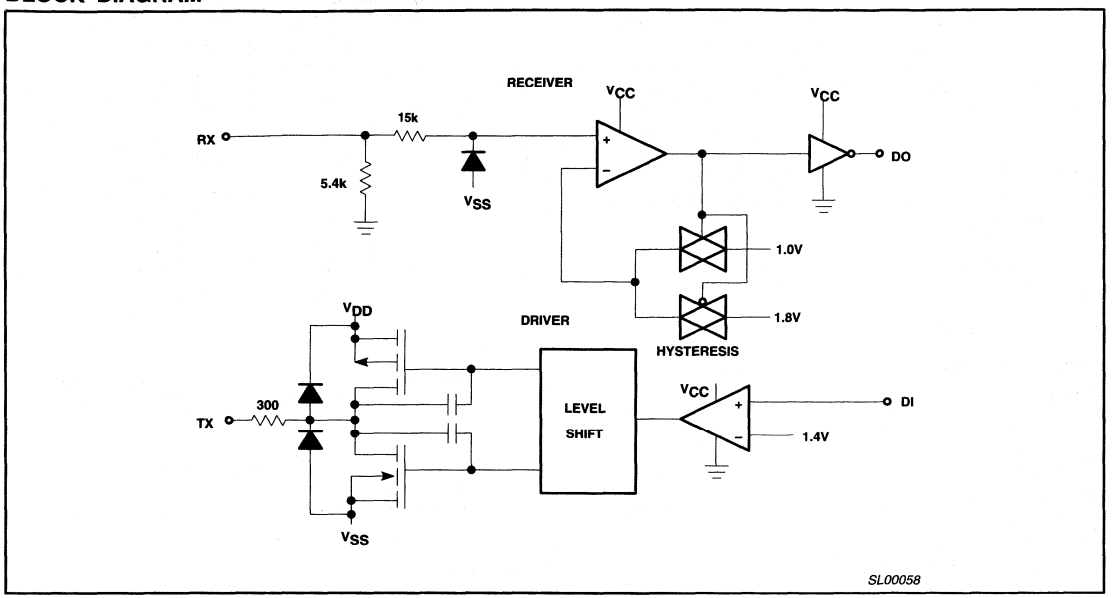


Figure 2. Block Diagram

PIN #	SYMBOL	PIN DESCRIPTION
1	V_{DD}	**Positive power supply.** The most positive power supply pin, which is typically 5 to 12 volts.
8	V_{SS}	**Negative power supply.** The most negative power supply pin, which is typically -5 to -12 volts.
16	V_{CC}	**Digital power supply.** The digital supply pin, which is connected to the logic power supply (maximum +5.5V).
9	GND	**Ground.** Ground return pin is typically connected to the signal ground pin of the EIA-232-D connector (Pin 7) as well as to the logic power supply ground.
2, 4, 6	RX_1, RX_2, RX_3	**Receive Data Input.** These are the EIA-232-D receive signal inputs whose voltages can range from +25 to -25V. A voltage between +3 and +25 is decoded as a space and causes the corresponding DO pin to swing to ground (0V); a voltage between -3 and -25V is decoded as a mark and causes the DO pin to swing up to V_{CC}. The actual turn-on input switchpoint is typically biased at 1.8V above ground, and includes 800mV of hysteresis for noise rejection. The nominal input impedance is 5kΩ. An open or grounded input pin is interpreted as a mark, forcing the DO pin to V_{CC}.
11, 13, 15	DO1, DO2, DO3	**Data Output.** These are the receiver digital output pins, which swing from V_{CC} to GND. A space on the RX pin causes DO to produce a logic zero; a mark produces a logic one. Each output pin is capable of driving one LSTTL input load.
10, 12, 14	DI1, DI2, DI3	**Data Input.** These are the high-impedance digital input pins to the drivers. TTL compatibility is accomplished by biasing the input switchpoint at 1.4V above ground. However, 5V CMOS compatibility is maintained as well. Input voltage levels on these pins must be between V_{CC} and GND.
3, 5, 7	TX1, TX2, TX3	**Transmit Data Output.** These are the EIA-232-D transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic one at a DI input causes the corresponding TX output to swing toward V_{SS}. A logic zero causes the output to swing toward V_{DD} (the output voltages will be slightly less than V_{DD} or V_{SS} depending upon the output load). Output slew rates are limited to a maximum of 30V/µs. When the MC145406 is off (V_{DD} = V_{SS} = V_{CC} = GND), the minimum output impedance is 300Ω.

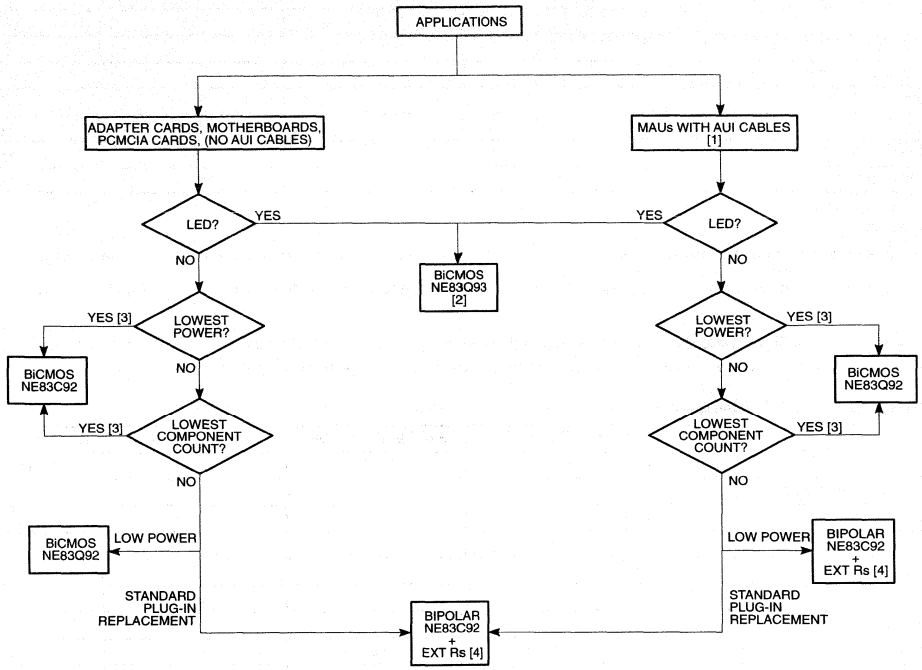
Section 5
Local Area Network Products

CONTENTS

Selection flowchart for Philips 10BASE5 and 10BASE2 transceivers 169
Ethernet transceiver power consumption comparison 170
NE83C92 Low-power coaxial Ethernet transceiver 171
NE83Q92 Low-power coaxial Ethernet transceiver 174
NE83Q93 Enhanced coaxial Ethernet transceiver 177

Selection flowchart for Philips 10BASE5 and 10BASE2 transceivers

Selection Flowchart for Philips 10BASE5 and 10BASE2 Transceivers



[1] The AUI Cable is normally terminated with 78Ω resistors.

[2] The NE83Q93 is the same as the NE83Q92 plus five status LED drivers.

[3] The NE83Q92 can drive the AUI cable without external R_S [4], and still meets the IEEE 802.3 specification. Without the AUI cable, the NE83C92 can perform as well. Existing designs with R_S can choose not to stuff them for appropriate application to save cost and power.

[4] External R_S = 500Ω external pull-down resistors (see Figure 1 of transceiver data sheets).

Selection Flowchart for Philips 10BASE5 and 10BASE2 Transceivers

Ethernet transceiver power consumption comparison

Supply Current in mA (TYP/MAX)

Device/Function	Idle Current	Ext Resistor Ntwk	Total Current	
	TYP	TYP	TYP	MAX
NE83Q92 CMOS				
Remote (Terminated AUI)				
Idle	15		15	20
Xmt	15		80	90
Rcv	15		35	39
Col + Jab	15		100	110

83Q92 Comments:

- External pull-down resistors optional in AUI Lines. Internal AUI drivers have an on-chip current source of 20mA for Rx± and 20mA for CD±.
- Rx±. only turns on when operating (external loopback or connected to cable) and CD±. only turns on when under collision or jabber conditions.
- NE83Q92 is best suited for Terminated (Remote MAU) applications where standard 50m AUI cable will be used as the only interface to the transceiver. NE83Q92 is best due to its low power requirements and external 500Ω pull-down resistors are optional.

Supply Current in mA (TYP/MAX)

NE83C92 CMOS	Idle Current	Ext Resistor Ntwk	Total Current	
	TYP	TYP	TYP	MAX
C92 Local (Unterminated AUI)				
Idle	15		15	20
Xmt	15		70	85
Rcv	15		25	30
Col + Jab	15		80	92
C92 Remote (Terminated AUI)				
Idle	15	28	43	48
Xmt	15	28	98	113
Rcv	15	28	53	58
Col + Jab	15	28	108	120

83C92 Comments:

- Uses simple internal pull-down current sources of 5mA on each side of the balanced output.
- 500Ω resistors are NOT required for an unterminated (local) application. (No AUI cable)
- 500Ω resistors ARE required for an terminated (remote) application, and add 28mA (7mA x4) to the total current consumption.
- Rx±. only turns on when operating (external loopback or connected to cable) and CD±. only turns on when under collision or jabber conditions.
- Best for Unterminated (Local, internal/adapter card) applications where the device resides on the adapter card with the controller and no AUI cable. (Interface is still the AUI, but the physical means is merely the PCB traces from the MAC to the Transceiver with very short chip-to-chip interface. Also, optimal for replacing bipolar parts in existing designs due to lowest power consumption and no external 500Ω resistors required. However, most customers will choose to use the resistors and bear the additional power consumption simply for the sake of compatibility to other solutions.
- For NEW designs requiring absolute lowest power/lowest cost solution, such as motherboards or PCMCIA cards, use the 83C92 without the 500Ω resistors.

Low-power coaxial Ethernet transceiver NE83C92

DESCRIPTION

The NE83C92 is a low power BiCMOS coaxial transceiver interface (CTI) for Ethernet (10base5) and Thin Ethernet (10base2) local area networks. The CTI is connected between the coaxial cable and the Data Terminal Equipment (DTE) and consists of a receiver, transmitter, receive-mode collision detector, heartbeat generator and jabber timer (see Block Diagram). The transmitter output connects directly to a doubly terminated 50Ω cable, while the receiver output, collision detector output and transmitter input are connected to the DTE through isolation transformers. Isolation between the CTI and the DTE is an IEEE 802.3 requirement that can be met on signal lines by using a set of pulse transformers. Power isolation for the CTI is achieved using DC-to-DC conversion through a power transformer.

The part is fully pin compatible with the industry standard 8392, but has substantially lower current consumption, is fully compliant with the IEEE802.3 standard, and has additional features such as automatic selection between AUI and coaxial connections, and requires no external pull-down resistors for local integrated MAU application.

The NE83C92 is manufactured on an advanced BiCMOS process and is available with PLCC package which make it ideally suited to lap-top personal computers or systems where low power consumption, limited board space and jumperless design is required. Refer to selection flow chart for optimal application.

FEATURES

- Fully compliant with Ethernet II, IEEE 802.3 10BASE-5 and 10BASE-2, and ISO 8802/3 interface specifications
- 100% drop-in compatible with industry standard 8392 sockets
- Optimal implementation can use 1 Watt DC-DC converter and reduces external part count (local/integrated MAU requires no external pull-down resistors).
- High efficiency AUI drivers automatically power-down under idle conditions to minimize current consumption
- Automatically disabling AUI drivers when disconnecting coax cable, allowing hardwiring of AUI connection and local/integrated CTI connection
- Smart squelch on data inputs eliminates false activations
- Advanced BiCMOS process for extremely low power operation

PIN CONFIGURATION

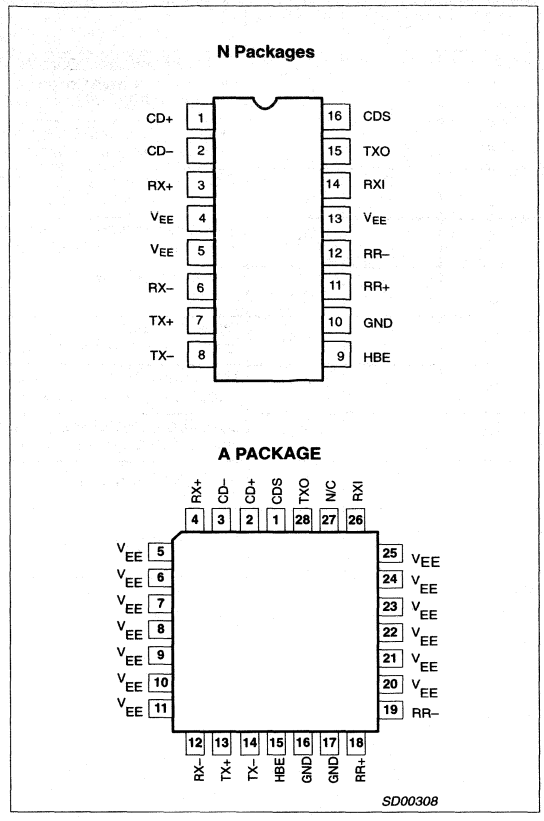


Figure 1. Pin Configurations

- Available in 16-pin DIP, and 28-pin PLCC packages
- Expanded version (NE83Q93) with 5 LED status drivers is available for repeater and advanced system applications
- Full ESD protection
- Power-on reset prevents glitches on coaxial cable during power-up

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package	0 to +70°C	NE83C92N	SOT38-4
28-Pin Plastic Leaded Chip Carrier	0 to +70°C	NE83C92A	SOT261-3

PIN DESCRIPTIONS

PIN NO. N PKG	PIN NO. PLCC	SYMBOL	DESCRIPTION
1 2	2 3	CD+ CD–	**Collision Outputs.** Balanced differential line driver outputs which send a 10MHz signal to the DTE in the event of a collision, jabber interrupt or heartbeat test. External pull-down resistors are optional with local/integrated MAU application.
3 6	4 12	RX+ RX–	**Receiver Outputs.** Balanced differential line driver outputs which send the received signal to the DTE. External pull-down resistors are optional with local/integrated MAU application.
7 8	13 14	TX+ TX–	**Transmitter Inputs.** Balanced differential line receiver inputs which accept the transmission signal from the DTE and apply it to the coaxial cable at TXO, once it meets Tx squelch threshold.
9	15	HBE	**Heartbeat Enable.** The heartbeat function is disabled when this pin is connected to V_{EE} and enabled when connected to GND or left floating.
11 12	18 19	RR+ RR–	**External Resistor.** A 1kΩ (1%) resistor connected between these pins establishes the signaling current at TXO.
14	26	RXI	**Receiver Input.** This pin is connected directly to the coaxial cable. Received signals are equalized, amplified, and sent to the DTE through the RX± pins, once it meets Rx squelch threshold.
15	28	TXO	**Transmitter Output.** This pin is connected directly (Thin Ethernet) or through an external isolating diode (Ethernet) to the coaxial cable.
16	1	CDS	**Collision Detect Sense.** Ground sense connection for the collision detection circuitry. This pin should be connected directly to the coaxial cable shield for standard Ethernet operation.
10	16 17	GND	**Positive Supply Pin.**
4 5 13	5 to 11 20 to 25	V_{EE}	**Negative Supply Pins.**

NOTE:
1. The IEEE 802.3 name for CD is CI; for RX is DI; for TX is DO.

BLOCK DIAGRAM

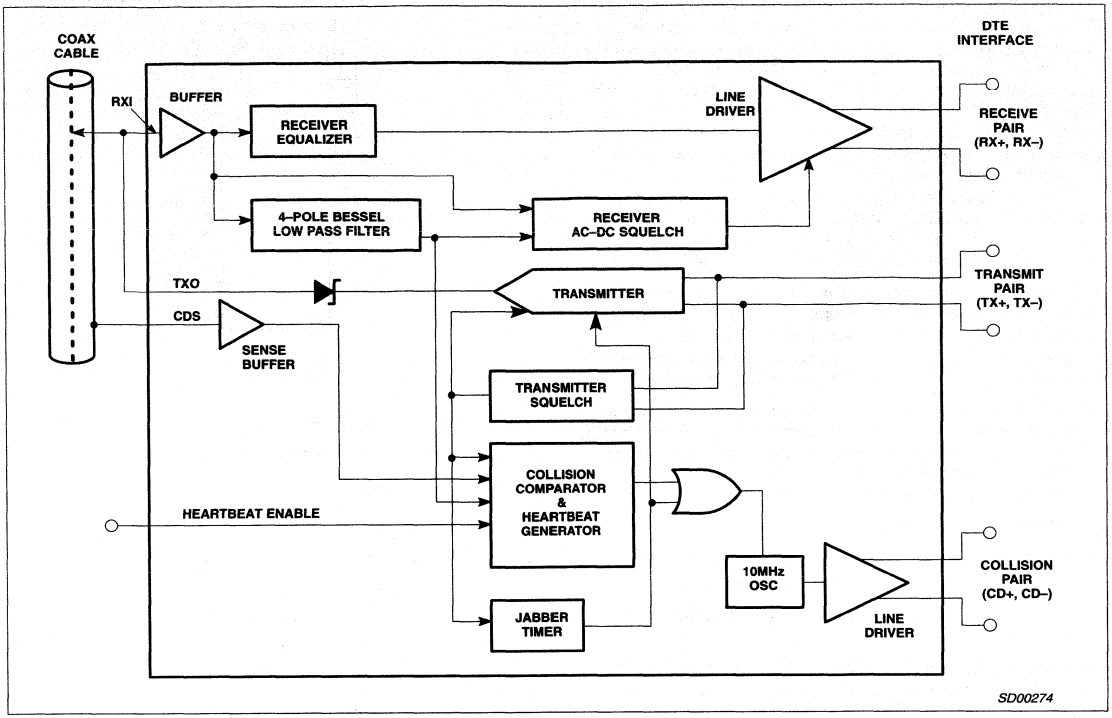


Figure 2. Block Diagram

Low-power coaxial Ethernet transceiver NE83Q92

DESCRIPTION

The NE83Q92 is a low power BiCMOS coaxial transceiver interface (CTI) for Ethernet (10base5) and Thin Ethernet (10base2) local area networks. The CTI is connected between the coaxial cable and the Data Terminal Equipment (DTE) and consists of a receiver, transmitter, receive-mode collision detector, heartbeat generator and jabber timer (see Block Diagram). The transmitter output connects directly to a doubly terminated 50Ω cable, while the receiver output, collision detector output and transmitter input are connected to the DTE through isolation transformers. Isolation between the CTI and the DTE is an IEEE 802.3 requirement that can be met on signal lines by using a set of pulse transformers. Power isolation for the CTI is achieved using DC-to-DC conversion through a power transformer (see Figure 3, Connection Diagram, included in CD-ROM version).

The part is fully pin compatible with the industry standard 8392, but has substantially lower current consumption, is fully compliant with the IEEE802.3 standard, and has additional features such as optional pull-down resistors (Figure 3, Note 4, included in CD-ROM version), and automatic selection between AUI and coaxial connections.

The NE83Q92 is manufactured on an advanced BiCMOS process and is available with PLCC and SOL packages which make it ideally suited to lap-top personal computers or systems where low power consumption, limited board space and jumperless design is required. Refer to selection flow chart for optimal application.

FEATURES

- Fully compliant with Ethernet II, IEEE 802.3 10BASE-5 and 10BASE-2, and ISO 8802/3 interface specifications
- 100% drop-in compatible with industry standard 8392 sockets (N & A options)
- Optimal implementation can use 1 Watt DC-DC converter and reduces external part count by not requiring external pull-down resistors
- High efficiency AUI drivers automatically power-down under idle conditions to minimize current consumption
- Automatically disables AUI drivers when no coaxial cable is connected, allowing hard-wiring of AUI connection and local/integrated CTI connection
- Smart squelch on data inputs eliminates false activations
- Advanced BiCMOS process for extremely low power operation
- Available in 16-pin DIP, 16-pin SOL and both 20- and 28-pin PLCC packages
- Expanded version (NE83Q93) with 5 LED status drivers is available for repeater and advanced system applications
- Full ESD protection
- Power-on reset prevents glitches on coaxial cable

PIN CONFIGURATION

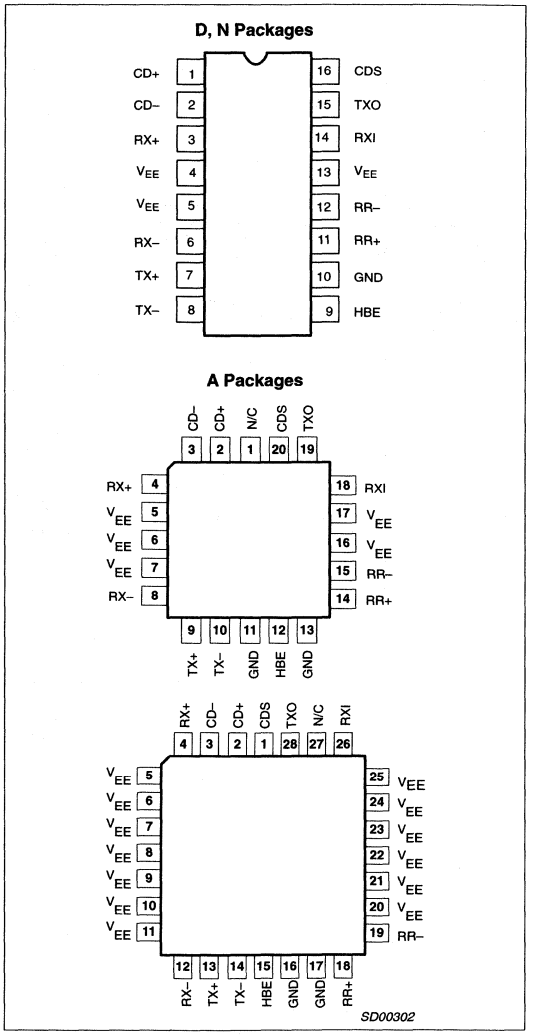


Figure 1. Pin Configurations

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE83Q92N	SOT38-4
16-Pin Plastic Small Outline Large (SOL) Package	0 to +70°C	NE83Q92D	SOT162-1
20-Pin Plastic Leaded Chip Carrier (PLCC) Package	0 to +70°C	NE83Q92A20	SOT380-1
28-Pin Plastic Leaded Chip Carrier (PLCC) Package	0 to +70°C	NE83Q92A	SOT261-3

PIN DESCRIPTIONS

PIN NO. N PKG	PIN NO. PLCC-20	PIN NO. PLCC-28	SYMBOL	DESCRIPTION
1 2	2 3	2 3	CD+ CD–	**Collision Outputs.** Balanced differential line driver outputs which send a 10MHz signal to the DTE in the event of a collision, jabber interrupt or heartbeat test. External pull-down resistors are optional.
3 6	4 8	4 12	RX+ RX–	**Receiver Outputs.** Balanced differential line driver outputs which send the received signal to the DTE. External pull-down resistors are optional.
7 8	9 10	13 14	TX+ TX–	**Transmitter Inputs.** Balanced differential line receiver inputs which accept the transmission signal from the DTE and apply it to the coaxial cable at TXO, if it meets Tx squelch threshold.
9	12	15	HBE	**Heartbeat Enable.** The heartbeat function is disabled when this pin is connected to V_{EE} and enabled when connected to GND or left floating.
11 12	14 15	18 19	RR+ RR–	**External Resistor.** A 1kΩ (1%) resistor connected between these pins establishes the signaling current at TXO.
14	18	26	RXI	**Receiver Input.** This pin is connected directly to the coaxial cable. Received signals are equalized, amplified, and sent to the DTE through the RX± pins, if it meets Rx squelch threshold.
15	19	28	TXO	**Transmitter Output.** This pin is connected directly (Thin Ethernet) or through an external isolating diode (Ethernet) to the coaxial cable.
16	20	1	CDS	**Collision Detect Sense.** Ground sense connection for the collision detection circuitry. This pin should be connected directly to the coaxial cable shield for standard Ethernet operation.
10	11 13	16 17	GND	**Positive Supply Pin.**
4 5 13	5 – 7 16 – 17	5 to 11 20 to 25	V_{EE}	**Negative supply pins.**
	1		N/C	**Not used.**

NOTE:
1. The IEEE 802.3 name for CD is CI; for RX is DI; for TX is DO.

BLOCK DIAGRAM

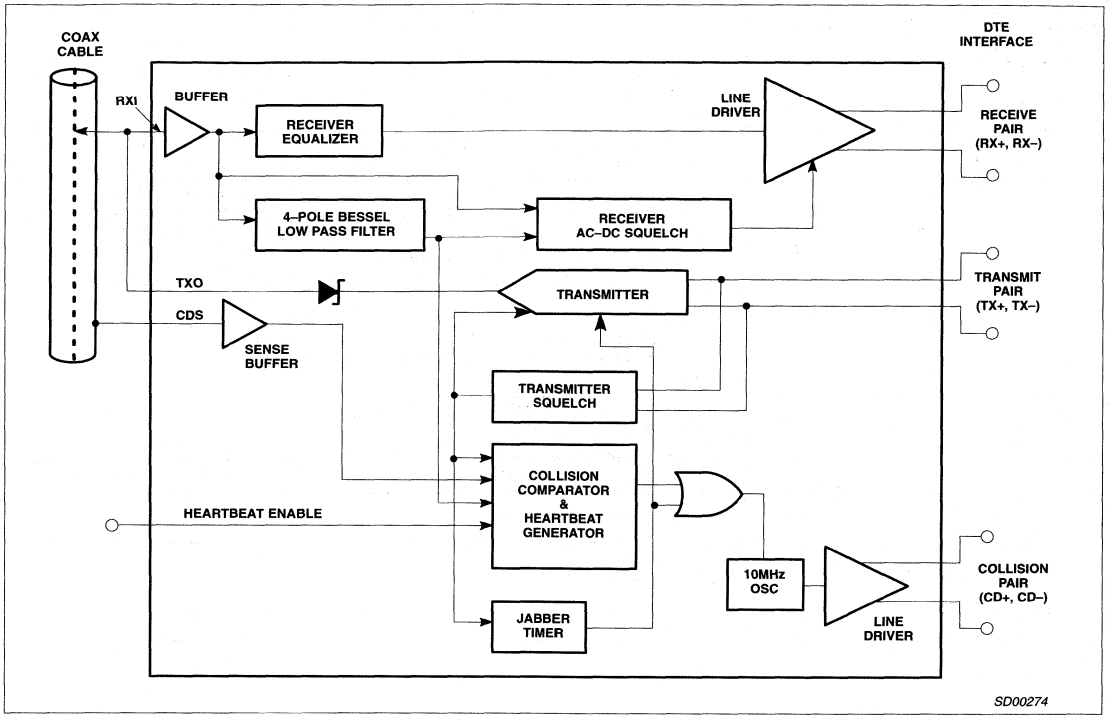


Figure 2. Block Diagram

Enhanced coaxial Ethernet transceiver NE83Q93

DESCRIPTION

The NE83Q93 is a low power coaxial transceiver interface (CTI) for Ethernet (10base5) and Thin Ethernet (10base2) local area networks. The CTI is connected between the coaxial cable and the Data Terminal Equipment (DTE) and consists of a receiver, transmitter, receive-mode collision detector, heartbeat generator and jabber timer (see Block Diagram). The transmitter output connects directly to a doubly terminated 50Ω cable, while the receiver output, collision detector output and transmitter input are connected to the DTE through isolation transformers. Isolation between the CTI and the DTE is an IEEE 802.3 requirement that can be met on signal lines by using a set of pulse transformers. Power isolation for the CTI is achieved using DC-to-DC conversion through a power transformer (see Figure 3, Connection Diagram, included in CD-ROM version).

The part is functionally the same as the NE83Q92, but with additional features such as a transmit enable input, a carrier detect output and five status LED driver outputs.

The NE83Q93 is manufactured on an advanced BiCMOS process and is available in an SOL package making it ideally suited to lap-top personal computers or systems where low power consumption, limited board space and jumperless design is required. Refer to selection flow chart for optimal application.

PIN CONFIGURATION

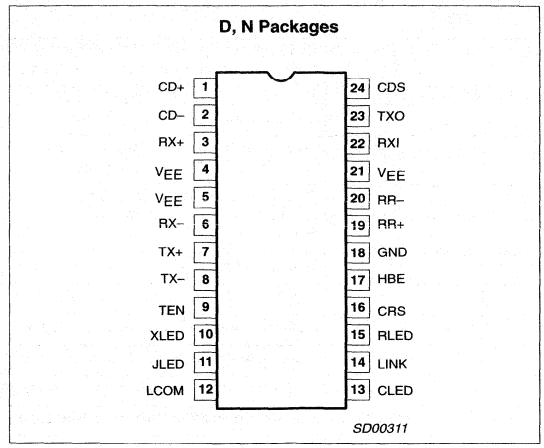


Figure 1. Pin Configurations

FEATURES

- Fully compliant with Ethernet II, IEEE 802.3 10BASE-5 and 10BASE-2, and ISO 8802/3 interface specifications
- Functionally compatible with industry standard 8392 applications
- Optimal implementation can use 1 Watt DC-DC converter and reduces external parts count
- High efficiency AUI drivers minimize current consumption under idle conditions by automatically powering-down
- Automatically disables AUI drivers when disconnecting coax cable, allowing hard-wiring of AUI connector and local/integrated CTI connection
- Smart squelch on data inputs eliminates false activations
- Transmit enable input and carrier sense output for repeater applications
- Five LED status drivers for transmit, receive, collision, jabber and link fail indication
- Advanced BiCMOS process for extremely low power operation
- Available in 24-pin DIP and 24-pin SOL packages
- Full ESD protection
- Power-on reset prevents glitches on coaxial cable

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE83Q93N	SOT222–1
24-Pin Plastic Small Outline Large (SOL) Package	0 to +70°C	NE83Q93D	SOT137-1

PIN DESCRIPTIONS

PIN NO. D, N PKG	SYMBOL	DESCRIPTION
1 2	CD+ CD–	**Collision Outputs.** Balanced differential line driver outputs which send a 10MHz signal to the DTE in the event of a collision, jabber interrupt or heartbeat test. External pull-down resistors are optional.
3 6	RX+ RX–	**Receiver Outputs.** Balanced differential line driver outputs which send the received signal to the DTE. External pull-down resistors are optional.
7 8	TX+ TX–	**Transmitter Inputs.** Balanced differential line receiver inputs which accept the transmission signal from the DTE and apply it to the coaxial cable at TXO, if it meets Tx squelch threshold.
9	TEN	**Transmit Enable.** A CMOS compatible input requiring an input voltage range of V_{EE} to V_{EE} + 5V. The transmitter and loopback functions are disabled when TEN is LOW and enabled when TEN is HIGH or left floating. TEN is normally driven through an opto-coupler.
10	XLED	**Transmit Indicator.** Indicates a packet is being transmitted onto the coaxial cable.
11	JLED	**Jabber Indicator.** Indicates that the jabber timer has timed out and the coaxial driver is disabled.
12	LCOM	**LED Common.** The anodes of all status indicator LEDs are connected to this pin. It's voltage is V_{EE} + 5V.
13	CLED	**Collision Indicator.** Indicates that a collision has been detected.
14	LINK	**Link Indicator.** Indicates that a connection is present to the coaxial cable network.
15	RLED	**Receive Indicator.** Indicates that a packet is being received from the coaxial cable.
16	CRS	**Carrier Sense.** A real time output that indicates the presence of a carrier on the coaxial cable. CRS is normally used to drive an opto-coupler.
17	HBE	**Heartbeat Enable.** The heartbeat function is disabled when this pin is connected to V_{EE} and enabled when connected to GND or left floating.
11 12	RR+ RR–	**External Resistor.** A 1kΩ (1%) resistor connected between these pins establishes the signaling current at TXO.
22	RXI	**Receiver Input.** This pin is connected directly to the coaxial cable. Received signals are equalized, amplified, and sent to the DTE through the RX± pins, if it meets Rx squelch threshold.
23	TXO	**Transmitter Output.** This pin is connected directly (Thin Ethernet) or through an external isolating diode (Ethernet) to the coaxial cable.
24	CDS	**Collision Detect Sense.** Ground sense connection for the collision detection circuitry. This pin should be connected directly to the coaxial cable shield for standard Ethernet operation.
18	GND	**Positive Supply Pin.**
4 5 21	V_{EE}	**Negative supply pins.**

NOTE:
1. The IEEE 802.3 name for CD is CI; for RX is DI; for TX is DO.

BLOCK DIAGRAM

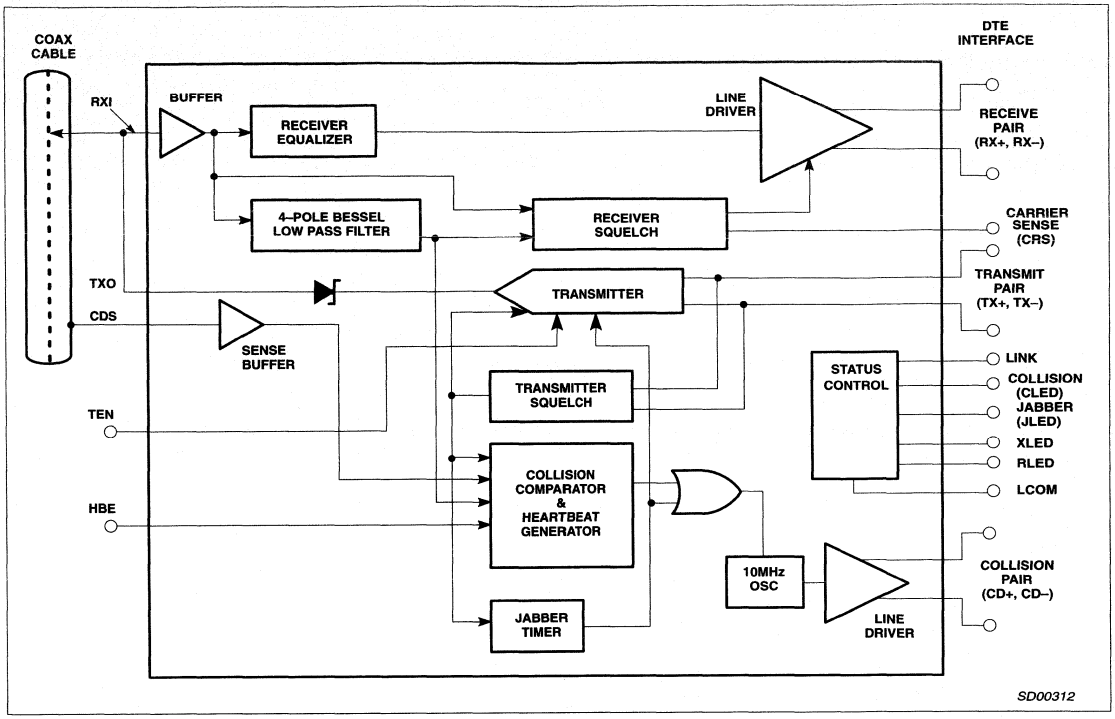


Figure 2. Block Diagram

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Fiber Optic Products

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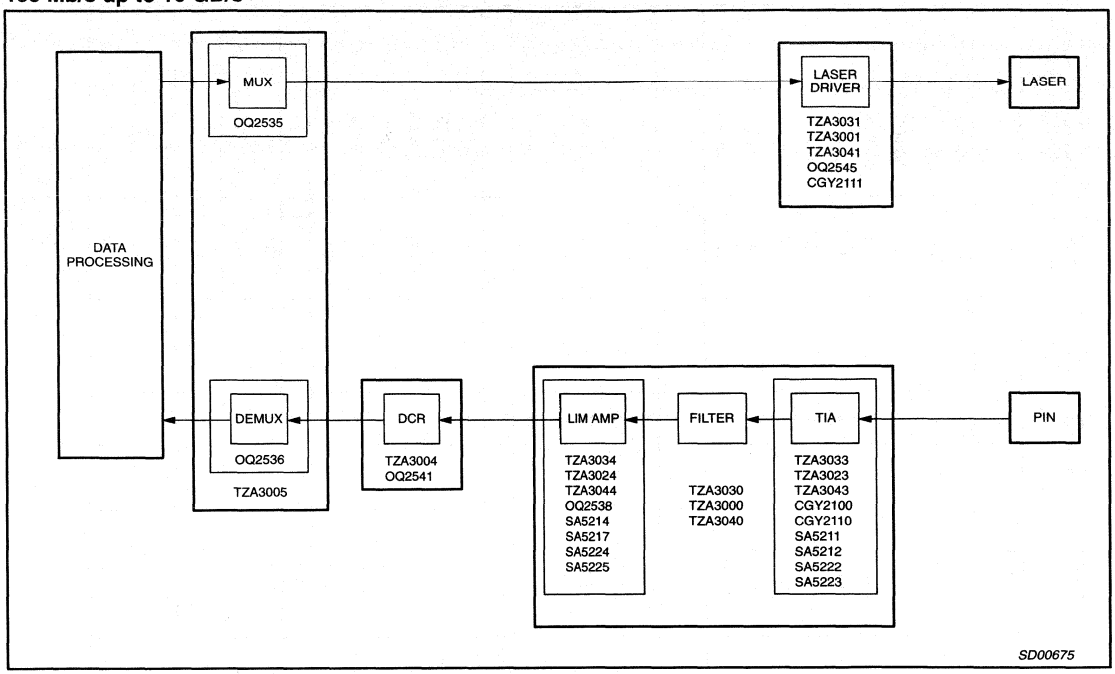
Fiber optic interface ICs selection guide

FIBER OPTIC INTERFACE ICs
155 Mb/s up to 10 GB/s



FIBER OPTIC INTERFACE ICs

Part Number	Datarate Mb/s	Package Type	Bare Die	Features			I/O	Single Supply		Multiple Supply	Power Dissipation	Process Technology	Status April '98
								3.3 V	5 V				
TRANSIMPEDANCE AMPLIFIERS				**In (nA)**	**Eq Sens (dBm)**	**LP Filter**	**Output**				**mW**		
NE/SA5223	155	SO8	X	16	–38.3		50 ohm		X		110	BiCMOS	A
TZA3030	155	LQFP 32	X	16	–38.3	X	CML/PECL	X	X		175	BiCMOS	D
TZA3033	155	SO8	X	16	–38.3		50 ohm	X	X		95	BiCMOS	S
TZA3000	622	LQFP 32	X	75	–31.6	X	CML/PECL	X	X		175	BiCMOS	A
TZA3023	622	SO8	X	72	–31.8		50 ohm	X	X		95	BiCMOS	A
TZA3040	1250	LQFP 32	X	160	–28.3		CML/PECL	X	X		175	BiCMOS	S
TZA3043	1250	SO8	X	160	–28.3		50 ohm	X	X		95	BiCMOS	S
CGY2100	2488	LQFP48	X	388	–24.5		50 ohm			X	430	GaAs	S
CGY2110	9952		X	620	–22.4		50 ohm		X		350	GaAs	S
LASERDRIVERS				**Imod/bias (mA)**	**EAM (Vppse)**	**E.R. control**	**Input**						
TZA3031	155	LQFP 32	X	60/90		X	CML/PECL		X		430	BiCMOS	D
TZA3001	622	LQFP 32	X	60/90		X	CML/PECL		X		430	BiCMOS	S
TZA3041	1250	LQFP 32	X	60/90		X	CML/PECL		X		430	BiCMOS	D
OQ2545	2488	LQFP48		60/100	2.5		CML			X	1350	BiCMOS	A
CGY2111	9952		X		3.0		CML		X		1350	GaAs	S
LIMITING AMPLIFIER				**Sens (mV)**	**BW (MHz)**	**Level detect**	**Output**						
NE/SA5224	155	SO16	X	2	120	2–13 mV	PECL		X		135	BiCMOS	A
NE/SA5225	155	SO16	X	2	120	2–12 mV	PECL		X		135	BiCMOS	A
TZA3034	155	SO16	X	2	150	2–12 MV	PECL	X	X		100	BiCMOS	S
TZA3024	622	SO16	X	2	600	2–12 mV	PECL	X	X		100	BiCMOS	D
TZA3044	1250	SO16	X	2	1200	2–12 mV	PECL	X	X		100	BiCMOS	D
OQ2538	2488	LQFP48	X	2	3200	analog	CML		X		270	BiCMOS	A
DATA AND CLOCK RECOVERY				**Sens (mV)**	**BER flag**	**Loop filter**	**I/O**						
TZA3004	155 & 622	LQFP48		2.5	X	internal	CML		X		350	BiCMOS	A
OQ2541	2488	LQFP48	X	2.5	X	internal	CML		X		350	BiCMOS	A
MULTIPLEXERS/DEMULTIPLEXERS				**Clock conversion**	**Frame D/Align**	**Buswidth**	**I/O**						
TZA3005	155 & 622	QFP64		X	X	4 or 8	PECL/TTL	X	X		900	BiCMOS	S
OQ2535	2488	HLQFP100				32	CML/TTL			X	1650	BiCMOS	A
OQ2536	2488	HLQFP100				32	CML/GTL			X	1450	BiCMOS	A

NOTES:

All figures given are typical at 25°C, power dissipation is given for 3.3 V when applicable
Eq. sensitivity conditions: extinction ratio, 10 Cpar = 1 pF, Responsivity diode = 0.85 A/W
Bandwidth = 60% of datarate

Status: A = Available (pilot or production)
S = Samples
D = Development

Transimpedance amplifier (180MHz) SA5211

DESCRIPTION

The SA5211 is a 28kΩ transimpedance, wide-band, low noise amplifier with differential outputs, particularly suitable for signal recovery in fiber optic receivers. The part is ideally suited for many other RF applications as a general purpose gain block.

FEATURES

- Extremely low noise: 1.8pA / $\sqrt{Hz}$
- Single 5V supply
- Large bandwidth: 180MHz
- Differential outputs
- Low input/output impedances
- High power supply rejection ratio
- 28kΩ differential transresistance

APPLICATIONS

- Fiber optic receivers, analog and digital
- Current-to-voltage converters
- Wide-band gain block

PIN CONFIGURATION

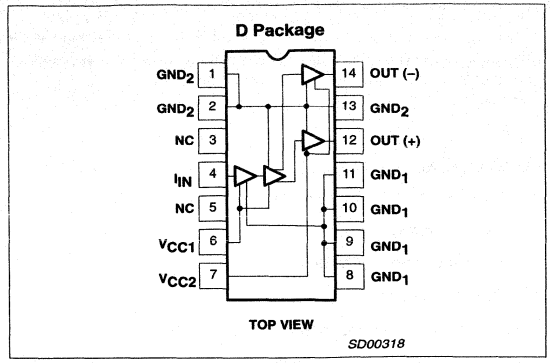


Figure 1. Pin Configuration

- Medical and scientific Instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO) Package	-40 to +85°C	SA5211D	SOT108-1

Transimpedance amplifier (140MHz) SA5212A

DESCRIPTION

The SA5212A is a 14kΩ transimpedance, wideband, low noise differential output amplifier, particularly suitable for signal recovery in fiber optic receivers and in any other applications where very low signal levels obtained from high-impedance sources need to be amplified.

FEATURES

- Extremely low noise: 2.5pA/√Hz
- Single 5V supply
- Large bandwidth: 140MHz
- Differential outputs
- Low input/output impedances
- 14kΩ differential transresistance
- ESD hardened

APPLICATIONS

- Fiber-optic receivers, analog and digital
- Current-to-voltage converters

PIN CONFIGURATION

N, FE, D Packages

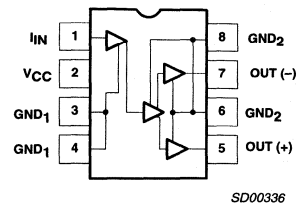


Figure 1. Pin Configuration

- Wideband gain block
- Medical and scientific instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA5212AD	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA5212AN	SOT97-1
8-Pin Ceramic Dual In-Line Package (DIP)	-40°C to +85°C	SA5212AFE	0580A

Postamplifier with link status indicator SA5214

DESCRIPTION

The SA5214 is a 75MHz postamplifier system designed to accept low level high-speed signals. These signals are converted into a TTL level at the output. The SA5214 can be DC coupled with the previous transimpedance stage using SA5210, SA5211 or SA5212 transimpedance amplifiers. This "system on a chip" features an auto-zeroed first stage with noise shaping, a symmetrical limiting second stage, and a matched rise/fall time TTL output buffer. The system is user-configurable to provide noise filtering, adjustable input thresholds and hysteresis. The threshold capability allows the user to maximize signal-to-noise ratio, insuring a low Bit Error Rate (BER). An Auto-Zero loop can be used to minimize the number of external coupling capacitors to one. A signal absent flag indicates when signals are below threshold. Additionally, the low signal condition forces the overall TTL output to a logical Low level. User interaction with this "jamming" system is available. The SA5214 is packaged in a standard 20-pin surface-mount package and typically consumes 42mA from a standard 5V supply. The SA5214 is designed as a companion to the SA5211/5212 transimpedance amplifiers. These differential preamplifiers may be directly coupled to the post-amplifier inputs. The SA5212/5214 or SA5211/5214 combinations convert nanoamps of photodetector current into standard digital TTL levels.

APPLICATIONS

- Fiber optics
- Communication links in Industrial and/or Telecom environment with high EMI/RFI
- Local Area Networks (LAN)
- Metropolitan Area Networks (MAN)
- Synchronous Optical Networks (SONET)
- RF limiter

PIN CONFIGURATION

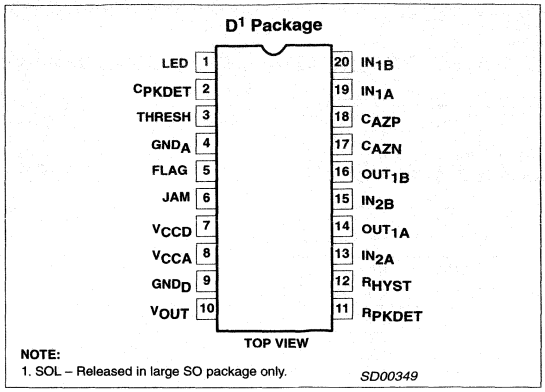


Figure 1. Pin Configuration

FEATURES

- Postamp for the SA5211/5212 preamplifier family
- Wideband operation: typical 75MHz (100MBaud NRZ)
- Interstage filtering/equalization possible
- Single 5V supply
- Low signal flag
- Low signal output disable
- Link status threshold and hysteresis programmable
- LED driver (normally ON with above threshold signal)
- Fully differential for excellent PSRR
- Auto-zero loop for DC offset cancellation
- 2kV ElectroStatic Discharge (ESD) protection

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) Package	-40°C to +85°C	SA5214D	SOT163-1

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	LED	Output for the LED driver. Open collector output transistor with 125Ω series limiting resistor. An above threshold signal turns this transistor ON.
2	C_{PKDET}	Capacitor for the peak detector. The value of this capacitor determines the detector response time to the signal, supplementing the internal 10pF capacitor.
3	THRESH	Peak detector threshold resistor. The value of this resistor determines the threshold level of the peak detector.
4	GND_A	Device analog ground pin.
5	FLAG	Peak detector digital output. When this output is LOW, there is data present above the threshold. This pin is normally connected to the JAM pin and has a TTL fanout of two.
6	JAM	Input to inhibit data flow. Sending the pin HIGH forces TTL DATA OUT ON, Pin 10, LOW. This pin is normally connected to the FLAG pin and is TTL-compatible.
7	V_{CCD}	Power supply pin for the digital portion of the chip.
8	V_{CCA}	Power supply pin for the analog portion of the chip.
9	GND_D	Device digital ground pin.
10	V_{OUT}	TTL output pin with a fanout of five.
11	R_{PKDET}	Peak detector current resistor. The value of this resistor determines the amount of discharge current available to the peak detector capacitor, C_{PKDET}.
12	R_{HYST}	Peak detector hysteresis resistor. The value of this resistor determines the amount of hysteresis in the peak detector.
13	IN_{2A}	Non-inverting input to amplifier A2.
14	OUT_{1A}	Non-inverting output of amplifier A1.
15	IN_{2B}	Inverting input to amplifier A2.
16	OUT_{1B}	Inverting output of amplifier A1.
17	C_{AZN}	Auto-Zero capacitor pin (Negative terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
18	C_{AZP}	Auto-Zero capacitor pin (Positive terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
19	IN_{1A}	Non-inverting input of the preamp A1.
20	IN_{1B}	Inverting input of the preamp A1.

BLOCK DIAGRAM

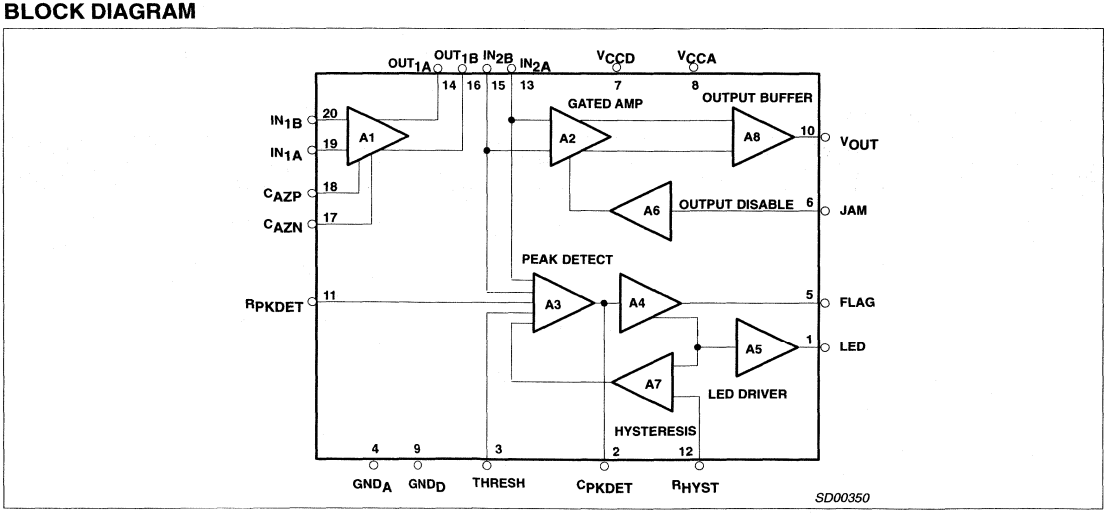


Figure 2. Block Diagram

Postamplifier with link status indicator SA5217

DESCRIPTION

The SA5217 is a 75MHz postamplifier system designed to accept low level high-speed signals. These signals are converted into a TTL level at the output. The SA5217 can be DC coupled with the previous transimpedance stage using SA5210, SA5211 or SA5212A transimpedance amplifiers. The main difference between the SA5217 and the SA5214 is that the SA5217 does not make the output of A1 and input of A2 accessible; instead, it brings out the output of A2 and the input of A8 thus activating the on-chip Schmitt trigger function by connecting two external capacitors. The result is that a much longer string of 1s and 0s, in the bit stream, can be tolerated. This "system on a chip" features an auto-zeroed first stage with noise shaping, a symmetrical limiting second stage, and a matched rise/fall time TTL output buffer. The system is user-configurable to provide adjustable input threshold and hysteresis. The threshold capability allows the user to maximize signal-to-noise ratio, thereby insuring a low Bit Error Rate (BER). An auto-zero loop can be used to replace two input coupling capacitors with a single Auto Zero (AZ) capacitor. A signal absent flag indicates when signals are below threshold. The low signal condition forces the TTL output to the last logic state. User interaction with this "jamming" system is available. The SA5217 is packaged in a standard 20-pin surface-mount package and typically consumes 40mA from a standard 5V supply. The SA5217 is designed as a companion to the SA5211/5212A and SA5210 transimpedance amplifiers. These differential preamplifiers may be directly coupled to the postamplifier inputs. The SA5210/5217, SA5211/5217 or SA5212A/5217 combinations convert nanoamps of photodetector current into standard digital TTL levels.

APPLICATIONS

- Fiber optics
- Communication links in Industrial and/or Telecom environment with high EMI/RFI
- Local Area Networks (LAN)
- Synchronous Optical Networks (SONET) STS-1
- RF limiter
- Good for 2^{23} -1 pseudo random bit stream

PIN CONFIGURATION

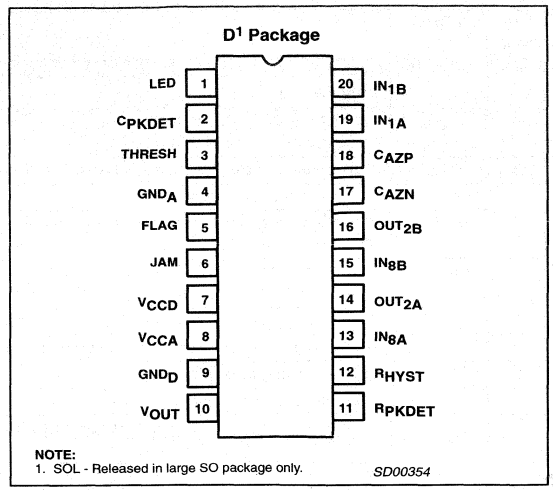


Figure 1. Pin Configuration

FEATURES

- Postamp for the SA5211/5212A. SA5210 preamplifier family
- Wideband operation: typical 75MHz (150MBaud NRZ)
- Interstage filtering/equalization possible
- Single 5V supply
- Low signal flag
- Output disable
- Link status threshold and hysteresis programmable
- LED driver (normally ON with above threshold signal)
- Fully differential for excellent PSRR
- Auto-zero loop for DC offset cancellation
- 2kV ElectroStatic Discharge (ESD) protection

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) Package	-40 to +85°C	SA5217D	SOT163-1

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	LED	Output for the LED driver. Open collector output transistor with 125Ω series limiting resistor. An above threshold signal turns this transistor ON.
2	C_{PKDET}	Capacitor for the peak detector. The value of this capacitor determines the detector response time to the signal, supplementing the internal 10pF capacitor.
3	THRESH	Peak detector threshold resistor. The value of this resistor determines the threshold level of the peak detector.
4	GND_A	Device analog ground pin.
5	FLAG	Peak detector digital output. When this output is LOW, there is data present above the threshold. This pin is normally connected to the JAM pin and has a TTL fanout of two.
6	JAM	Input to inhibit data flow. Sending the pin HIGH forces TTL DATA OUT ON, Pin 10, LOW. This pin is normally connected to the FLAG pin and is TTL-compatible.
7	V_{CCD}	Power supply pin for the digital portion of the chip.
8	V_{CCA}	Power supply pin for the analog portion of the chip.
9	GND_D	Device digital ground pin.
10	V_{OUT}	TTL output pin with a fanout of five.
11	R_{PKDET}	Peak detector current resistor. The value of this resistor determines the amount of discharge current available to the peak detector capacitor, C_{PKDET}.
12	R_{HYST}	Peak detector hysteresis resistor. The value of this resistor determines the amount of hysteresis in the peak detector.
13	IN_{8A}	Non-inverting input to amplifier A8.
14	OUT_{2A}	Non-inverting output of amplifier A2.
15	IN_{8B}	Inverting input to amplifier A8.
16	OUT_{2B}	Inverting output of amplifier A2.
17	C_{AZN}	Auto-Zero capacitor pin (Negative terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
18	C_{AZP}	Auto-Zero capacitor pin (Positive terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
19	IN_{1A}	Non-inverting input of the preamp A1.
20	IN_{1B}	Inverting input of the preamp A1.

BLOCK DIAGRAM

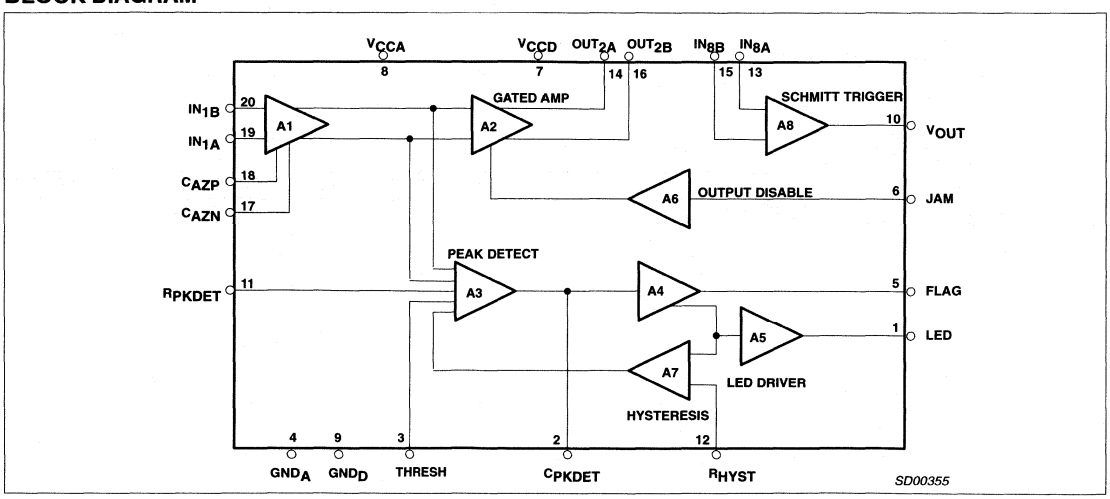


Figure 2. Block Diagram

Low-power FDDI transimpedance amplifier SA5222

DESCRIPTION

The SA5222 is a low-power, wide-band, low noise transimpedance amplifier with differential outputs, optimized for signal recovery in FDDI fiber optic receivers. The part is also suited for many other RF and fiber optic applications as a general purpose gain block.

FEATURES

- Extremely low noise: 2.0pA/ $\sqrt{Hz}$
- Single 5V supply
- Low supply current: 9mA
- Large bandwidth: 165MHz
- Differential outputs
- Low output offset
- Low input/output impedances
- High power-supply-rejection ratio: 55dB
- Tight transresistance control
- High input overload: 115μA
- ESD protected

PIN DESCRIPTION

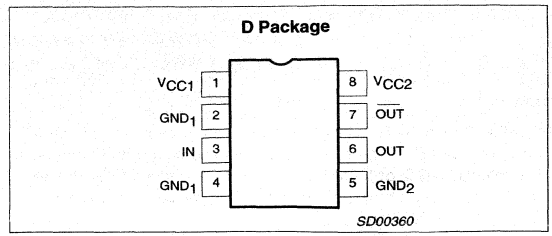


Figure 1. Pin Configuration

APPLICATIONS

- FDDI preamp
- Current-to-voltage converters
- Wide-band gain block
- Medical and scientific instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5222D	SOT96-1

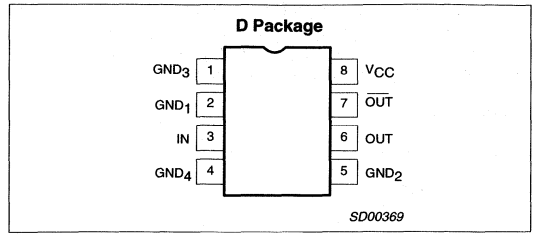
Wide dynamic range AGC transimpedance amplifier(150MHz) SA5223

DESCRIPTION

The SA5223 is a wide-band, low-noise transimpedance amplifier with differential outputs, incorporating AGC and optimized for signal recovery in wide-dynamic-range fiber optic receivers, such as SONET. The part is also suited for many other RF and fiber optic applications as a general purpose gain block.

The SA5223 is the first AGC amplifier to incorporate internal AGC loop hold capacitor, therefore, no external components are required. The internal AGC loop enables the SA5223 to effortlessly handle bursty data over a range of nA to mA of signal current, positive direction (sinking) only.

PIN DESCRIPTION



FEATURES

- Extremely low noise: 1.17pA/ $\sqrt{Hz}$
- Single 5V supply
- Low supply current: 22mA
- Large bandwidth: 150MHz
- Differential outputs
- Internal hold capacitor
- Low input/output impedances
- High power-supply-rejection ratio: 55dB
- Tight transresistance control
- High input overload: 4mA
- 2000V HBM ESD protection

APPLICATIONS

- OC3 SONET preamp (see AN1431 for detailed analysis
- Current-to-voltage converters
- Wide-band gain block
- Medical and scientific instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline	-40 to +85°C	SA5223D	SOT96-1

For unpackaged die please contact factory.

FDDI fiber optic postamplifier SA5224

DESCRIPTION

The SA5224 is a high-gain limiting amplifier that is designed to process signals from fiber optic preamplifiers. Capable of operating at 125Mb/s, the chip is FDDI compatible and has input signal level-detection with a user-adjustable threshold. The DATA and LEVEL-DETECT outputs are differential for optimum noise margin and ease of use. Also available is the SA5225 which is an ECL 10K version of the SA5224.

FEATURES

- Wideband operation: 1.0kHz to 120MHz typical
- Applicable in 155Mb/s OC3/SONET receivers
- Operation with single +5V or –5.2V supply
- Differential 100k ECL outputs
- Programmable input signal level-detection
- Fully differential for excellent PSRR to 1GHz

PIN DESCRIPTION

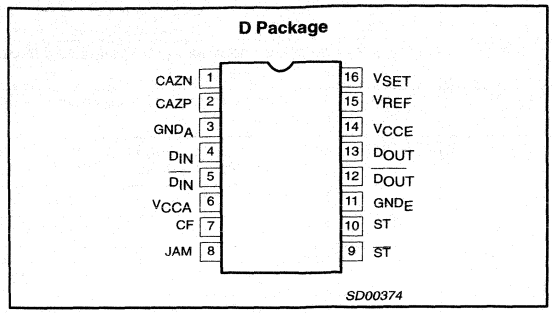


Figure 1. Pin Configuration

APPLICATIONS

- FDDI
- Data communication in noisy industrial environments
- LANs

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) package	–40 to +85°C	SA5224D	SOT109-1

BLOCK DIAGRAM

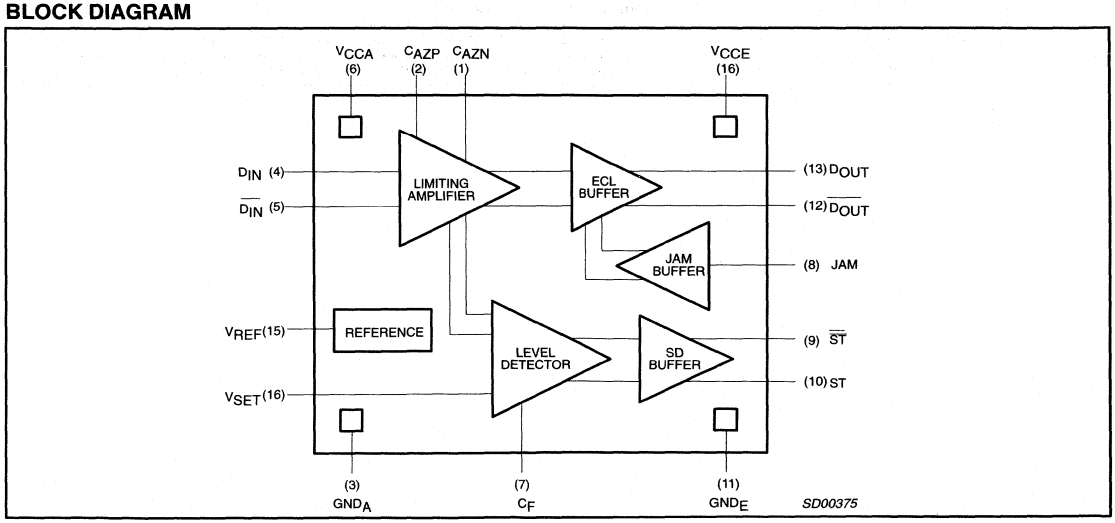


Figure 2. Block Diagram

PIN DESCRIPTIONS

PIN NO.	NAME	FUNCTION
1	C_{AZN}	Auto-zero capacitor pin. Connecting a capacitor between this pin and C_{AZP} will cancel the offset voltage of the limiting amplifier.
2	C_{AZP}	Auto-zero capacitor pin. Connecting a capacitor between this pin and C_{AZN} will cancel the offset voltage of the limiting amplifier.
3	GND_A	Analog GND pin. Connect to ground for +5V upshifted ECL operation. Connect to –5.2V for standard ECL operation. Must be at same potential as GND_E (Pin 11).
4	D_{IN}	Differential input. DC bias level is set internally at approximately 2.9V. Complimentary to $\overline{D_{IN}}$ (Pin 5).
5	$\overline{D_{IN}}$	Differential input. DC bias level is set internally at approximately 2.9V. Complimentary to D_{IN} (Pin 4).
6	V_{CCA}	Analog power supply pin. Connect to a +5V supply for upshifted ECL operation. Connect to ground for standard ECL operation. Must be at same potential as V_{CCE} (Pin 14).
7	C_F	Filter capacitor for level detector. Capacitor should be connected between this pin and V_{CCA}.
8	JAM	This ECL-compatible input controls the output buffers $\overline{D_{OUT}}$ and D_{OUT} (Pins 12 and 13). When an ECL LOW signal is applied, the outputs will follow the input signal. When an ECL HIGH signal is applied, the D_{OUT} and $\overline{D_{OUT}}$ pins will latch into LOW and HIGH states, respectively. When left unconnected, this pin is actively pulled-low (JAM OFF).
9	$\overline{ST}$	Input signal level-detect $\overline{STATUS}$. This ECL output is high when the input signal is below the user programmable threshold level.
10	ST	ECL compliment of $\overline{ST}$ (Pin 9).
11	GND_E	Digital GND pin. Connect to ground for +5V upshifted ECL operation. Connect to a negative supply for normal ECL operation. Must be at the same potential as GND_A (Pin 3).
12	$\overline{D_{OUT}}$	ECL-compatible output. Nominal level is V_{CCE}–1.3V. When JAM is HIGH, this pin will be forced into an ECL HIGH condition. Complimentary to D_{OUT} (Pin 13).
13	D_{OUT}	ECL-compatible output. Nominal level is V_{CCE}–1.3V. When JAM is HIGH, this pin will be forced into an ECL LOW condition. Complimentary to $\overline{D_{OUT}}$ (Pin 12).
14	V_{CCE}	Digital power supply pin. Connect to a +5V supply for upshifted ECL operation. Connect to ground during normal ECL operation. Must be at the same potential as V_{CCA} (Pin 6).
15	V_{REF}	Reference voltage for threshold level voltage divider. Nominal value is approximately 2.64V.
16	V_{SET}	Input threshold level setting circuit. This input can come from a voltage divider between V_{REF} and GND_A.

Fiber optic postamplifier SA5225

DESCRIPTION

The SA5225 is a high-gain limiting amplifier that is designed to process signals from fiber optic preamplifiers. Capable of operating at 125Mb/s, the chip has input signal level-detection with a user-adjustable threshold. The DATA and LEVEL-DETECT outputs are differential for optimum noise margin and ease of use. Also available is the SA5224 which is optimized for FDDI applications.

FEATURES

- Wideband operation: 1.0kHz to 120MHz typical
- Applicable in 155Mb/s OC3/SONET receivers
- Operation with single +5V or –5.2V supply
- Differential 10k ECL outputs
- Programmable input signal level-detection
- Fully differential for excellent PSRR to 1GHz

APPLICATIONS

- Data communication in noisy industrial environments
- LANs

PIN DESCRIPTION

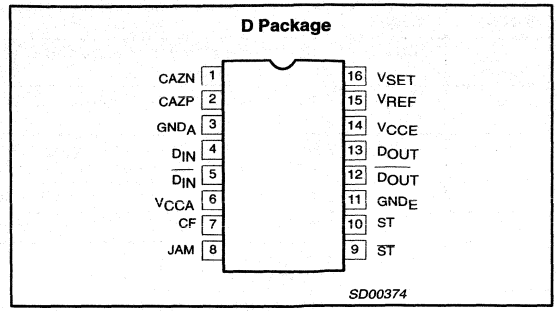


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) Package	–40 to +85°C	SA5225D	SOT109-1

BLOCK DIAGRAM

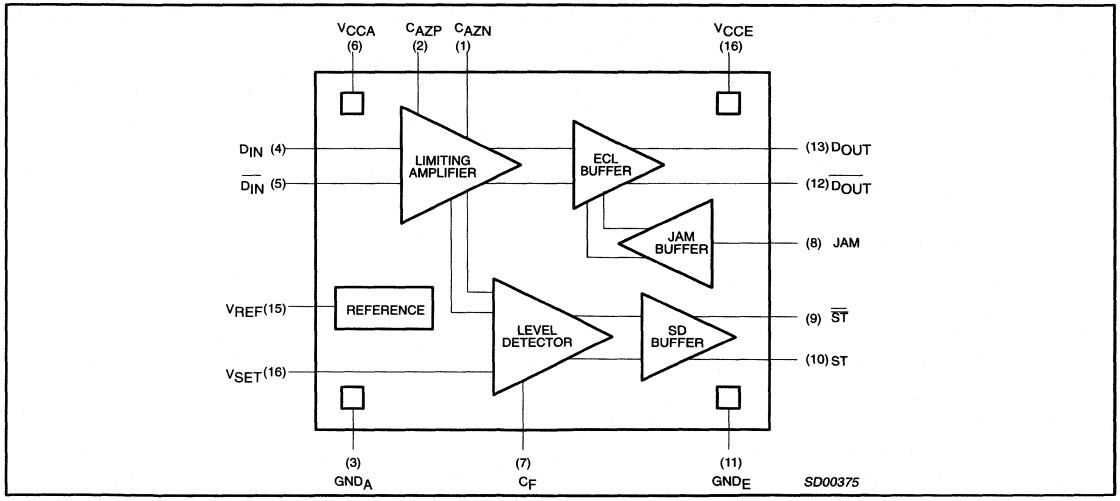


Figure 2. Block Diagram

PIN DESCRIPTIONS

PIN NO.	NAME	FUNCTION
1	C_{AZN}	Auto-zero capacitor pin. Connecting a capacitor between this pin and C_{AZP} will cancel the offset voltage of the limiting amplifier.
2	C_{AZP}	Auto-zero capacitor pin. Connecting a capacitor between this pin and C_{AZN} will cancel the offset voltage of the limiting amplifier.
3	GND_A	Analog GND pin. Connect to ground for +5V upshifted ECL operation. Connect to –5.2V for standard ECL operation. Must be at same potential as GND_E (Pin 11).
4	D_{IN}	Differential input. DC bias level is set internally at approximately 2.9V. Complimentary to $\overline{D_{IN}}$ (Pin 5).
5	$\overline{D_{IN}}$	Differential input. DC bias level is set internally at approximately 2.9V. Complimentary to D_{IN} (Pin 4).
6	V_{CCA}	Analog power supply pin. Connect to a +5V supply for upshifted ECL operation. Connect to ground for standard ECL operation. Must be at same potential as V_{CCE} (Pin 14).
7	C_F	Filter capacitor for level detector. Capacitor should be connected between this pin and V_{CCA}.
8	JAM	This ECL-compatible input controls the output buffers $\overline{D_{OUT}}$ and D_{OUT} (Pins 12 and 13). When an ECL LOW signal is applied, the outputs will follow the input signal. When an ECL HIGH signal is applied, the D_{OUT} and $\overline{D_{OUT}}$ pins will latch into LOW and HIGH states, respectively. When left unconnected, this pin is actively pulled-low (JAM OFF).
9	$\overline{ST}$	Input signal level-detect $\overline{STATUS}$. This ECL output is high when the input signal is below the user programmable threshold level.
10	ST	ECL compliment of $\overline{ST}$ (Pin 9).
11	GND_E	Digital GND pin. Connect to ground for +5V upshifted ECL operation. Connect to a negative supply for normal ECL operation. Must be at the same potential as GND_A (Pin 3).
12	$\overline{D_{OUT}}$	ECL-compatible output. Nominal level is V_{CCE}–1.3V. When JAM is HIGH, this pin will be forced into an ECL HIGH condition. Complimentary to D_{OUT} (Pin 13).
13	D_{OUT}	ECL-compatible output. Nominal level is V_{CCE}–1.3V. When JAM is HIGH, this pin will be forced into an ECL LOW condition. Complimentary to $\overline{D_{OUT}}$ (Pin 12).
14	V_{CCE}	Digital power supply pin. Connect to a +5V supply for upshifted ECL operation. Connect to ground during normal ECL operation. Must be at the same potential as V_{CCA} (Pin 6).
15	V_{REF}	Reference voltage for threshold level voltage divider. Nominal value is approximately 2.64V.
16	V_{SET}	Input threshold level setting circuit. This input can come from a voltage divider between V_{REF} and GND_A.

SDH/SONET STM16/OC48 multiplexer OQ2535HP

FEATURES

- Normal and loop (test) modes
- 3.3 V TTL compatible data inputs
- Differential CML (Current-Mode Logic) clock and data outputs
- 5 V TTL clock output (low speed interface)
- High input sensitivity (50 mV for the high speed clock input)
- Input capacitance <2 pF (low speed data inputs)
- Clock phase margin of 250° at 78 Mbits/s interface
- Boundary Scan Test (BST) at low speed interface, in accordance with *"IEEE Std 1149.1-1990"*
- Low power dissipation (typically 1.65 W).

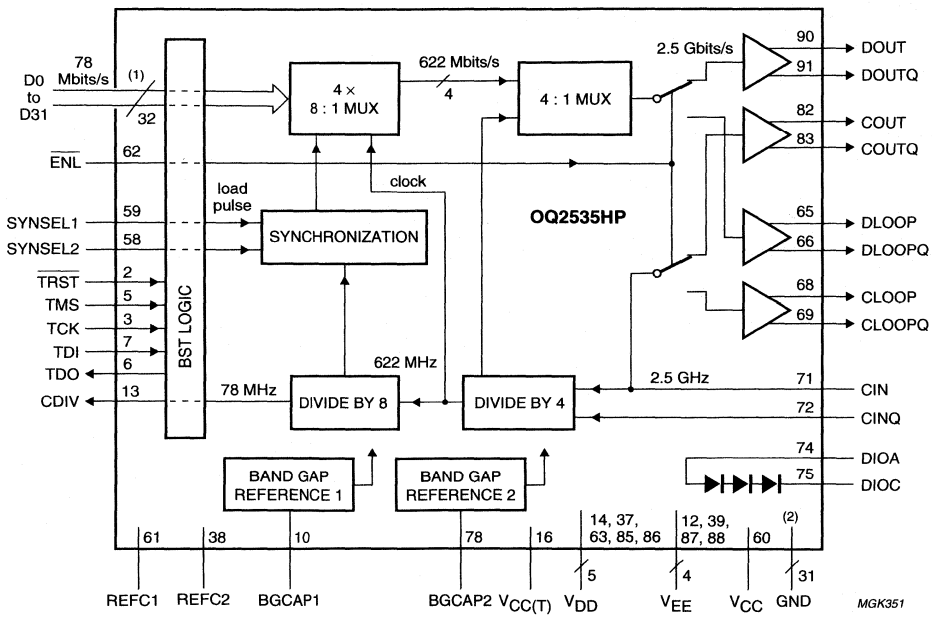
GENERAL DESCRIPTION

The OQ2535HP is a 32-channel multiplexer intended for use in STM16/OC48 applications. It combines data from a total of 32 × 78 Mbits/s input channels onto a single 2.5 Gbits/s output channel. It features 3.3 V TTL data inputs and a 5 V TTL clock output at the low speed interface, and CML compatible inputs and outputs at the high speed interface.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OQ2535HP	HLQFP100	plastic heat-dissipating low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT470-1

BLOCK DIAGRAM



(1) See Chapter "Pinning" for D0 to D31 pin numbers.

(2) Pins 1, 4, 8, 9, 11, 15, 17, 21, 25, 36, 40, 56, 64, 67, 70, 73, 76, 77, 79, 80, 81, 84, 89, 92 to 98 and 100.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE[1]	DESCRIPTION
GND	1	S	ground
$\overline{TRST}$	2	I	test RESET input for BST mode (active LOW)
TCK	3	I	test clock input for BST mode
GND	4	S	ground
TMS	5	I	test mode select input for BST mode
TDO	6	O	serial test data output for BST mode
TDI	7	I	serial test data input for BST mode
GND	8	S	ground
GND	9	S	ground
BGCAP1	10	A	pin for connecting external band gap decoupling capacitor (4 × 8 : 1 MUX)
GND	11	S	ground
V_{EE}	12	S	supply voltage (−4.5 V)
CDIV	13	O	78 MHz clock output
V_{DD}	14	S	supply voltage (+3.3 V)
GND	15	S	ground
$V_{CC(T)}$	16	S	supply voltage for TTL buffer (+5.0 V); not connected internally to V_{CC}
GND	17	S	ground
D31	18	I	78 Mbits/s data input channel for D31
D27	19	I	78 Mbits/s data input channel for D27
D23	20	I	78 Mbits/s data input channel for D23
GND	21	S	ground
D19	22	I	78 Mbits/s data input channel for D19
D15	23	I	78 Mbits/s data input channel for D15
D11	24	I	78 Mbits/s data input channel for D11
GND	25	S	ground
D7	26	I	78 Mbits/s data input channel for D7
D3	27	I	78 Mbits/s data input channel for D3
D30	28	I	78 Mbits/s data input channel for D30
D26	29	I	78 Mbits/s data input channel for D26
D22	30	I	78 Mbits/s data input channel for D22
D18	31	I	78 Mbits/s data input channel for D18
D14	32	I	78 Mbits/s data input channel for D14
D10	33	I	78 Mbits/s data input channel for D10
D6	34	I	78 Mbits/s data input channel for D6
D2	35	I	78 Mbits/s data input channel for D2
GND	36	S	ground
V_{DD}	37	S	supply voltage (+3.3 V)
REFC2	38	A	pin for connecting external reference decoupling capacitor (3.3 V CMOS reference)

SYMBOL	PIN	TYPE[1]	DESCRIPTION
V_{EE}	39	S	supply voltage (−4.5 V)
GND	40	S	ground
D29	41	I	78 Mbits/s data input channel for D29
D25	42	I	78 Mbits/s data input channel for D25
D21	43	I	78 Mbits/s data input channel for D21
D17	44	I	78 Mbits/s data input channel for D17
D13	45	I	78 Mbits/s data input channel for D13
D9	46	I	78 Mbits/s data input channel for D9
D5	47	I	78 Mbits/s data input channel for D5
D1	48	I	78 Mbits/s data input channel for D1
D28	49	I	78 Mbits/s data input channel for D28
D24	50	I	78 Mbits/s data input channel for D24
D20	51	I	78 Mbits/s data input channel for D20
D16	52	I	78 Mbits/s data input channel for D16
D12	53	I	78 Mbits/s data input channel for D12
D8	54	I	78 Mbits/s data input channel for D8
D4	55	I	78 Mbits/s data input channel for D4
GND	56	S	ground
D0	57	I	78 Mbits/s data input channel for D0
SYNSEL2	58	I	selection input 2 for synchronization pulse timing
SYNSEL1	59	I	selection input 1 for synchronization pulse timing
V_{CC}	60	S	supply voltage (+5.0 V)
REFC1	61	A	pin for connecting external reference decoupling capacitor (for standard TTL reference)
$\overline{ENL}$	62	I	loop mode enable (active LOW)
V_{DD}	63	S	supply voltage (+3.3 V)
GND	64	S	ground
DLOOP	65	O	data output to demultiplexer IC OQ2536 (loop mode)
DLOOPQ	66	O	inverted data output to demultiplexer IC OQ2536 (loop mode)
GND	67	S	ground
CLOOP	68	O	clock output to demultiplexer IC OQ2536 (loop mode)
CLOOPQ	69	O	inverted clock output to demultiplexer IC OQ2536 (loop mode)
GND	70	S	ground
CIN	71	I	clock input from VCO IC
CINQ	72	I	inverted clock input from VCO IC
GND	73	S	ground
DIOA	74	A	anode of temperature diode array
DIOC	75	A	cathode of temperature diode array
GND	76	S	ground
GND	77	S	ground
BGCAP2	78	A	pin for connecting external band gap decoupling capacitor (4 : 1 MUX)

SYMBOL	PIN	TYPE[1]	DESCRIPTION
GND	79	S	ground
GND	80	S	ground
GND	81	S	ground
COUT	82	O	clock output to laser driver IC
COUTQ	83	O	inverted clock output to laser driver IC
GND	84	S	ground
V_{DD}	85	S	supply voltage (+3.3 V)
V_{DD}	86	S	supply voltage (+3.3 V)
V_{EE}	87	S	supply voltage (−4.5 V)
V_{EE}	88	S	supply voltage (−4.5 V)
GND	89	S	ground
DOUT	90	O	data output to laser driver IC
DOUTQ	91	O	inverted data output to laser driver IC
GND	92	S	ground
GND	93	S	ground
GND	94	S	ground
GND	95	S	ground
GND	96	S	ground
GND	97	S	ground
GND	98	S	ground
i.c.	99	–	internally connected, to be left open-circuit
GND	100	S	ground

Note

1. Pin type abbreviations: O = Output, I = Input, S =power Supply, A = Analog function.

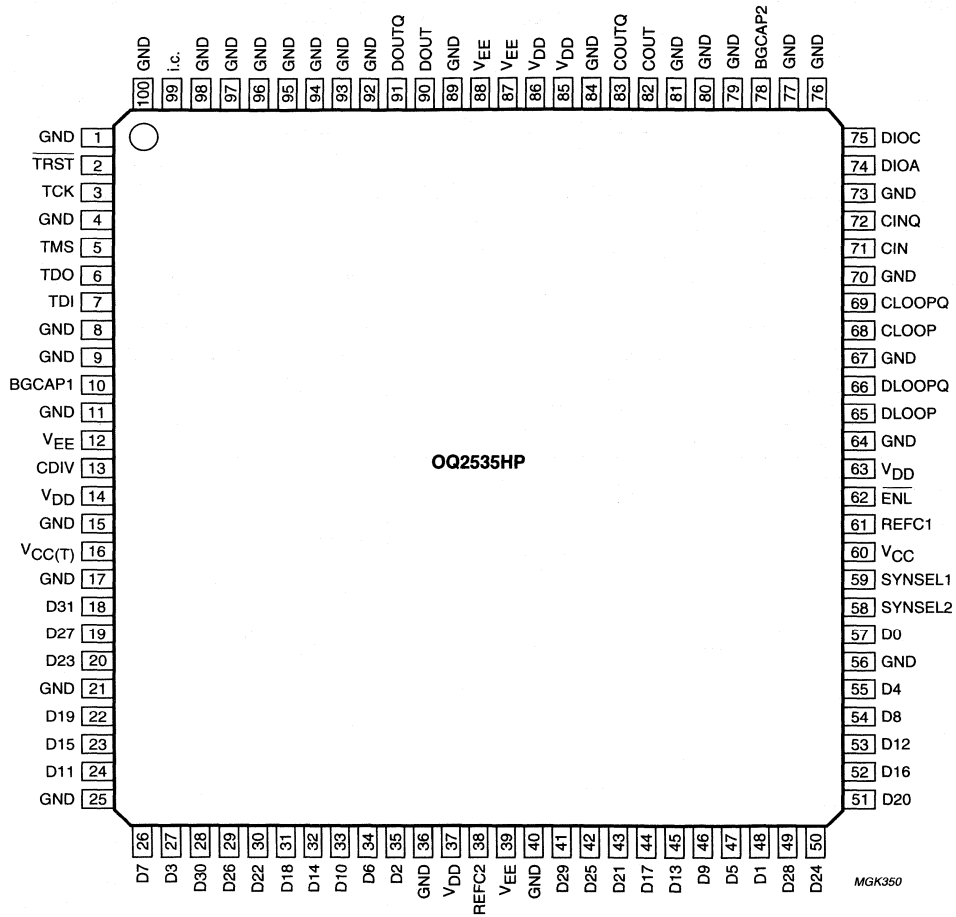


Fig.2 Pin configuration.

SDH/SONET STM16/OC48 demultiplexer OQ2536HP

FEATURES

- Normal and loop (test) modes
- 1.2 V GTL (Gunning Transceiver Logic) level compatible data and clock outputs (low speed interface)
- Differential CML (Current-Mode Logic) data and clock inputs
- High input sensitivity (100 mV for the high speed inputs)
- Boundary Scan Test (BST) at low speed interface, in accordance with *"IEEE Std 1149.1-1990"*
- Low power dissipation (typically 1.45 W).

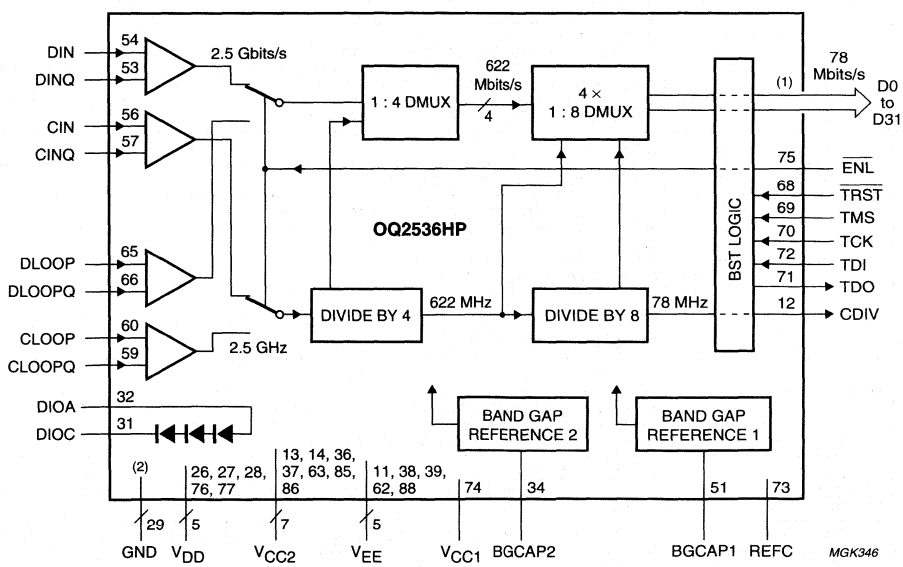
DESCRIPTION

The OQ2536HP is a 32-channel demultiplexer intended for use in STM16/OC48 applications. It demultiplexes a single 2.5 Gbits/s input channel to 32 × 78 Mbits/s output channels. The data and clock outputs on the low speed interface are GTL compatible, while the high speed data and clock inputs are CML compatible.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OQ2536HP	HLQFP100	plastic heat-dissipating low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT470-1

BLOCK DIAGRAM



(1) See Chapter "Pinning" for D0 to D31 pin numbers.

(2) Pins 1, 8, 17, 22, 25, 29, 33, 35, 40 to 50, 52, 55, 58, 61, 64, 67, 78, 82, 91 and 96.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE[1]	DESCRIPTION
GND	1	S	ground
D29	2	O	78 Mbits/s data output channel for D29
D25	3	O	78 Mbits/s data output channel for D25
D21	4	O	78 Mbits/s data output channel for D21
D17	5	O	78 Mbits/s data output channel for D17
D13	6	O	78 Mbits/s data output channel for D13
D9	7	O	78 Mbits/s data output channel for D9
GND	8	S	ground
D5	9	O	78 Mbits/s data output channel for D5
D1	10	O	78 Mbits/s data output channel for D1
V_{EE}	11	S	supply voltage (−4.5 V)
CDIV	12	O	78 MHz clock output
V_{CC2}	13	S	supply voltage (+1.5 V)
V_{CC2}	14	S	supply voltage (+1.5 V)
D28	15	O	78 Mbits/s data output channel for D28
D24	16	O	78 Mbits/s data output channel for D24
GND	17	S	ground
D20	18	O	78 Mbits/s data output channel for D20
D16	19	O	78 Mbits/s data output channel for D16
D12	20	O	78 Mbits/s data output channel for D12
D8	21	O	78 Mbits/s data output channel for D8
GND	22	S	ground
D4	23	O	78 Mbits/s data output channel for D4
D0	24	O	78 Mbits/s data output channel for D0
GND	25	S	ground
V_{DD}	26	I	supply voltage (+3.3 V)
V_{DD}	27	I	supply voltage (+3.3 V)
V_{DD}	28	I	supply voltage (+3.3 V)
GND	29	S	ground
i.c.	30	–	internally connected, to be left open-circuit
DIOC	31	A	cathode of temperature diode array
DIOA	32	A	anode of temperature diode array
GND	33	S	ground
BGCAP2	34	A	pin for connecting external band gap decoupling capacitor (4 × 1 : 8 DMUX)
GND	35	S	ground
V_{CC2}	36	S	supply voltage (+1.5 V)
V_{CC2}	37	S	supply voltage (+1.5 V)
V_{EE}	38	S	supply voltage (−4.5 V)
V_{EE}	39	S	supply voltage (−4.5 V)
GND	40	S	ground

SYMBOL	PIN	TYPE[1]	DESCRIPTION
GND	41	S	ground
GND	42	S	ground
GND	43	S	ground
GND	44	S	ground
GND	45	S	ground
GND	46	S	ground
GND	47	S	ground
GND	48	S	ground
GND	49	S	ground
GND	50	S	ground
BGCAP1	51	A	pin for connecting external band gap decoupling capacitor (1 : 4 DMUX)
GND	52	S	ground
DINQ	53	I	inverted data input in normal mode
DIN	54	I	data input in normal mode
GND	55	S	ground
CIN	56	I	clock input in normal mode
CINQ	57	I	inverted clock input in normal mode
GND	58	S	ground
CLOOPQ	59	I	inverted clock input from multiplexer IC OQ2535 (loop mode)
CLOOP	60	I	clock input from multiplexer IC OQ2535 (loop mode)
GND	61	S	ground
V_{EE}	62	S	supply voltage (−4.5 V)
V_{CC2}	63	S	supply voltage (+1.5 V)
GND	64	S	ground
DLOOP	65	I	data input from multiplexer IC OQ2535 (loop mode)
DLOOPQ	66	I	inverted data input from multiplexer IC OQ2535 (loop mode)
GND	67	S	ground
$\overline{TRST}$	68	I	test RESET input for BST mode (active LOW)
TMS	69	I	test mode select input for BST
TCK	70	I	test clock input for BST mode
TDO	71	O	serial test data output for BST mode
TDI	72	I	serial test data input for BST mode
REFC	73	A	pin for connecting external reference decoupling capacitor (for standard TTL reference)
V_{CC1}	74	S	supply voltage (+5.0 V)
$\overline{ENL}$	75	I	loop mode enable input (active LOW)
V_{DD}	76	I	supply voltage (+3.3 V)
V_{DD}	77	I	supply voltage (+3.3 V)
GND	78	S	ground
D31	79	O	78 Mbits/s data output channel for D31
D27	80	O	78 Mbits/s data output channel for D27

SYMBOL	PIN	TYPE[1]	DESCRIPTION
D23	81	O	78 Mbits/s data output channel for D23
GND	82	S	ground
D19	83	O	78 Mbits/s data output channel for D19
D15	84	O	78 Mbits/s data output channel for D15
V_{CC2}	85	S	supply voltage (+1.5 V)
V_{CC2}	86	S	supply voltage (+1.5 V)
D11	87	O	78 Mbits/s data output channel for D11
V_{EE}	88	S	supply voltage (−4.5 V)
D7	89	O	78 Mbits/s data output channel for D7
D3	90	O	78 Mbits/s data output channel for D3
GND	91	S	ground
D30	92	O	78 Mbits/s data output channel for D30
D26	93	O	78 Mbits/s data output channel for D26
D22	94	O	78 Mbits/s data output channel for D22
D18	95	O	78 Mbits/s data output channel for D18
GND	96	S	ground
D14	97	O	78 Mbits/s data output channel for D14
D10	98	O	78 Mbits/s data output channel for D10
D6	99	O	78 Mbits/s data output channel for D6
D2	100	O	78 Mbits/s data output channel for D2

Note

1. Pin type abbreviations: O = Output, I = Input, S = power Supply, A = Analog function.

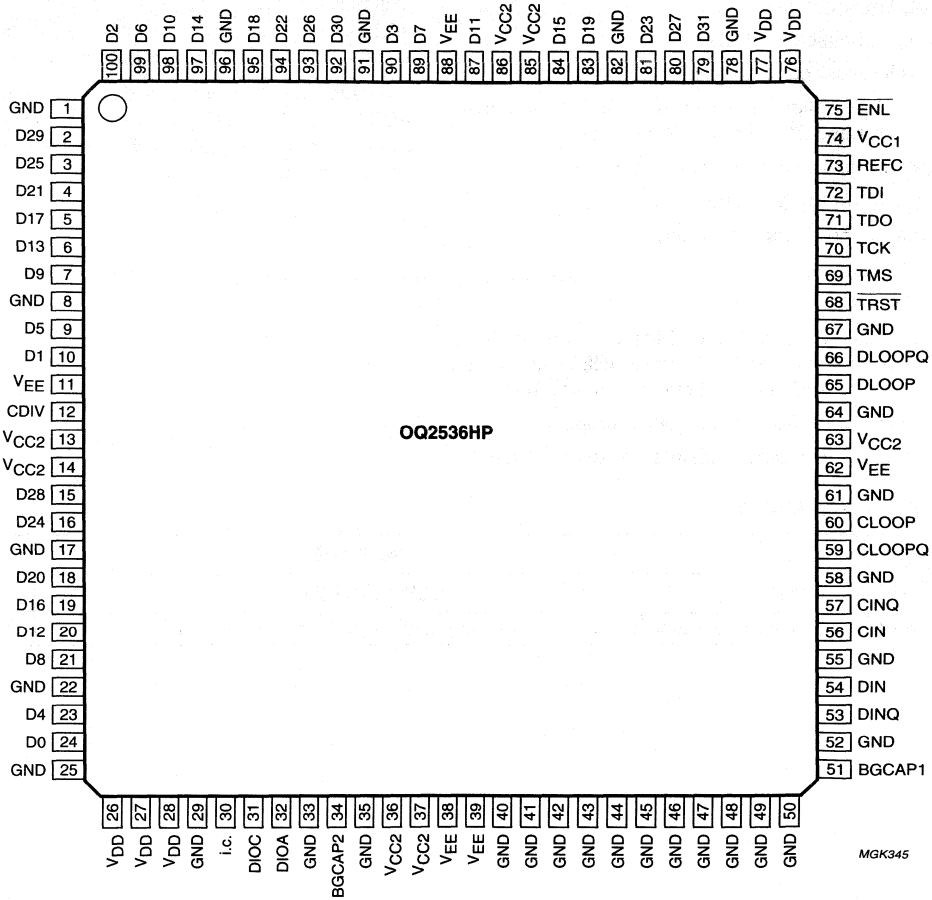


Fig.2 Pin configuration.

SDH/SONET main amplifier OQ2538HP

FEATURES

- Differential 100 Ω outputs for direct connection to Current-Mode Logic (CML) inputs
- Wide bandwidth (3 GHz)
- 48.5 dB limiting gain
- Noise figure typically 11 dB
- Automatic offset compensation
- Input level-detection circuits for Automatic Gain Control (AGC) and Loss Of Signal (LOS) detection
- Low power dissipation (typically 270 mW)
- Single –4.5 V supply voltage
- Low cost LQFP48 plastic package.

APPLICATIONS

- Main amplifier in Synchronous Digital Hierarchy (SDH) and Synchronous Optical Network (SONET) systems for short, medium and long haul optical transmission
- Level detector for laser diode control loops
- Wideband RF gain block with internal level detectors.

GENERAL DESCRIPTION

The OQ2538HP is a limiting amplifier IC intended for use as the main amplifier in 2.5 Gbits/s Non-Return to Zero (NRZ) transmission systems (SDH/SONET).

Comprised of four amplifier stages with a total gain of 48.5 dB, it provides for a wide input signal dynamic range at a constant CML compatible output level.

Two level-detection circuits are provided for monitoring AGC and LOS input signal levels. An internal automatic offset compensation circuit eliminates offset in the amplifier chain.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OQ2538HP	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM

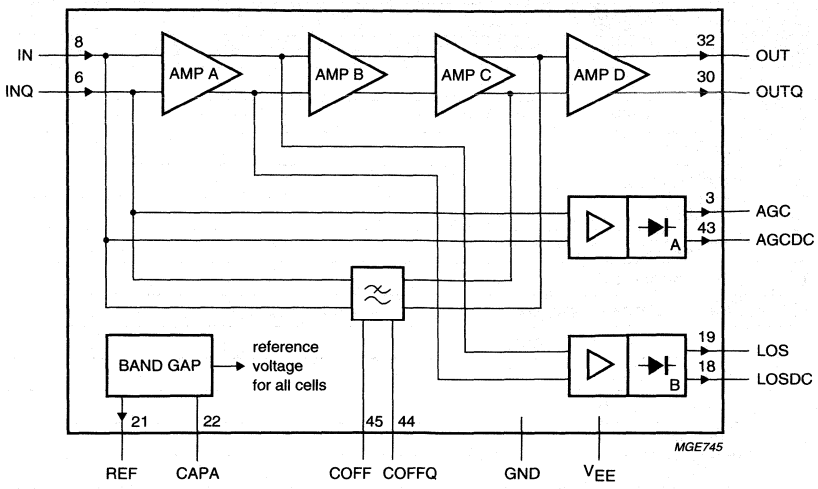


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE[1]
V_{EE}	1	negative power supply	S
n.c.	2	not connected	–
AGC	3	rectifier A output	O
GND	4	ground	S
GND	5	ground	S
INQ	6	main amplifier inverting input	I
GND	7	ground	S
IN	8	main amplifier input	I
GND	9	ground	S
GND	10	ground	S
n.c.	11	not connected	–
V_{EE}	12	negative power supply	S
V_{EE}	13	negative power supply	S
n.c.	14	not connected	–
n.c.	15	not connected	–
GND	16	ground	S
GND	17	ground	S
LOSDC	18	rectifier B reference output	O
LOS	19	rectifier B output	O
GND	20	ground	S
REF	21	band gap reference	O
CAPA	22	pin for connecting band gap reference decoupling capacitor	A
n.c.	23	not connected	–
V_{EE}	24	negative power supply	S
V_{EE}	25	negative power supply	S
n.c.	26	not connected	–
n.c.	27	not connected	–
GND	28	ground	S
GND	29	ground	S
OUTQ	30	main amplifier inverted output	O
GND	31	ground	S
OUT	32	main amplifier output	O
GND	33	ground	S
GND	34	ground	S
n.c.	35	not connected	–
V_{EE}	36	negative power supply	S
V_{EE}	37	negative power supply	S
n.c.	38	not connected	–
GND	39	ground	S
n.c.	40	not connected	–

SYMBOL	PIN	DESCRIPTION	TYPE(1)
GND	41	ground	S
GND	42	ground	S
AGCDC	43	rectifier A reference output	O
COFFQ	44	pin for connecting automatic offset control capacitor (return)	A
COFF	45	pin for connecting automatic offset control capacitor	A
n.c.	46	not connected	–
n.c.	47	not connected	–
V_{EE}	48	negative power supply	S

Note

1. Pin type abbreviations: O = Output, I = Input, S = power Supply, A = Analog function.

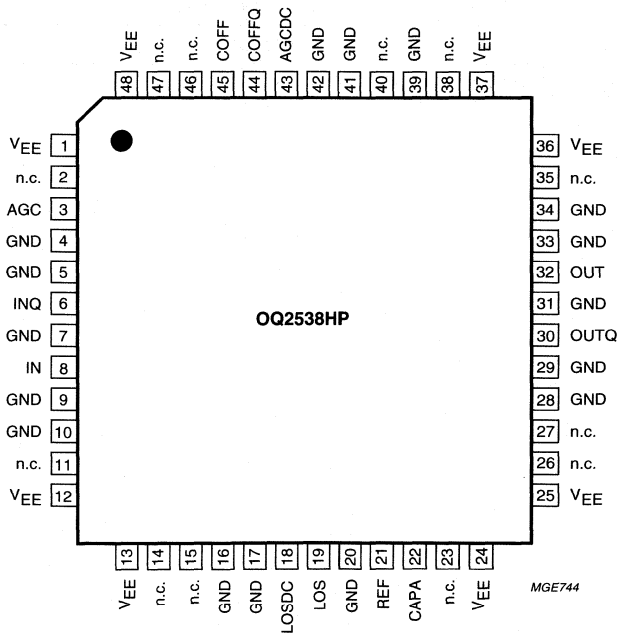


Fig.2 Pin configuration.

SDH/SONET data and clock recovery unit STM1/4/16 OC3/12/48

OQ2541HP

FEATURES

- Data and clock recovery up to 2.5 Gbits/s (STM1/OC3, STM4/OC12 and STM16/OC48)
- Differential data input with 2.5 mV peak-to-peak typical sensitivity
- Differential CML (Current-Mode Logic) data and clock outputs with 50 Ω driving capability
- Adjustable CML output level
- Loop mode for system testing
- BER related LOS detection
- Few external components needed
- LQFP48 plastic package
- Power dissipation typical 350 mW
- Single supply voltage.

DESCRIPTION

The OQ2541HP is a data and clock recovery IC intended for use in SDH (Synchronous Digital Hierarchy) and SONET (Synchronous Optical Network) systems.
The circuit recovers data and extracts the clock signal from an incoming bitstream up to 2.5 Gbits/s. It can be configured for use in STM1/OC3, STM4/OC12 and STM16/OC48 systems.

APPLICATIONS

- Data and clock recovery in STM1/OC3, STM4/OC12 and STM16/OC48 transmission systems (up to 2.5 Gbits/s).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OQ2541HP	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM

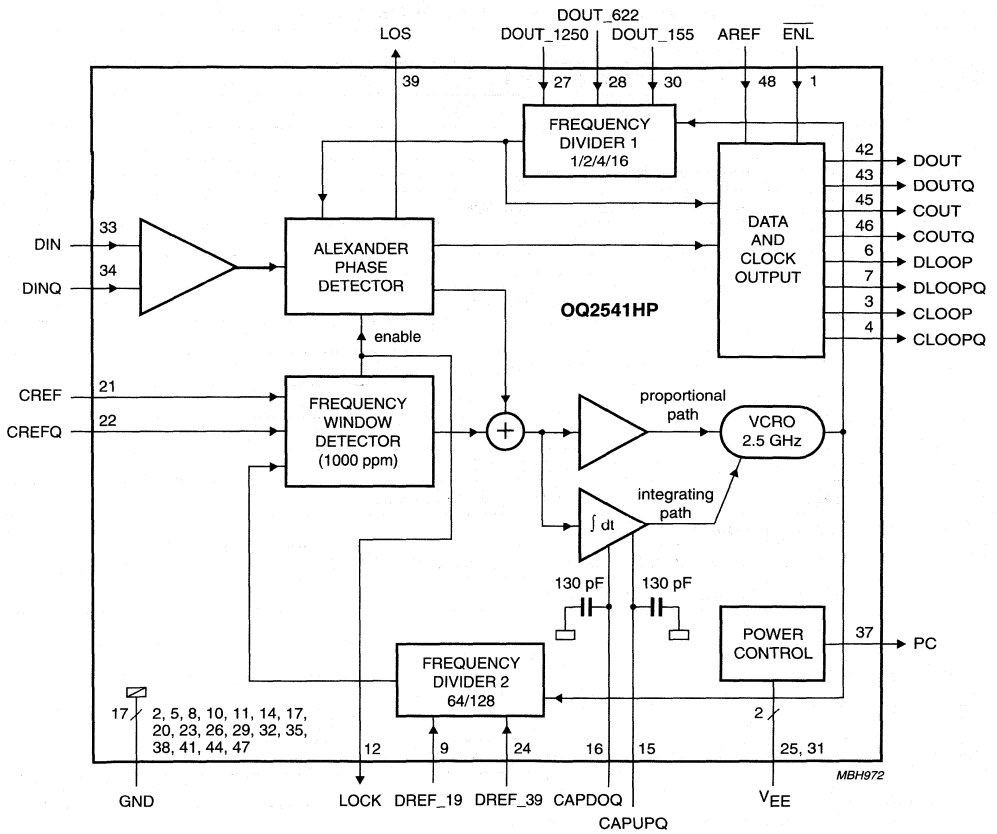


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{ENL}$	1	loop mode enable input (active low)
GND	2	ground
CLOOP	3	clock output in loop mode (differential)
CLOOPQ	4	inverted clock output in loop mode (differential)
GND	5	ground
DLOOP	6	data output in loop mode (differential)
DLOOPQ	7	inverted data output in loop mode (differential)
GND	8	ground
DREF_19	9	reference frequency select input (see Table 1)
GND	10	ground
GND	11	ground
LOCK	12	phase lock detection output
i.c.	13	internally connected (leave open)
GND	14	ground
CAPUPQ	15	external loop filter capacitor
CAPDOQ	16	external loop filter capacitor return
GND	17	ground
i.c.	18	internally connected (leave open)
i.c.	19	internally connected (leave open)
GND	20	ground
CREF	21	reference clock input (differential)
CREFQ	22	inverting reference clock input (differential)
GND	23	ground
DREF_39	24	reference frequency select input (see Table 1)
V_{EE}	25	negative supply voltage
GND	26	ground
DOUT_1250	27	STM mode select input (see Table 2)
DOUT_622	28	STM mode select input (see Table 2)
GND	29	ground
DOUT_155	30	STM mode select input (see Table 2)
V_{EE}	31	negative supply voltage
GND	32	ground
DIN	33	data input (differential)
DINQ	34	inverting data input (differential)
GND	35	ground
i.c.	36	internally connected (leave open)
PC	37	negative power supply control signal output
GND	38	ground
LOS	39	loss-of-signal detection output
i.c.	40	internally connected (leave open)

SYMBOL	PIN	DESCRIPTION
GND	41	ground
DOUT	42	data output in normal mode (differential)
DOUTQ	43	inverted data output in normal mode (differential)
GND	44	ground
COUT	45	clock output in normal mode (differential)
COUTQ	46	inverted clock output in normal mode (differential)
GND	47	ground
AREF	48	reference voltage input for controlling voltage swing on data and clock outputs

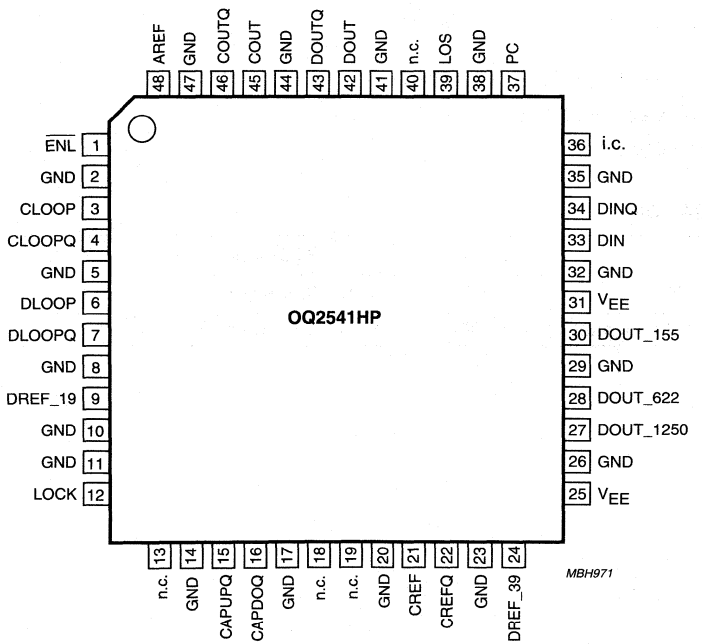


Fig.2 Pin configuration.

SDH/SONET STM16/OC48 laser driver OQ2545HP

FEATURES

- Differential 50 Ω inputs for direct connection to CML (Current-Mode Logic) outputs
- Internal retiming to minimize jitter
- Input clock phase margin of 320° at 2.5 Gbits/s
- RF output current sinking capability of 60 mA for 25 Ω loads and 50 mA for 50 Ω loads
- Bias output current sinking capability of 100 mA
- TTL compatible control inputs
- Loop mode for system testing
- Continuous output monitoring
- Typical power dissipation: 1420 mW
- Low cost LQFP48 plastic package.

APPLICATIONS

- Digital fibre optic modulation driver in STM16/OC48 short, medium and long haul optical transmission systems
- Optical modulation driver in high speed data networks
- High current driver for electro-optical converters
- High current electrical line driver.

GENERAL DESCRIPTION

The OQ2545HP is a driver IC intended to be used with directly modulated laser diodes or with Electro Absorption Modulators (EAMs) in SDH/SONET 2.5 Gbits/s optical transmission systems.

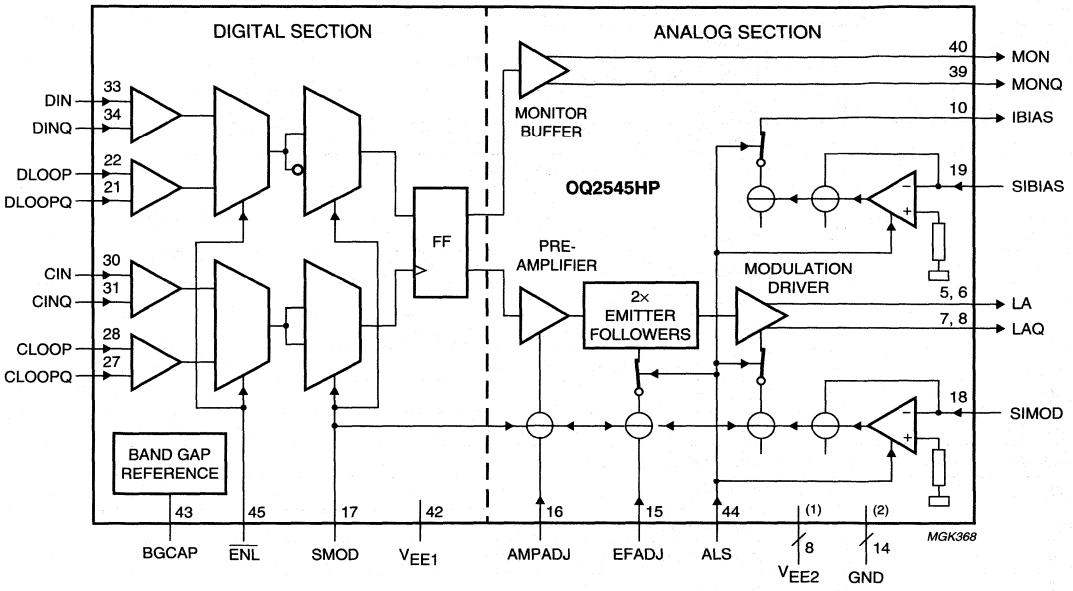
It features differential data and clock inputs and internal retiming for better jitter performance. Loop mode inputs are provided for system testing, along with an output for continuous monitoring.

The high current drive has bias and modulating current outputs, the levels of which can be set separately. As an additional safety measure, the active HIGH ALS (Automatic Laser Shutdown) input can be used to switch off the laser modulation and bias currents. Although the circuit is intended for 2.5 Gbits/s optical transmission systems, it can be used in any application requiring high current drive at high frequencies.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OQ2545HP	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM



(1) Pins 1, 12, 13, 24, 25, 36, 37 and 48

(2) Pins 2, 4, 9, 11, 14, 20, 23, 26, 29, 32, 35, 38, 41 and 47.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE[1]
V_{EE2}	1	supply voltage for analog section	S
GND	2	ground	S
DIOA	3	anode of temperature sensing diode array	A
GND	4	ground	S
LA	5	modulation current output	O
LA	6	modulation current output	O
LAQ	7	modulation current output inverted	O
LAQ	8	modulation current output inverted	O
GND	9	ground	S
IBIAS	10	bias current output	O
GND	11	ground	S
V_{EE2}	12	supply voltage for analog section	S
V_{EE2}	13	supply voltage for analog section	S
GND	14	ground	S
EFADJ	15	input for emitter follower current adjustment	AI
AMPADJ	16	input for preamplifier current adjustment	AI
SMOD	17	data polarity switch	I
SIMOD	18	RF modulated output current adjustment	I
SIBIAS	19	DC output current adjustment	I
GND	20	ground	S
DLOOPQ	21	loop mode data input inverted	I
DLOOP	22	loop mode data input	I
GND	23	ground	S
V_{EE2}	24	supply voltage for analog section	S
V_{EE2}	25	supply voltage for analog section	S
GND	26	ground	S
CLOOPQ	27	loop mode clock input inverted	I
CLOOP	28	loop mode clock input	I
GND	29	ground	S
CIN	30	clock input	I
CINQ	31	clock input inverted	I
GND	32	ground	S
DIN	33	data input	I
DINQ	34	data input inverted	I
GND	35	ground	S
V_{EE2}	36	supply voltage for analog section	S
V_{EE2}	37	supply voltage for analog section	S
GND	38	ground	S
MONQ	39	data monitor output inverted	O
MON	40	data monitor output	O

SYMBOL	PIN	DESCRIPTION	TYPE[1]
GND	41	ground	S
V_{EE1}	42	supply voltage for digital section	S
BGCAP	43	pin for connecting band gap reference decoupling capacitor	A
ALS	44	automatic laser shut down control (active HIGH)	I
$\overline{ENL}$	45	loop mode enable (active LOW)	I
V_{CC}	46	supply voltage for TTL interface	S
GND	47	ground	S
V_{EE2}	48	supply voltage for analog section	S

Note

1. Pin type abbreviations: O = Output, I = Input, S = power Supply, A = Analog function.

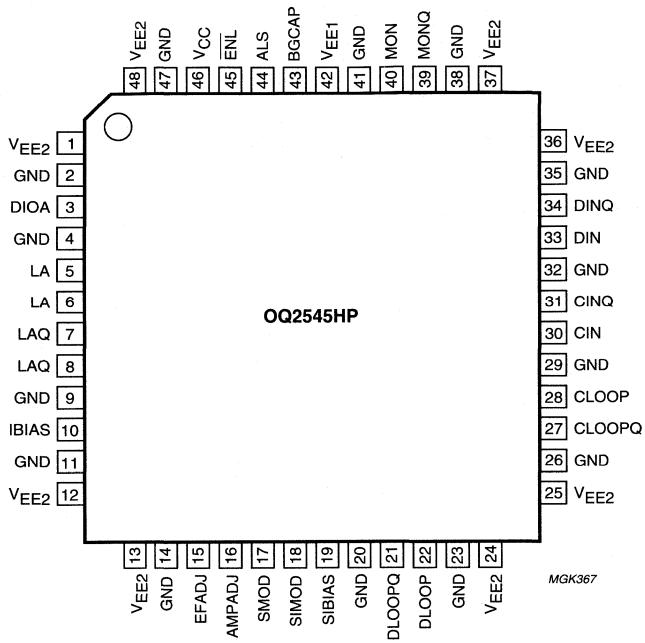


Fig.2 Pin configuration.

SDH/SONET STM1/OC3 optical receiver TZA3030

FEATURES

- Low equivalent input noise, typically 1 pA/√Hz
- Wide dynamic range, typically 0.5 μA to 2 mA
- On-chip low-pass filter. The bandwidth can be varied between 90 and 150 MHz using an external resistor. Default value is 120 MHz.
- Differential transimpedance of 1.8 MΩ
- On-chip Automatic Gain Control (AGC)
- Positive Emitter Coupled Logic (PECL) or Current-Mode Logic (CML) compatible data outputs
- LOS (Loss Of Signal) detection
- LOS threshold level can be adjusted using a single external resistor
- On-chip DC offset compensation
- Single supply voltage from 3.0 to 5.5 V
- Bias voltage for PIN diode.

APPLICATIONS

- Digital fibre optic receiver in short, medium and long haul optical telecommunications transmission systems or in high speed data networks
- Wideband RF gain block.

GENERAL DESCRIPTION

The TZA3030 optical receiver is a low-noise transimpedance amplifier with AGC plus a limiting amplifier designed to be used in SDH/SONET fibre optic links. The TZA3030 amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and converts it to a differential output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3030HL	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1
TZA3030U	–	naked die in waffle pack carriers; die dimensions 1.58 × 1.58 mm	–

BLOCK DIAGRAM

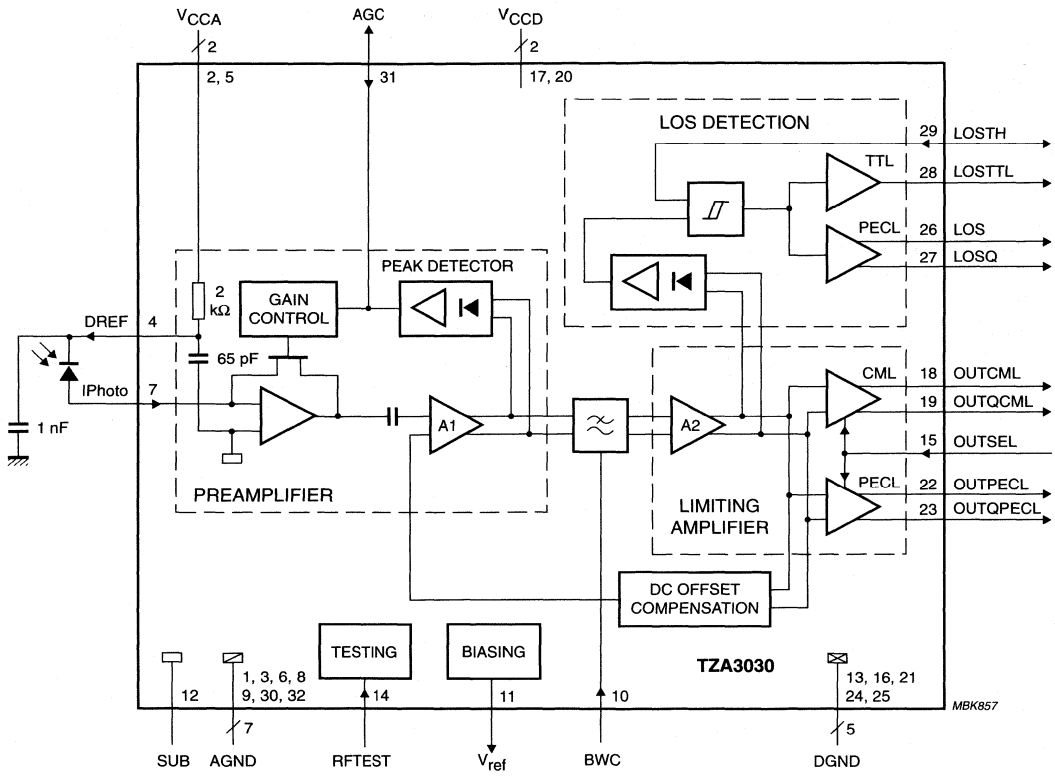


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
AGND	1	ground	analog ground
V_{CCA}	2	supply	analog supply voltage
AGND	3	ground	analog ground
DREF	4	analog output	bias voltage for PIN diode (V_{CCA}); cathode should be connected to this pin
V_{CCA}	5	supply	analog supply voltage
AGND	6	ground	analog ground
IPhoto	7	analog input	current input; connect the anode of PIN diode to this pin; DC bias level is 1048 mV
AGND	8	ground	analog ground
AGND	9	ground	analog ground
BWC	10	analog input	bandwidth control pin; default bandwidth is 120 MHz; a resistor should be connected between V_{ref} (pin 11) and BWC (pin 10) to decrease bandwidth, or between BWC (pin 10) and AGND to increase bandwidth
V_{ref}	11	analog output	band gap reference voltage; nominal value approximately 1.2 V
SUB	12	substrate	substrate pin; to be connected to AGND
DGND	13	ground	digital ground
RFTEST	14	analog input	test pin; not connected; not used in application
OUTSEL	15	CMOS input	output select pin; when OUTSEL is HIGH, CML data outputs are active and PECL data outputs are disabled; OUTSEL is pulled LOW if left unconnected, PECL data outputs will then be active and CML data outputs disabled
DGND	16	ground	digital ground
V_{CCD}	17	supply	digital supply voltage
OUTCML	18	CML output	CML data output; OUTCML goes HIGH when current flows into IPhoto (pin 7)
OUTQCML	19	CML output	CML compliment of OUTCML (pin 18)
V_{CCD}	20	supply	digital supply voltage
DGND	21	ground	digital ground
OUTPECL	22	PECL output	PECL data output; OUTPECL goes HIGH when current flows into IPhoto (pin 7)
OUTQPECL	23	PECL output	PECL compliment of OUTPECL (pin 22)
DGND	24	ground	digital ground
DGND	25	ground	digital ground
LOS	26	PECL output	PECL-compatible LOS detection pin; LOS output is HIGH when the input signal is below the user programmable threshold level
LOSQ	27	PECL output	PECL compliment of LOS (pin 26)
LOSTTL	28	TTL output	CMOS-compatible LOS detection pin; the LOSTTL output is HIGH when the input signal is below the user programmable threshold level
LOSTH	29	analog I/O	pin for setting input threshold level; nominal DC voltage is $V_{CCA} - 1.5$ V; threshold level set by connecting an external resistor between LOSTH and V_{CCA} or by forcing a current into LOSTH; default value for this resistor is 400 kΩ
AGND	30	ground	analog ground
AGC	31	analog I/O	AGC monitor voltage; the internal AGC circuit can be disabled by applying an external voltage to this pin
AGND	32	ground	analog ground

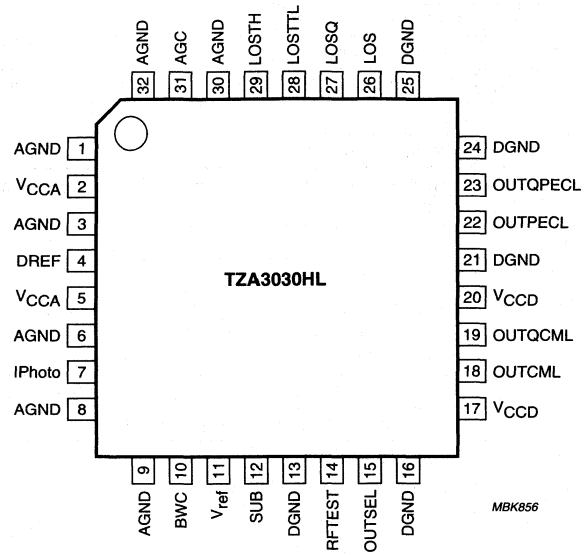


Fig.2 Pin configuration.

SDH/SONET STM1/OC3 laser drivers

TZA3031AHL; TZA3031BHL; TZA3031U

FEATURES

- 155 Mbits/s data input, both Current-Mode Logic (CML) and Positive Emitter Coupled Logic (PECL) compatible; maximum 800 mV (peak-to-peak value)
- Adaptive laser output control, stabilizing optical ONE and ZERO levels
- Optional external (non-adaptive) control of laser modulation and biasing currents
- Automatic Laser Shutdown (ALS)
- Few external components required
- Rise and fall times typically 120 ps
- Jitter <50 mUI (peak-to-peak value)
- RF output current sinking capability of 60 mA
- Bias current sinking capability of 90 mA
- Power dissipation typically 475 mW
- Low cost LQFP32 plastic package
- Single 5 V power supply.

TZA3031AHL

- Laser alarm output for signalling extremely low and high bias current conditions.

TZA3031BHL

- Loop mode for testing STM1 155 Mbits/s optical interfaces; CML and PECL compatible.

TZA3031U

- Naked die version with combined bias alarm and loop mode functionality.

APPLICATIONS

- SDH/SONET STM1/OC3 optical transmission systems
- SDH/SONET STM1/OC3 optical laser modules.

DESCRIPTION

The TZA3031AHL, TZA3031BHL and TZA3031U are fully integrated laser drivers for STM1/OC3 (155 Mbits/s) systems, incorporating the RF path between the data multiplexer and the laser diode. Since the bias and modulation control circuits are integrated on the IC, the external component count is low (only decoupling capacitors and adjustment resistors are required).

The TZA3031AHL features an alarm function for signalling extreme bias current conditions. The alarm low and high threshold levels can be adjusted to suit the application using only a resistor. An additional RF data input is provided with the TZA3031BHL to facilitate remote (loop mode) system testing.

The TZA3031U is a naked die version for use in compact laser module designs. The die contains 40 pads and features the combined functionality of the TZA3031AHL and TZA3031BHL.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3031AHL	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1
TZA3031BHL			
TZA3031U	–	naked die; 2000 × 2000 × 380 μm	–

BLOCK DIAGRAMS

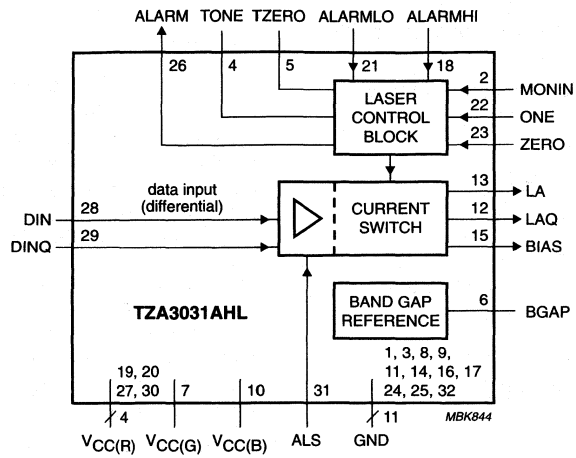


Fig.1 Block diagram: TZA3031AHL.

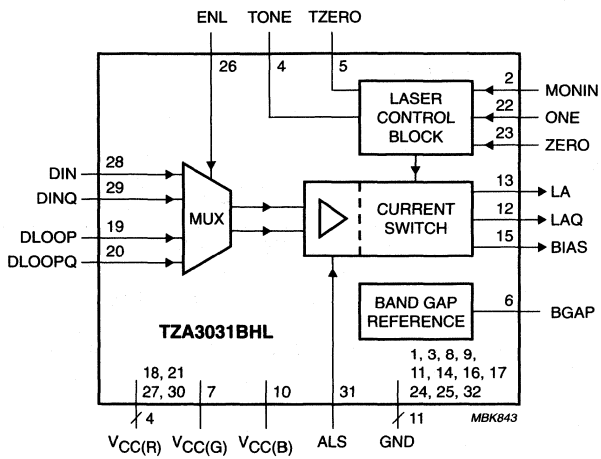


Fig.2 Block diagram: TZA3031BHL.

PINNING

TZA3031AHL

SYMBOL	PIN	DESCRIPTION
GND	1	ground
MONIN	2	monitor photodiode current input
GND	3	ground
TONE	4	connection for external capacitor used to set optical ONE control loop time constant (optional)
TZERO	5	connection for external capacitor used to set optical ZERO control loop time constant (optional)
BGAP	6	connection for external band gap decoupling capacitor
$V_{CC(G)}$	7	supply voltage; note 1
GND	8	ground
GND	9	ground
$V_{CC(B)}$	10	supply voltage; note 1
GND	11	ground
LAQ	12	inverted laser modulation output
LA	13	laser modulation output
GND	14	ground
BIAS	15	laser bias current output
GND	16	ground
GND	17	ground
ALARMHI	18	maximum bias current alarm reference level input
$V_{CC(R)}$	19	supply voltage; note 1
$V_{CC(R)}$	20	supply voltage; note 1
ALARMLO	21	minimum bias current alarm reference level input
ONE	22	optical ONE reference level input
ZERO	23	optical ZERO reference level input
GND	24	ground
GND	25	ground
ALARM	26	alarm output
$V_{CC(R)}$	27	supply voltage; note 1
DIN	28	data input
DINQ	29	inverted data input
$V_{CC(R)}$	30	supply voltage; note 1
ALS	31	automatic laser shutdown input
GND	32	ground

TZA3031BHL

SYMBOL	PIN	DESCRIPTION
GND	1	ground
MONIN	2	monitor photodiode current input
GND	3	ground
TONE	4	connection for external capacitor used to set optical ONE control loop time constant (optional)
TZERO	5	connection for external capacitor used to set optical ZERO control loop time constant (optional)
BGAP	6	connection for external band gap decoupling capacitor
$V_{CC(G)}$	7	supply voltage; note 1
GND	8	ground
GND	9	ground
$V_{CC(B)}$	10	supply voltage; note 1
GND	11	ground
LAQ	12	inverted laser modulation output
LA	13	laser modulation output
GND	14	ground
BIAS	15	laser bias current output
GND	16	ground
GND	17	ground
$V_{CC(R)}$	18	supply voltage; note 1
DLOOP	19	loop mode data input
DLOOPQ	20	loop mode inverted data input
$V_{CC(R)}$	21	supply voltage; note 1
ONE	22	optical ONE reference level input
ZERO	23	optical ZERO reference level input
GND	24	ground
GND	25	ground
ENL	26	loop mode enable input
$V_{CC(R)}$	27	supply voltage; note 1
DIN	28	data input
DINQ	29	inverted data input
$V_{CC(R)}$	30	supply voltage; note 1
ALS	31	automatic laser shutdown input
GND	32	ground

Note to Tables TZA3031AHL and TZA3031BHL

1. See Section "Power supply connections".

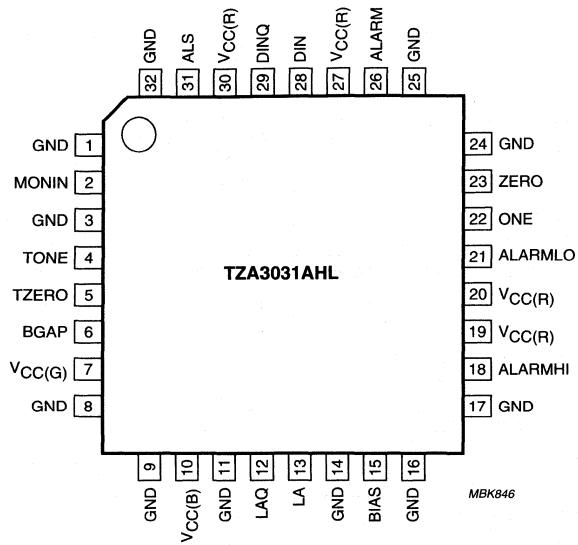


Fig.3 Pin configuration: TZA3031AHL.

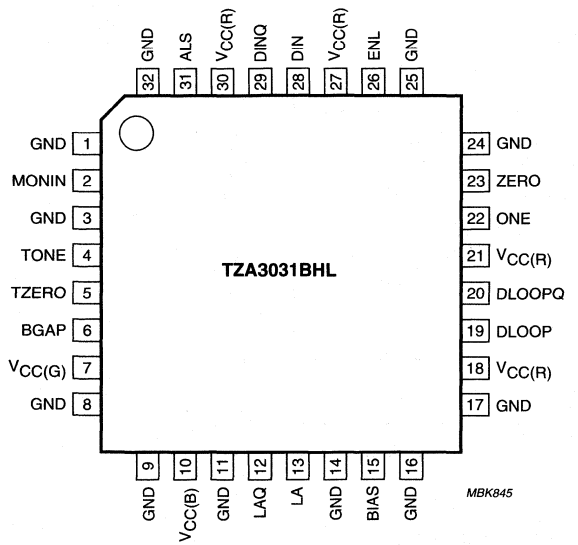


Fig.4 Pin configuration: TZA3031BHL.

SDH/SONET STM1/OC3 transimpedance amplifier TZA3033

FEATURES

- Low equivalent input noise, typically 1 pA/√Hz
- Wide dynamic range, typically 0.25 μA to 1.6 mA
- Differential transimpedance of 117 kΩ
- Bandwidth minimum 150 MHz
- Differential outputs
- On-chip AGC (Automatic Gain Control)
- No external components required
- Single supply voltage from 3.0 to 5.5 V
- Bias voltage for PIN diode
- Pin compatible with SA5223.

APPLICATIONS

- Digital fibre optic receiver in short, medium and long haul optical telecommunications transmission systems or in high speed data networks
- Wideband RF gain block.

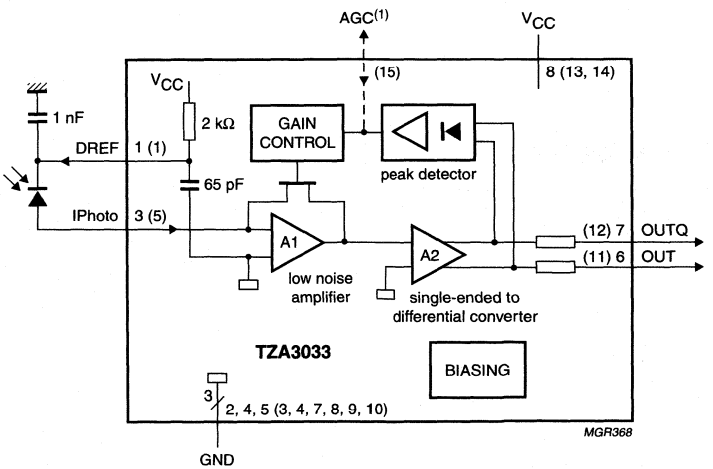
GENERAL DESCRIPTION

The TZA3033 is a low-noise transimpedance amplifier with AGC designed to be used in STM1/OC3 fibre optic links. It amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and converts it to a differential output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3033T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TZA3033U	naked die	die in waffle pack carriers; die dimensions 0.960 × 1.210 mm	–

BLOCK DIAGRAM



(1) AGC analog I/O is only available on the TZA3033U (pad 15).
The numbers in brackets refer to the pad numbers of the naked die version.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
DREF	1	analog output	bias voltage for PIN diode (V_{CC}); cathode should be connected to this pin
GND	2	ground	ground
IPhoto	3	analog input	current input; anode of PIN diode should be connected to this pin; DC bias voltage is 1048 mV
GND	4	ground	ground
GND	5	ground	ground
OUT	6	data output	data output; OUT goes HIGH when current flows into IPhoto (pin 3)
OUTQ	7	data output	compliment of OUT (pin 6)
V_{CC}	8	supply	supply voltage

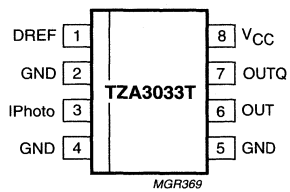


Fig.2 Pin configuration.

SDH/SONET STM1/OC3 postamplifiers TZA3034T; TZA3034U

FEATURES

- Pin compatible with the NE/SA5224 and NE/SA5225 but with extended power supply range and less external component count
- Wideband operation from 1.0 kHz to 150 MHz typical
- Applicable in 155 Mbits/s SDH/SONET receivers
- Single supply voltage from 3.0 to 5.5 V
- PECL (Positive Emitter Coupled Logic) compatible data outputs
- Programmable input signal level-detection which can be adjusted using a single external resistor
- On-chip DC offset compensation without external capacitor
- Fully differential for excellent PSRR.

APPLICATIONS

- Digital fibre optic receiver in short, medium and long haul optical telecommunications transmission systems or in high speed data networks
- Wideband RF gain block.

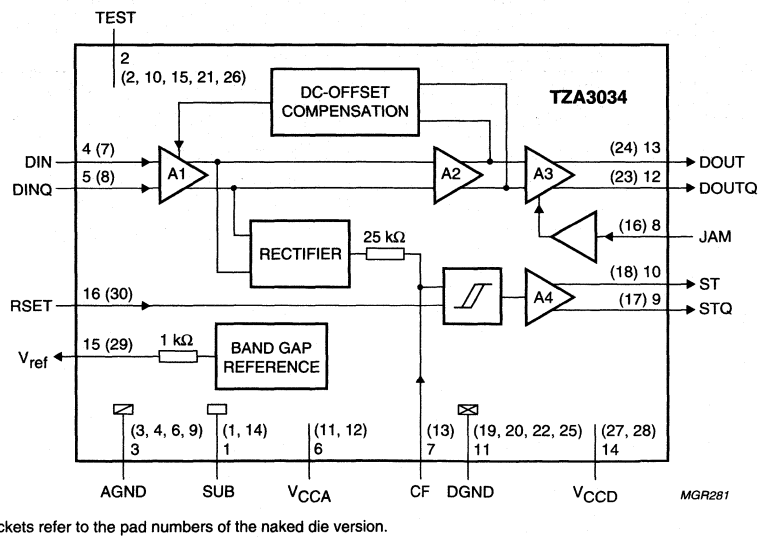
GENERAL DESCRIPTION

The TZA3034 is a high gain limiting amplifier that is designed to process signals from fibre optic preamplifiers like the TZA3033. It is pin compatible with the NE/SA5224 and NE/SA5225 but with extended power supply range, and needs less external components. Capable of operating at 155 Mbits/s, the chip has input signal level detection with a user-programmable threshold. The data and level-detection status outputs are differential outputs for optimum noise margin and ease of use.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3034T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TZA3034U	naked die	die in waffle pack carriers; die dimensions 1.58 × 1.58 mm	–

BLOCK DIAGRAM



The numbers in brackets refer to the pad numbers of the naked die version.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
SUB	1	substrate	substrate pin; must be at the same potential as AGND (pin 3)
TEST	2	test pin	for test purpose only; to be left open in the application
AGND	3	ground	analog ground; must be at the same potential as DGND (pin 11)
DIN	4	analog input	differential input; DC bias level is set internally at approximately 2.55 V; complimentary to DINQ (pin 5)
DINQ	5	analog input	differential input; DC bias level is set internally at approximately 2.55 V; complimentary to DIN (pin 4)
V_{CCA}	6	supply	analog supply voltage; must be at the same potential as V_{CCD} (pin 14)
CF	7	analog input	filter capacitor for input signal level detector; capacitor should be connected between this pin and V_{CCA} (pin 6)
JAM	8	PECL input	PECL-compatible input; controls the output buffers DOUT and DOUTQ (pins 13 and 12). When a LOW signal is applied, the outputs will follow the input signal3 When a HIGH signal is applied, the DOUT and DOUTQ pins will latch into LOW and HIGH states, respectively. When left unconnected, this pin is actively pulled LOW (JAM OFF).
STQ	9	PECL output	PECL-compatible status output of the input signal level detector; when the input signal is below the user-programmed threshold level, this output is HIGH; complimentary to ST (pin 10)
ST	10	PECL output	PECL-compatible status output of the input signal level detector; when the input signal is below the user-programmed threshold level, this output is LOW; complimentary to STQ (pin 9)
DGND	11	ground	digital ground; must be at the same potential as AGND (pin 3)
DOUTQ	12	PECL output	PECL-compatible differential output; when JAM is HIGH, this pin will be forced into a HIGH condition; complimentary to DOUT (pin 13)
DOUT	13	PECL output	PECL-compatible differential output; when JAM is HIGH, this pin will be forced into a LOW condition; complimentary to DOUTQ (pin 12)
V_{CCD}	14	supply	digital supply voltage; must be at the same potential as V_{CCA} (pin 6)
V_{ref}	15	analog output	band gap reference voltage; typical value is 1.2 V; internal series resistor of 1 kΩ
RSET	16	analog input	input signal level detector programming; nominal DC voltage is $V_{CCA} - 1.5$ V; threshold level is set by connecting an external resistor between RSET and V_{CCA} or by forcing a current into RSET; default value for this resistor is 180 kΩ which corresponds with approximately 4 mV (p-p) differential input signal

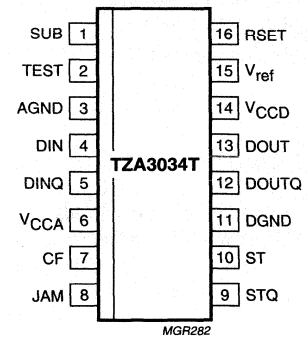


Fig.2 Pin configuration.

SDH/SONET STM4/OC12 optical receiver TZA3000

FEATURES

- Low equivalent input noise, typically 3.5 pA/√Hz
- Wide dynamic range, typically 1 μA to 1.5 mA
- On-chip low-pass filter. The bandwidth can be varied between 370 and 600 MHz using an external resistor. Default value is 470 MHz.
- Differential transimpedance of 1.8 MΩ
- On-chip AGC (Automatic Gain Control)
- PECL (Positive Emitter-Coupled Logic) or CML (Current-Mode Logic) compatible data outputs
- LOS (Loss-Of-Signal) detection
- LOS threshold level can be adjusted using a single external resistor
- On-chip DC offset compensation
- Single supply voltage from 3.0 to 5.5 V
- Bias voltage for PIN diode.

APPLICATIONS

- Digital fibre optic receiver in short, medium and long haul optical telecommunications transmission systems or in high speed data networks
- Wideband RF gain block.

DESCRIPTION

The TZA3000 optical receiver is a low-noise transimpedance amplifier with AGC plus a limiting amplifier designed to be used in SDH/SONET fibre optic links. The TZA3000 amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and converts it to a differential output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3000HL	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1
TZA3000U	naked die	die in waffle pack carriers; die dimensions 1.58 × 1.58 mm	–

BLOCK DIAGRAM

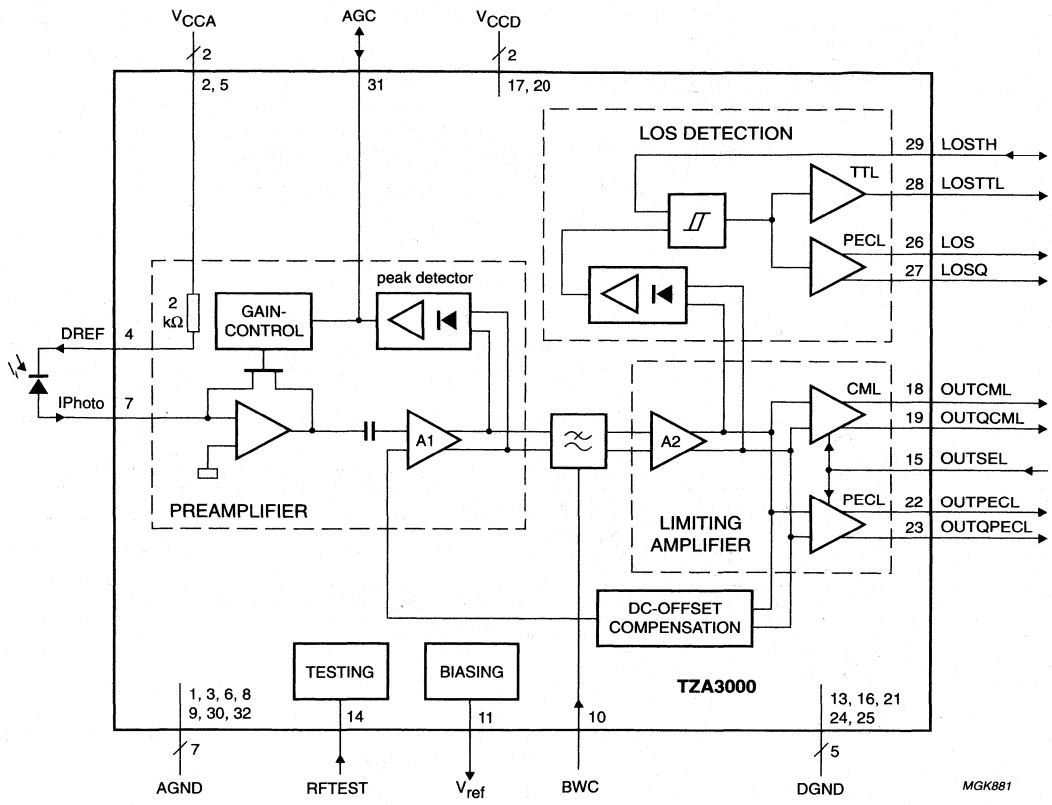


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
AGND	1	ground	analog ground
V_{CCA}	2	supply	analog supply voltage
AGND	3	ground	analog ground
DREF	4	analog output	bias voltage for PIN diode (V_{CCA}); cathode should be connected to this pin
V_{CCA}	5	supply	analog supply voltage
AGND	6	ground	analog ground
IPhoto	7	analog input	current input; connect the anode of PIN diode to this pin; DC bias level is 800 mV, one diode voltage above ground
AGND	8	ground	analog ground
AGND	9	ground	analog ground
BWC	10	analog input	bandwidth control pin; default bandwidth is 470 MHz; a resistor should be connected between V_{ref} (pin 11) and BWC (pin 10) to decrease bandwidth, or between BWC (pin 10) and AGND to increase bandwidth
V_{ref}	11	analog output	band gap reference voltage; nominal value approximately 1.2 V
SUB	12	substrate	substrate pin; to be connected to AGND
DGND	13	ground	digital ground
RFTEST	14	analog input	test pin; not used in application; not connected
OUTSEL	15	CMOS input	output select pin; when OUTSEL is HIGH, CML data outputs are active and PECL data outputs are disabled; OUTSEL is pulled LOW if left unconnected, PECL data outputs will then be active and CML data outputs disabled
DGND	16	ground	digital ground
V_{CCD}	17	supply	digital supply voltage
OUTCML	18	CML output	CML data output; OUTCML goes HIGH when current flows into IPhoto (pin 7)
OUTQCML	19	CML output	CML compliment of OUTCML (pin 18)
V_{CCD}	20	supply	digital supply voltage
DGND	21	ground	digital ground
OUTPECL	22	PECL output	PECL data output; OUTPECL goes HIGH when current flows into IPhoto (pin 7)
OUTQPECL	23	PECL output	PECL compliment of OUTPECL (pin 22)
DGND	24	ground	digital ground
DGND	25	ground	digital ground
LOS	26	PECL output	PECL-compatible LOS detection pin; LOS output is HIGH when the input signal is below the user programmable threshold level
LOSQ	27	PECL output	PECL compliment of LOS
LOSTTL	28	TTL output	CMOS-compatible LOS detection pin; the LOSTTL output is HIGH when the input signal is below the user programmable threshold level
LOSTH	29	analog I/O	pin for setting input threshold level; nominal DC voltage is $V_{CCA} - 1.5$ V; threshold level set by connecting an external resistor between LOSTH and V_{CCA} or by forcing a current into LOSTH; default value for this resistor is 86 kΩ
AGND	30	ground	analog ground
AGC	31	analog I/O	AGC monitor voltage; the internal AGC circuit can be disabled by applying an external voltage to this pin
AGND	32	ground	analog ground

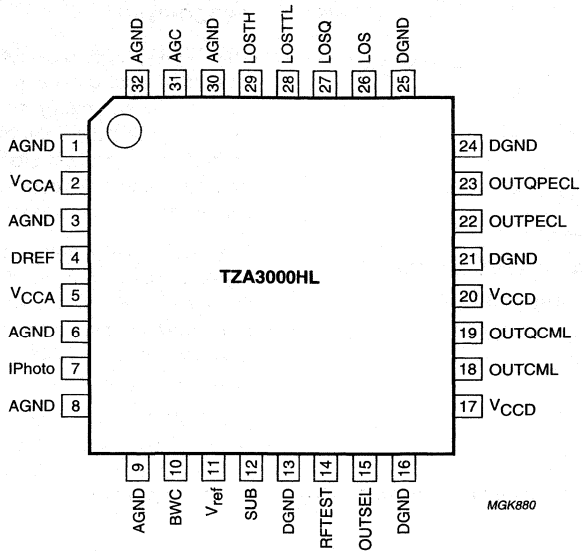


Fig.2 Pin configuration.

SDH/SONET STM4/OC12 laser drivers

TZA3001AHL; TZA3001BHL; TZA3001U

FEATURES

- 622 Mbits/s data input, both Current-Mode Logic (CML) and Positive Emitter-Coupled Logic (PECL) compatible (800 mV peak-to-peak maximum)
- Adaptive laser output control, stabilizing optical ONE and ZERO levels
- Optional external (non-adaptive) control of laser modulation and biasing currents
- Automatic Laser Shutdown (ALS)
- Few external components required
- Rise and fall times typically 120 ps
- Jitter <50 mUI peak-to-peak
- RF output current sinking capability of 60 mA
- Bias current sinking capability of 90 mA
- Power dissipation typically 475 mW
- Low cost LQFP32 plastic package
- Single 5 V power supply.

TZA3001AHL

- Laser alarm output for signalling extremely low and high bias current conditions.

TZA3001BHL

- Loop mode for testing STM4 622 Mbits/s optical interfaces; CML and PECL compatible.

TZA3001U

- Naked die version with combined bias alarm and loop mode functionality.

DESCRIPTION

The TZA3001AHL, TZA3001BHL and TZA3001U are fully integrated laser drivers for STM4/OC12 (622 Mbits/s) systems, incorporating the RF path between the data multiplexer and the laser diode. Since the bias and modulation control circuits are integrated on the IC, the external component count is low (only decoupling capacitors and adjustment resistors are required).

The TZA3001AHL features an alarm function for signalling extreme bias current conditions. The alarm low and high threshold levels can be adjusted to suit the application using only a resistor. An additional RF data input is provided with the TZA3001BHL to facilitate remote (loop mode) system testing.

The TZA3001U is a naked die version for use in compact laser module designs. The die contains 40 pads and features the combined functionality of the TZA3001AHL and TZA3001BHL.

APPLICATIONS

- SDH/SONET STM4/OC12 optical transmission systems
- SDH/SONET STM4/OC12 optical laser modules.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3001AHL	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1
TZA3001BHL	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1
TZA3001U	–	naked die; 2000 × 2000 × 380 μm	–

BLOCK DIAGRAMS

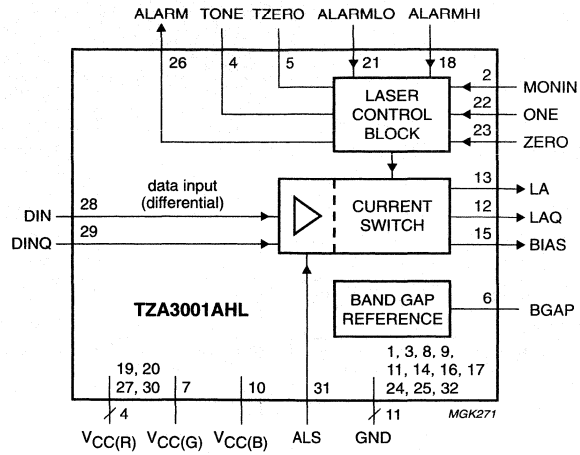


Fig.1 Block diagram: TZA3001AHL.

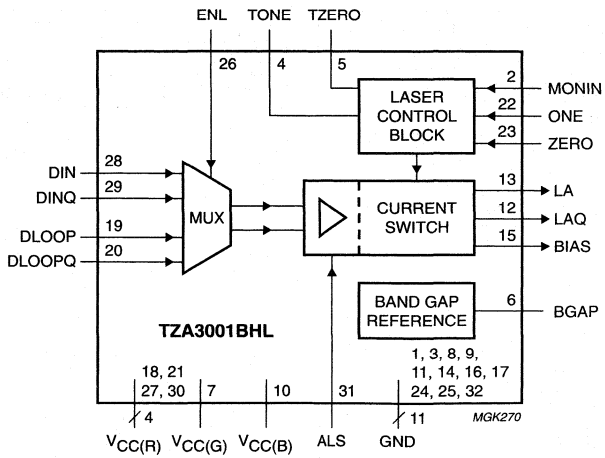


Fig.2 Block diagram: TZA3001BHL.

PINNING

TZA3001AHL

SYMBOL	PIN	DESCRIPTION
GND	1	ground
MONIN	2	monitor photo diode current input
GND	3	ground
TONE	4	connection for external capacitor used to set optical ONE control loop time constant (optional)
TZERO	5	connection for external capacitor used to set optical ZERO control loop time constant (optional)
BGAP	6	connection for external band gap decoupling capacitor
$V_{CC(G)}$	7	supply voltage; note 1
GND	8	ground
GND	9	ground
$V_{CC(B)}$	10	supply voltage; note 1
GND	11	ground
LAQ	12	inverted laser modulation output
LA	13	laser modulation output
GND	14	ground
BIAS	15	laser bias current output
GND	16	ground
GND	17	ground
ALARMHI	18	maximum bias current alarm reference level input
$V_{CC(R)}$	19	supply voltage; note 1
$V_{CC(R)}$	20	supply voltage; note 1
ALARMLO	21	minimum bias current alarm reference level input
ONE	22	optical ONE reference level input
ZERO	23	optical ZERO reference level input
GND	24	ground
GND	25	ground
ALARM	26	alarm output
$V_{CC(R)}$	27	supply voltage; note 1
DIN	28	data input
DINQ	29	inverted data input
$V_{CC(R)}$	30	supply voltage; note 1
ALS	31	automatic laser shutdown input
GND	32	ground

TZA3001BHL

SYMBOL	PIN	DESCRIPTION
GND	1	ground
MONIN	2	monitor photo diode current input
GND	3	ground
TONE	4	connection for external capacitor used to set optical ONE control loop time constant (optional)
TZERO	5	connection for external capacitor used to set optical ZERO control loop time constant (optional)
BGAP	6	connection for external band gap decoupling capacitor
$V_{CC(G)}$	7	supply voltage; note 1
GND	8	ground
GND	9	ground
$V_{CC(B)}$	10	supply voltage; note 1
GND	11	ground
LAQ	12	inverted laser modulation output
LA	13	laser modulation output
GND	14	ground
BIAS	15	laser bias current output
GND	16	ground
GND	17	ground
$V_{CC(R)}$	18	supply voltage; note 1
DLOOP	19	loop mode data input
DLOOPQ	20	loop mode inverted data input
$V_{CC(R)}$	21	supply voltage; note 1
ONE	22	optical ONE reference level input
ZERO	23	optical ZERO reference level input
GND	24	ground
GND	25	ground
ENL	26	loop mode enable input
$V_{CC(R)}$	27	supply voltage; note 1
DIN	28	data input
DINQ	29	inverted data input
$V_{CC(R)}$	30	supply voltage; note 1
ALS	31	automatic laser shutdown input
GND	32	ground

Note to Tables TZA3001AHL and TZA3001BHL

1. See Section "Power supply connections".

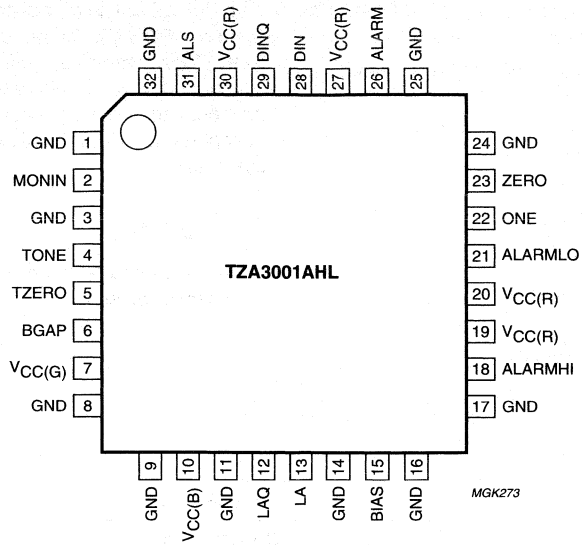


Fig.3 Pin configuration: TZA3001AHL.

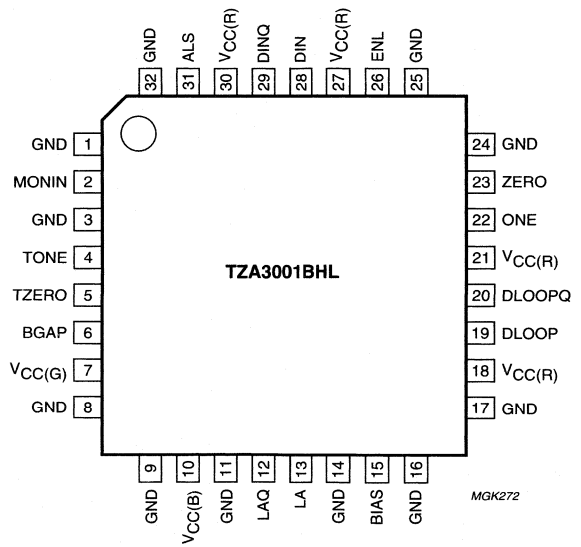


Fig.4 Pin configuration: TZA3001BHL.

SDH/SONET data and clock recovery unit STM1/4 OC3/12

TZA3004HL

FEATURES

- Data and clock recovery up to 622 Mbits/s (STM1/OC3 and STM4/OC12)
- Differential data input with 2.5 mV peak-to-peak typical sensitivity
- Differential CML (Current-Mode Logic) data and clock outputs with 50 Ω driving capability
- Adjustable CML output level
- Loop mode for system testing
- BER related LOS detection
- Few external components needed
- LQFP48 plastic package
- Power dissipation typical 370 mW
- Single supply voltage.

DESCRIPTION

The TZA3004HL is a data and clock recovery IC intended for use in SDH (Synchronous Digital Hierarchy) and SONET (Synchronous Optical Network) systems.
The circuit recovers data and extracts the clock signal from an incoming bitstream up to 622 Mbits/s. It can be configured for use in STM1/OC3 and STM4/OC12 systems.

APPLICATIONS

- Data and clock recovery in STM1/OC3 and STM4/OC12 transmission systems (up to 622 Mbits/s).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3004HL	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM

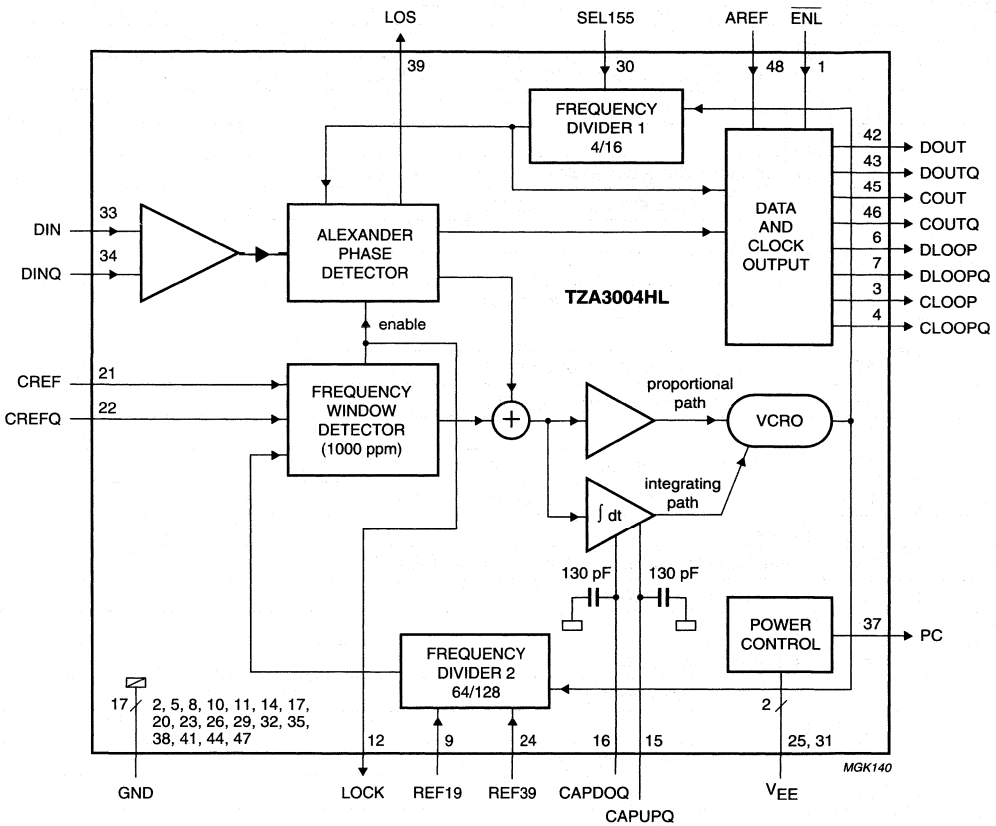


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{ENL}$	1	loop mode enable input (active low)
GND	2	ground
CLOOP	3	clock output in loop mode (differential)
CLOOPQ	4	inverted clock output in loop mode (differential)
GND	5	ground
DLOOP	6	data output in loop mode (differential)
DLOOPQ	7	inverted data output in loop mode (differential)
GND	8	ground
REF19	9	reference frequency select input (see Table 2)
GND	10	ground
GND	11	ground
LOCK	12	phase lock detection output
i.c	13	internally connected (leave open)
GND	14	ground
CAPUPQ	15	external loop filter capacitor
CAPDOQ	16	external loop filter capacitor return
GND	17	ground
i.c.	18	internally connected (leave open)
i.c.	19	internally connected (leave open)
GND	20	ground
CREF	21	reference clock input (differential)
CREFQ	22	inverting reference clock input (differential)
GND	23	ground
REF39	24	reference frequency select input (see Table 2)
V_{EE}	25	negative supply voltage
GND	26	ground
V_{EE}	27	negative supply voltage
V_{EE}	28	negative supply voltage
GND	29	ground
SEL155	30	STM mode select input (see Table 1)
V_{EE}	31	negative supply voltage
GND	32	ground
DIN	33	data input (differential)
DINQ	34	inverting data input (differential)
GND	35	ground
i.c.	36	internally connected (leave open)
PC	37	negative power supply control signal output
GND	38	ground
LOS	39	loss-of-signal detection output
i.c.	40	internally connected (leave open)

SYMBOL	PIN	DESCRIPTION
GND	41	ground
DOUT	42	data output in normal mode (differential)
DOUTQ	43	inverted data output in normal mode (differential)
GND	44	ground
COUT	45	clock output in normal mode (differential)
COUTQ	46	inverted clock output in normal mode (differential)
GND	47	ground
AREF	48	reference voltage input for controlling voltage swing on data and clock outputs

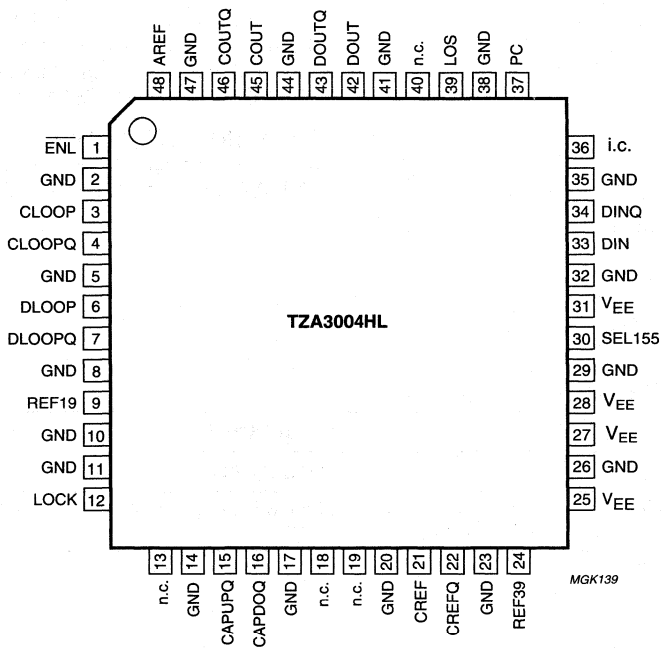


Fig.2 Pin configuration.

SDH/SONET STM1/OC3 and STM4/OC12 transceiver

TZA3005

FEATURES

- Supports STM1/OC3 (155.52 Mbits/s) and STM4/OC12 (622.08 Mbits/s)
- Supports 19.44, 38.88, 51.84 and 77.76 MHz reference clock frequencies
- Meets Bellcore, ANSI and ITU-T specifications
- Integral high-frequency PLL for clock generation
- Interface to TTL logic
- Low jitter PECL (Positive Emitter Coupled Logic) interface.
- 4- or 8-bit STM1/OC3 TTL/CMOS data path
- 4- or 8-bit STM4/OC12 TTL/CMOS data path
- No external filter components required
- QFP64 package
- Diagnostic and line loopback modes
- Lock detect
- LOS (Loss of Signal) input
- Low power (900 mW typically)

APPLICATIONS

- SDH/SONET modules
- SDH/SONET-based transmission systems
- SDH/SONET test equipment
- ATM over SDH/SONET
- Add drop multiplexers
- Broadband cross-connects
- Section repeaters
- Fiber optic test equipment.
- Fiber optic terminators

GENERAL DESCRIPTION

The TZA3005 SDH/SONET transceiver chip is a fully integrated serialization/deserialization SDH/SONET STM4/OC12 (622.08 Mbits/s) and STM1/OC3 (155.52 Mbits/s) interface device. It performs all necessary serial-to-parallel and parallel-to-serial functions in accordance with SDH/SONET transmission standards. It is suitable for SONET-based applications and can be used in conjunction with the TZA3004 clock recovery device, the TZA3000 optical receiver and the TZA3001 laser driver. Figure 13 shows a typical network application.

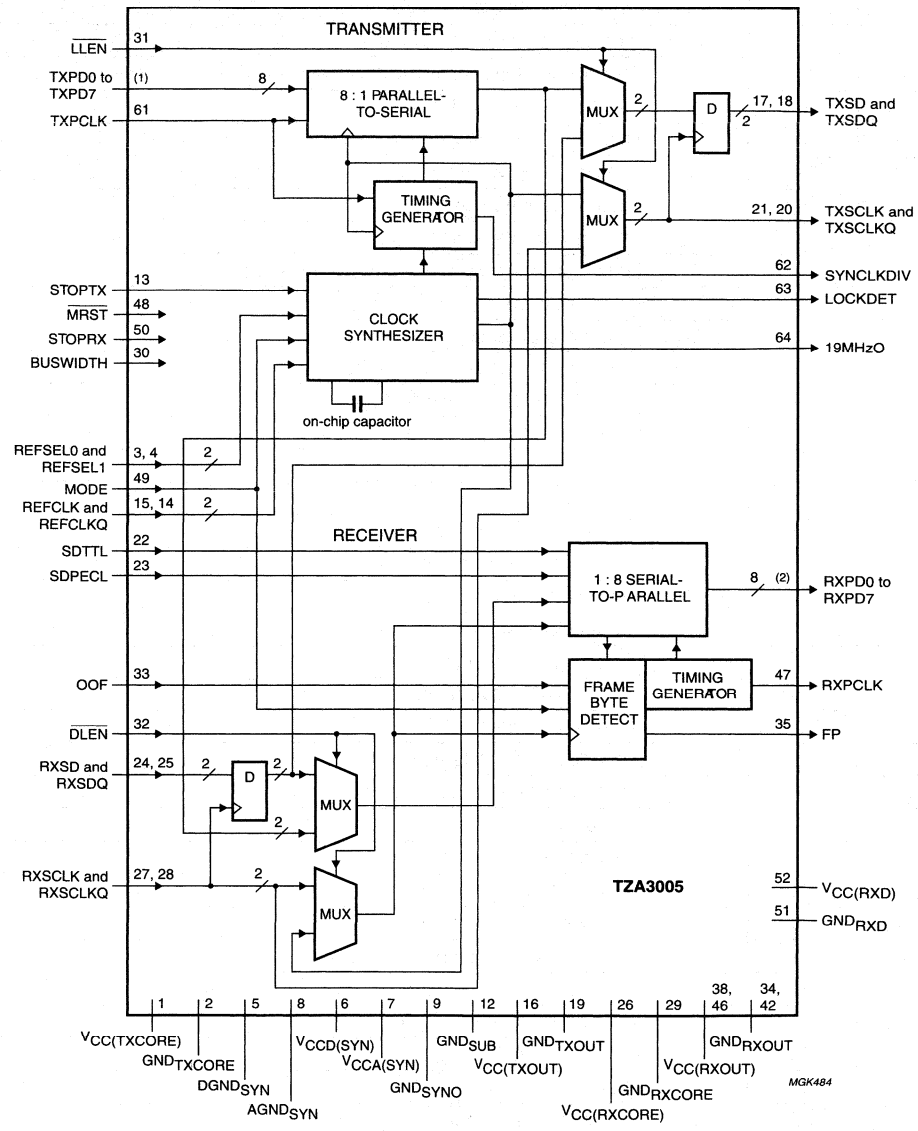
A high-frequency phase-locked loop is used for on-chip clock synthesis, which means a slower external transmit reference clock can be used. A 19.44, 38.88, 51.84 or 77.76 MHz reference clock can be used, in support of existing system clocking schemes. The TZA3005 performs SDH/SONET frame detection.

The low jitter PECL interface ensures that Bellcore, ANSI, and ITU-T bit-error rate requirements are satisfied. The TZA3005 comes in a compact QFP64 package.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3005H	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1

BLOCK DIAGRAM



(1) Pins 53 to 60.

(2) Pins 36, 37, 39, 40, 41, 43, 44 and 45.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE[1]	DESCRIPTION
$V_{CC(TXCORE)}$	1	S	supply voltage (transmitter core)
GND_{TXCORE}	2	S	ground (transmitter core)
REFSEL0	3	I	reference clock select input 0
REFSEL1	4	I	reference clock select input 1
$DGND_{SYN}$	5	S	digital ground (synthesizer)
$V_{CCD(SYN)}$	6	S	digital supply voltage (synthesizer)
$V_{CCA(SYN)}$	7	S	analog supply voltage (synthesizer)
$AGND_{SYN}$	8	S	analog ground (synthesizer)
GND_{SYNO}	9	S	ground (synthesizer output)
STOPSYN	10	I	test input : synthesizer section shut down
RSTRX	11	I	test input : reset receive logic
GND_{SUB}	12	S	ground (substrate)
STOPTX	13	I	test input : transmit section shut down
REFCLKQ	14	I	inverted reference clock input
REFCLK	15	I	reference clock input
$V_{CC(TXOUT)}$	16	S	supply voltage (transmitter output)
TXSD	17	O	serial data output
TXSDQ	18	O	inverted serial data output
GND_{TXOUT}	19	S	ground (transmitter output)
TXSCLKQ	20	O	inverted serial clock output
TXSCLK	21	O	serial clock output
SDTTL	22	I	TTL signal detect input
SDPECL	23	I	PECL signal detect input
RXSD	24	I	serial data input
RXSDQ	25	I	inverted serial data input
$V_{CC(RXCORE)}$	26	S	supply voltage (receiver core)
RXSCLK	27	I	serial clock input
RXSCLKQ	28	I	inverted serial clock input
GND_{RXCORE}	29	S	ground (receiver core)
BUSWIDTH	30	I	4/8 bus width select input
$\overline{LLEN}$	31	I	line loopback enable input (active LOW)
$\overline{DLEN}$	32	I	diagnostic loopback enable input (active LOW)
OOF	33	I	out of frame enable input
GND_{RXOUT}	34	S	ground (parallel output)
FP	35	O	frame pulse output
RXPD0	36	O	parallel data output 0
RXPD1	37	O	parallel data output 1
$V_{CC(RXOUT)}$	38	S	supply voltage (parallel output)
RXPD2	39	O	parallel data output 2
RXPD3	40	O	parallel data output 3

SYMBOL	PIN	TYPE[1]	DESCRIPTION
RXPD4	41	O	parallel data output 4
GND_{RXOUT}	42	S	ground (receiver output)
RXPD5	43	O	parallel data output 5
RXPD6	44	O	parallel data output 6
RXPD7	45	O	parallel data output 7
$V_{CC(RXOUT)}$	46	S	supply voltage (receiver output)
RXPCLK	47	O	receive parallel clock output
$\overline{MRST}$	48	I	master reset (active LOW)
MODE	49	I	serial data rate select STM1/STM4
STOPRX	50	I	receiver section shut down
GND_{RXD}	51	S	ground (receiver digital section)
$V_{CC(RXD)}$	52	S	supply voltage (receiver digital section)
TXPD0	53	I	parallel data input 0
TXPD1	54	I	parallel data input 1
TXPD2	55	I	parallel data input 2
TXPD3	56	I	parallel data input 3
TXPD4	57	I	parallel data input 4
TXPD5	58	I	parallel data input 5
TXPD6	59	I	parallel data input 6
TXPD7	60	I	parallel data input 7
TXPCLK	61	I	transmit parallel clock input
SYNCLKDIV	62	O	transmit byte/nibble clock output (synchronous)
LOCKDET	63	O	lock detect
19MHzO	64	O	19 MHz output reference clock

Note

1. Pin type abbreviations: O = Output, I = Input, S = power Supply.

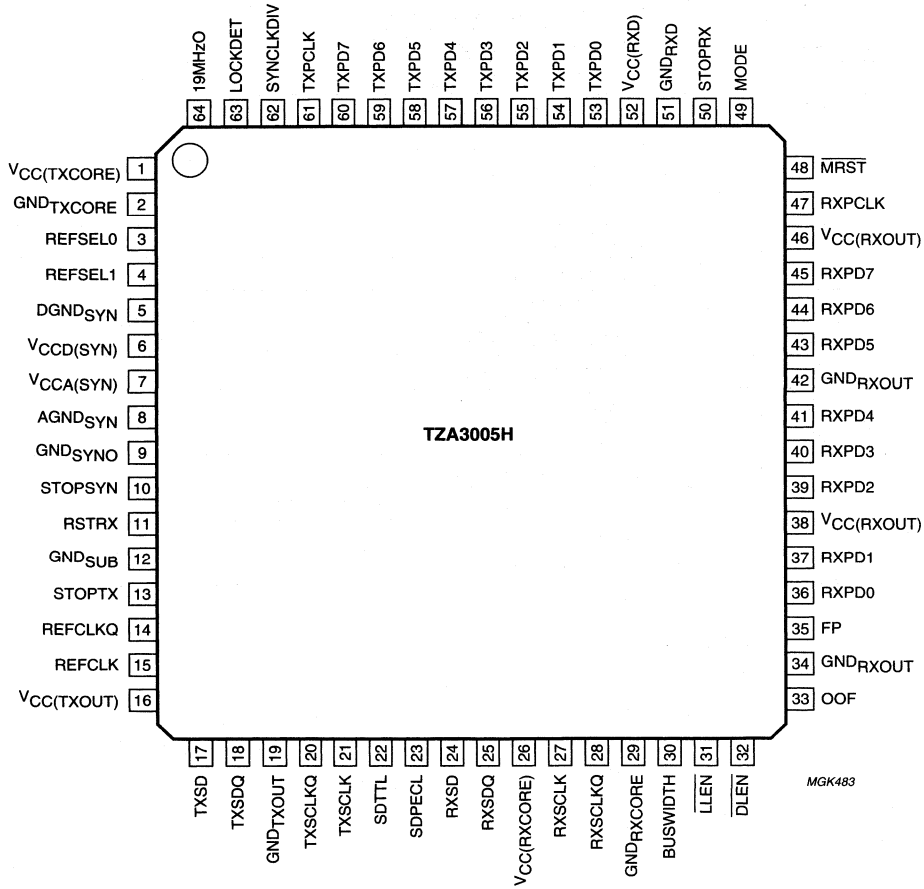


Fig.2 Pin configuration.

SDH/SONET STM4/OC12 transimpedance amplifier

TZA3023

FEATURES

- Low equivalent input noise, typically 3.5 pA/√Hz
- Wide dynamic range, typically 1 μA to 1.5 mA
- Differential transimpedance of 21 kΩ
- Wide bandwidth: 600 MHz
- Differential outputs
- On-chip AGC (Automatic Gain Control)
- No external components required
- Single supply voltage from 3.0 to 5.5 V
- Bias voltage for PIN diode.

APPLICATIONS

- Digital fibre optic receiver in short, medium and long haul optical telecommunications transmission systems or in high speed data networks
- Wideband RF gain block.

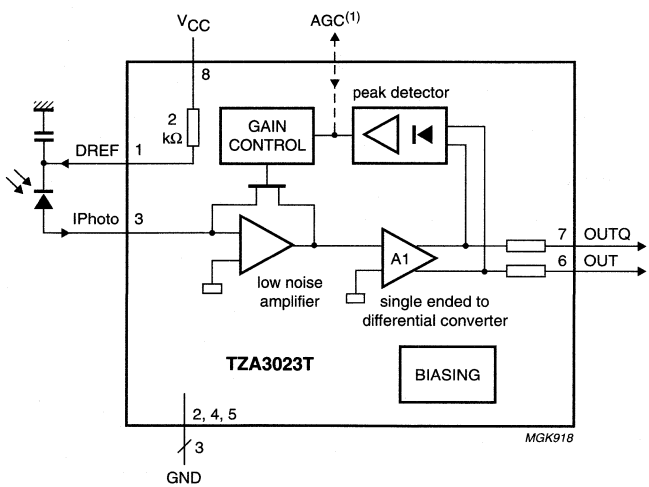
DESCRIPTION

The TZA3023 is a low-noise transimpedance amplifier with AGC designed to be used in STM4/OC12 fibre optic links. It amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and converts it to a differential output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3023T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TZA3023U	naked die	die in waffle pack carriers; die dimensions 0.960 × 1.210 mm	–

BLOCK DIAGRAM



(1) AGC analog I/O is only available on the TZA3023U (pad 13).

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
DREF	1	analog output	bias voltage for PIN diode (V_{CCA}); cathode should be connected to this pin
GND	2	ground	ground
IPhoto	3	analog input	current input; anode of PIN diode should be connected to this pin; DC bias level of 800 mV, one diode voltage above ground
GND	4	ground	ground
GND	5	ground	ground
OUT	6	CML output	data output; OUT goes HIGH when current flows into IPhoto (pin 3)
OUTQ	7	CML output	compliment of OUT (pin 6)
V_{CC}	8	supply	supply voltage

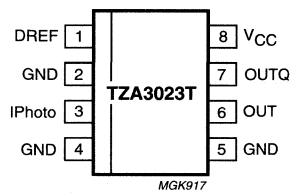


Fig.2 Pin configuration.

SDH/SONET STM4/OC12 postamplifiers TZA3024T; TZA3024U

FEATURES

- Pin compatible with the NE/SA5224 and NE/SA5225 but with extended power supply range and less external component count
- Wideband operation from 1.0 kHz to 620 MHz typical
- Applicable in 622 Mbits/s SDH/SONET receivers
- Single supply voltage from 3.0 to 5.5 V
- PECL (Positive Emitter Coupled Logic) compatible data outputs
- Programmable input signal level-detection which can be adjusted using a single external resistor
- On-chip DC offset compensation without external capacitor
- Fully differential for excellent PSRR.

APPLICATIONS

- Digital fibre optic receiver in short, medium and long haul optical telecommunications transmission systems or in high speed data networks
- Wideband RF gain block.

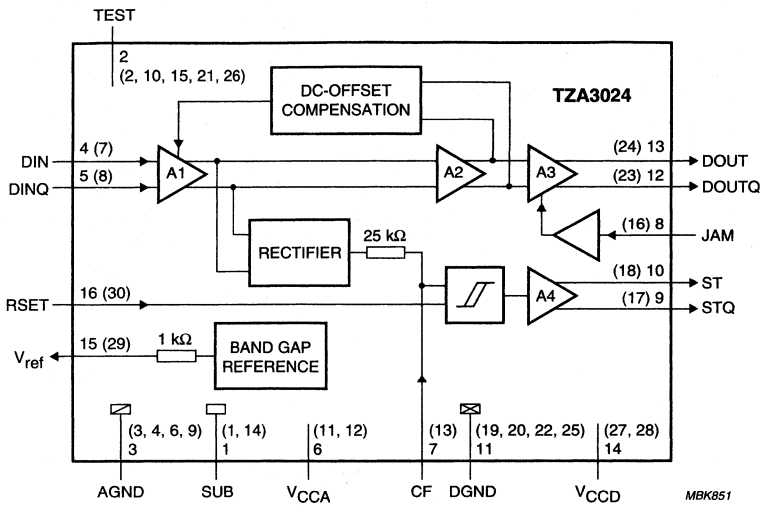
GENERAL DESCRIPTION

The TZA3024 is a high gain limiting amplifier that is designed to process signals from fibre optic preamplifiers such as the TZA3023. It is pin compatible with the NE/SA5224 and NE/SA5225 but with an extended power supply range, and needs less external components. Capable of operating at 622 Mbits/s, the chip has input signal level detection with a user-programmable threshold. The data and level-detection status outputs are differential outputs for optimum noise margin and ease of use.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3024T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TZA3024U	–	naked die in waffle pack carriers; die dimensions 1.58 × 1.58 mm	–

BLOCK DIAGRAM



The numbers in brackets refer to the pad numbers of the naked die version.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
SUB	1	substrate	substrate pin; must be at the same potential as AGND (pin 3)
TEST	2	test pin	for test purpose only; to be left open-circuit in the application
AGND	3	ground	analog ground; must be at the same potential as DGND (pin 11)
DIN	4	analog input	differential input; DC bias level is set internally at approximately 2.55 V; complimentary to DINQ (pin 5)
DINQ	5	analog input	differential input; DC bias level is set internally at approximately 2.55 V; complimentary to DIN (pin 4)
V_{CCA}	6	supply	analog supply voltage; must be at the same potential as V_{CCD} (pin 14)
CF	7	analog input	filter capacitor for input signal level detector; capacitor should be connected between this pin and V_{CCA} (pin 6)
JAM	8	PECL input	PECL-compatible input; controls the output buffers DOUT and DOUTQ (pins 13 and 12). When a LOW signal is applied, the outputs will follow the input signal. When a HIGH signal is applied, the DOUT and DOUTQ pins will latch into LOW and HIGH states, respectively. When left unconnected, this pin is actively pulled LOW (JAM off).
STQ	9	PECL output	PECL-compatible status output of the input signal level detector; when the input signal is below the user-programmed threshold level, this output is HIGH; complimentary to ST (pin 10)
ST	10	PECL output	PECL-compatible status output of the input signal level detector; when the input signal is below the user-programmed threshold level, this output is LOW; complimentary to STQ (pin 9)
DGND	11	ground	digital ground; must be at the same potential as AGND (pin 3)
DOUTQ	12	PECL output	PECL-compatible differential output; when JAM is HIGH, this pin will be forced into a HIGH condition; complimentary to DOUT (pin 13)
DOUT	13	PECL output	PECL-compatible differential output; when JAM is HIGH, this pin will be forced into a LOW condition; complimentary to DOUTQ (pin 12)
V_{CCD}	14	supply	digital supply voltage; must be at the same potential as V_{CCA} (pin 6)
V_{ref}	15	analog output	band gap reference voltage; typical value is 1.2 V; internal series resistor of 1 kΩ
RSET	16	analog input	input signal level detector programming; nominal DC voltage is V_{CCA} − 1.5 V; threshold level is set by connecting an external resistor between RSET and V_{CCA} or by forcing a current into RSET; default value for this resistor is 180 kΩ which corresponds with approximately 4 $mV_{(p-p)}$ differential input signal

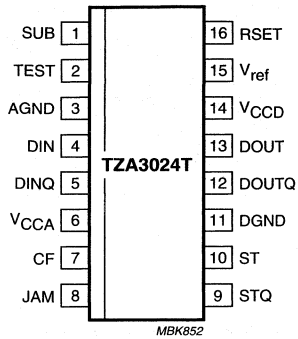


Fig.2 Pin configuration.

Gigabit Ethernet/Fibre Channel optical receiver TZA3040

FEATURES

- Equivalent input noise, typically 6.6 pA/√Hz
- Wide dynamic range, typically 2 μA to 1.5 mA
- Differential transimpedance of 1.1 MΩ
- On-chip Automatic Gain Control (AGC)
- Positive Emitter Coupled Logic (PECL) or Current-Mode Logic (CML) compatible data outputs
- Loss Of Signal (LOS) detection
- LOS threshold level can be adjusted using a single external resistor
- On-chip DC offset compensation
- Single supply voltage from 3.0 to 5.5 V
- Bias voltage for PIN diode.

APPLICATIONS

- Digital fibre optic receiver in short, medium and long haul optical telecommunications transmission systems or in high speed data networks
- Wideband RF gain block.

GENERAL DESCRIPTION

The TZA3040 optical receiver is a high speed transimpedance amplifier with AGC plus a limiting amplifier designed to be used in Gigabit Ethernet/Fibre Channel applications. The TZA3040 amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and converts it to a differential output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3040HL	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1
TZA3040U	–	naked die in waffle pack carriers; die dimensions 1.58 × 1.58 mm	–

BLOCK DIAGRAM

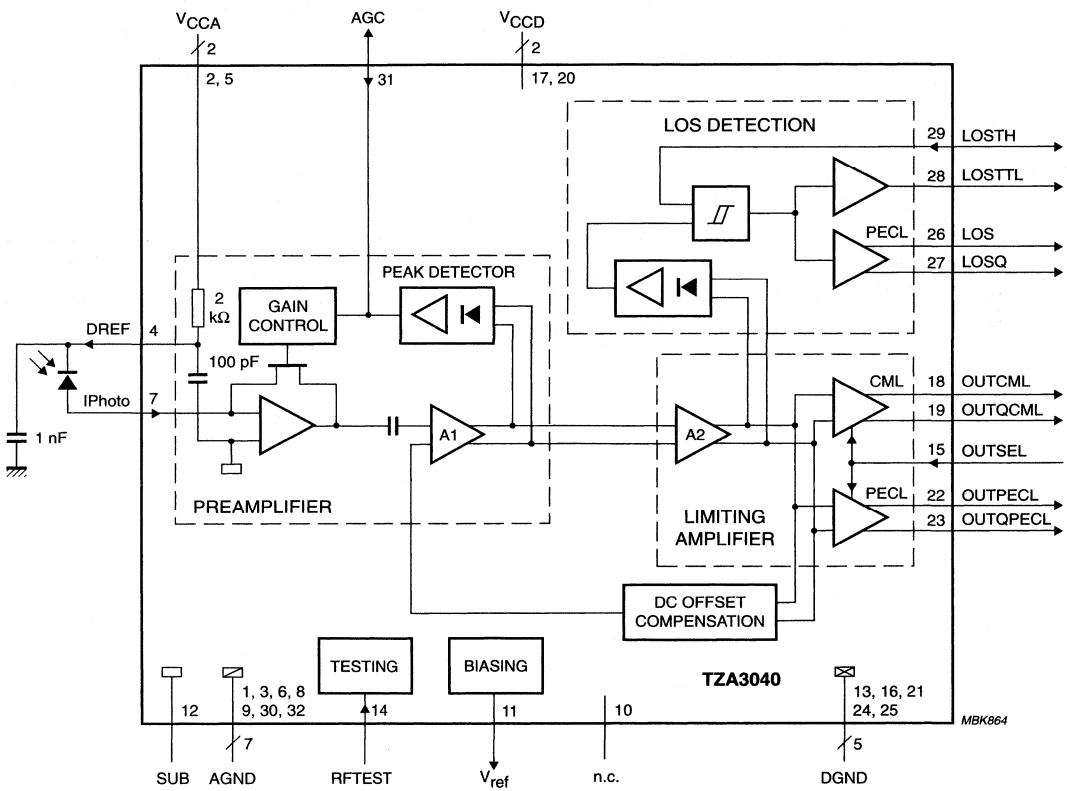


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
AGND	1	ground	analog ground
V_{CCA}	2	supply	analog supply voltage
AGND	3	ground	analog ground
DREF	4	analog output	bias voltage for PIN diode (V_{CCA}); cathode should be connected to this pin
V_{CCA}	5	supply	analog supply voltage
AGND	6	ground	analog ground
IPhoto	7	analog input	current input; connect the anode of PIN diode to this pin; DC bias level is 822 mV, one diode voltage above ground
AGND	8	ground	analog ground
AGND	9	ground	analog ground
n.c.	10	–	not connected
V_{ref}	11	analog output	band gap reference voltage; nominal value approximately 1.2 V
SUB	12	substrate	substrate pin; to be connected to AGND
DGND	13	ground	digital ground
RFTEST	14	analog input	test pin; not connected; not used in application
OUTSEL	15	CMOS input	output select pin; when OUTSEL is HIGH, CML data outputs are active and PECL data outputs are disabled; OUTSEL is pulled LOW if left unconnected, PECL data outputs will then be active and CML data outputs disabled
DGND	16	ground	digital ground
V_{CCD}	17	supply	digital supply voltage
OUTCML	18	CML output	CML data output; OUTCML goes HIGH when current flows into IPhoto (pin 7)
OUTQCML	19	CML output	CML compliment of OUTCML (pin 18)
V_{CCD}	20	supply	digital supply voltage
DGND	21	ground	digital ground
OUTPECL	22	PECL output	PECL data output; OUTPECL goes HIGH when current flows into IPhoto (pin 7)
OUTQPECL	23	PECL output	PECL compliment of OUTPECL (pin 22)
DGND	24	ground	digital ground
DGND	25	ground	digital ground
LOS	26	PECL output	PECL compatible LOS detection pin; LOS output is HIGH when the input signal is below the user programmable threshold level
LOSQ	27	PECL output	PECL compliment of LOS (pin 26)
LOSTTL	28	TTL output	TTL compatible LOS detection pin; the LOSTTL output is HIGH when the input signal is below the user programmable threshold level
LOSTH	29	analog I/O	pin for setting input threshold level; nominal DC voltage is $V_{CCA} - 1.5$ V; threshold level set by connecting an external resistor between LOSTH and V_{CCA} or by forcing a current into LOSTH; default value for this resistor is 39 kΩ
AGND	30	ground	analog ground
AGC	31	analog I/O	AGC monitor voltage; the internal AGC circuit can be disabled by applying an external voltage to this pin
AGND	32	ground	analog ground

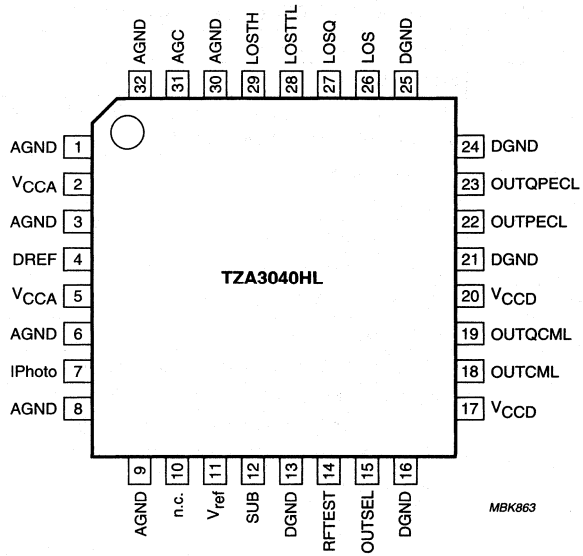


Fig.2 Pin configuration.

Gigabit Ethernet/Fibre Channel laser drivers

TZA3041AHL; TZA3041BHL; TZA3041U

FEATURES

- 1.2 Gbits/s data input, both Current-Mode Logic (CML) and Positive Emitter Coupled Logic (PECL) compatible; maximum 800 mV (peak-to-peak value)
- Adaptive laser output control, stabilizing optical ONE and ZERO levels
- Optional external (non-adaptive) control of laser modulation and biasing currents
- Automatic Laser Shut-down (ALS)
- Few external components required
- Rise and fall times typically 120 ps
- Jitter <50 mUI (peak-to-peak value)
- RF output current sinking capability of 60 mA
- Bias current sinking capability of 90 mA
- Power dissipation typically 475 mW
- Low cost LQFP32 plastic package
- Single 5 V power supply.

TZA3041AHL

- Laser alarm output for signalling extremely low and high bias current conditions.

TZA3041BHL

- Loop mode for testing 1.2 Gbits/s optical interfaces; CML and PECL compatible.

TZA3041U

- Naked die version with combined bias alarm and loop mode functionality.

APPLICATIONS

- Gigabit Ethernet/Fibre Channel optical transmission systems
- Gigabit Ethernet/Fibre Channel optical laser modules.

DESCRIPTION

The TZA3041AHL, TZA3041BHL and TZA3041U are fully integrated laser drivers for Gigabit Ethernet/Fibre Channel (1.2 Gbits/s) systems, incorporating the RF path between the data multiplexer and the laser diode. Since the bias and modulation control circuits are integrated on the IC, the external component count is low (only decoupling capacitors and adjustment resistors are required).

The TZA3041AHL features an alarm function for signalling extreme bias current conditions. The alarm low and high threshold levels can be adjusted to suit the application using only a resistor. An additional RF data input is provided with the TZA3041BHL to facilitate remote (loop mode) system testing.

The TZA3041U is a naked die version for use in compact laser module designs. The die contains 40 pads and features the combined functionality of the TZA3041AHL and TZA3041BHL.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3041AHL	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1
TZA3041BHL			
TZA3041U	–	naked die; 2000 × 2000 × 380 μm	–

BLOCK DIAGRAMS

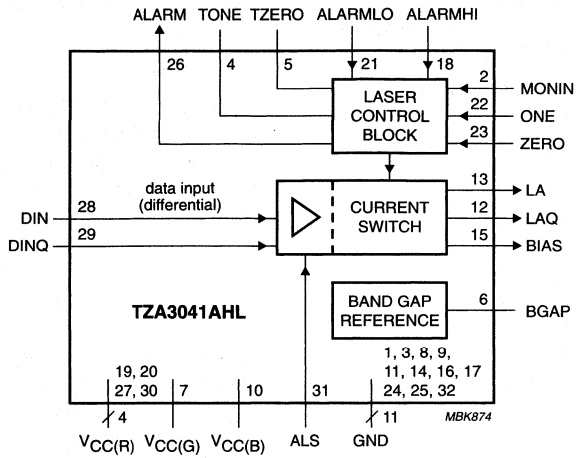


Fig.1 Block diagram: TZA3041AHL.

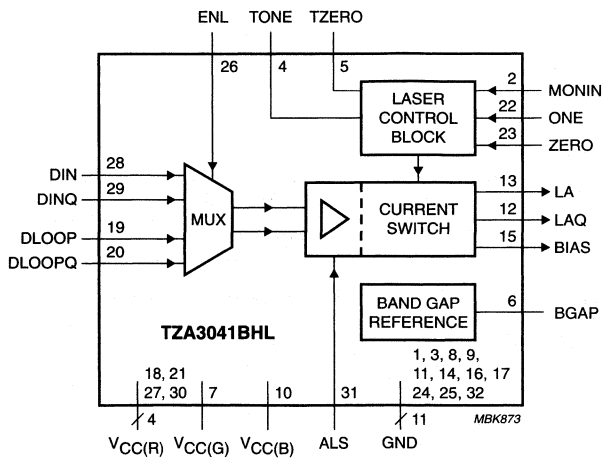


Fig.2 Block diagram: TZA3041BHL.

PINNING

TZA3041AHL

SYMBOL	PIN	DESCRIPTION
GND	1	ground
MONIN	2	monitor photodiode current input
GND	3	ground
TONE	4	connection for external capacitor used to set optical ONE control loop time constant (optional)
TZERO	5	connection for external capacitor used to set optical ZERO control loop time constant (optional)
BGAP	6	connection for external band gap decoupling capacitor
$V_{CC(G)}$	7	supply voltage; note 1
GND	8	ground
GND	9	ground
$V_{CC(B)}$	10	supply voltage; note 1
GND	11	ground
LAQ	12	inverted laser modulation output
LA	13	laser modulation output
GND	14	ground
BIAS	15	laser bias current output
GND	16	ground
GND	17	ground
ALARMHI	18	maximum bias current alarm reference level input
$V_{CC(R)}$	19	supply voltage; note 1
$V_{CC(R)}$	20	supply voltage; note 1
ALARMLO	21	minimum bias current alarm reference level input
ONE	22	optical ONE reference level input
ZERO	23	optical ZERO reference level input
GND	24	ground
GND	25	ground
ALARM	26	alarm output
$V_{CC(R)}$	27	supply voltage; note 1
DIN	28	data input
DINQ	29	inverted data input
$V_{CC(R)}$	30	supply voltage; note 1
ALS	31	automatic laser shut-down input
GND	32	ground

TZA3041BHL

SYMBOL	PIN	DESCRIPTION
GND	1	ground
MONIN	2	monitor photodiode current input
GND	3	ground
TONE	4	connection for external capacitor used to set optical ONE control loop time constant (optional)
TZERO	5	connection for external capacitor used to set optical ZERO control loop time constant (optional)
BGAP	6	connection for external band gap decoupling capacitor
$V_{CC(G)}$	7	supply voltage; note 1
GND	8	ground
GND	9	ground
$V_{CC(B)}$	10	supply voltage; note 1
GND	11	ground
LAQ	12	inverted laser modulation output
LA	13	laser modulation output
GND	14	ground
BIAS	15	laser bias current output
GND	16	ground
GND	17	ground
$V_{CC(R)}$	18	supply voltage; note 1
DLOOP	19	loop mode data input
DLOOPQ	20	loop mode inverted data input
$V_{CC(R)}$	21	supply voltage; note 1
ONE	22	optical ONE reference level input
ZERO	23	optical ZERO reference level input
GND	24	ground
GND	25	ground
ENL	26	loop mode enable input
$V_{CC(R)}$	27	supply voltage; note 1
DIN	28	data input
DINQ	29	inverted data input
$V_{CC(R)}$	30	supply voltage; note 1
ALS	31	automatic laser shutdown input
GND	32	ground

Note to Tables TZA3041AHL and TZA3041BHL

1. See Section "Power supply connections".

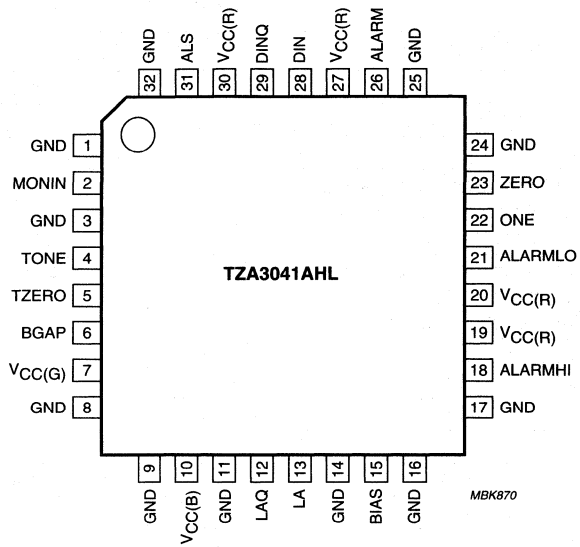


Fig.3 Pin configuration: TZA3041AHL.

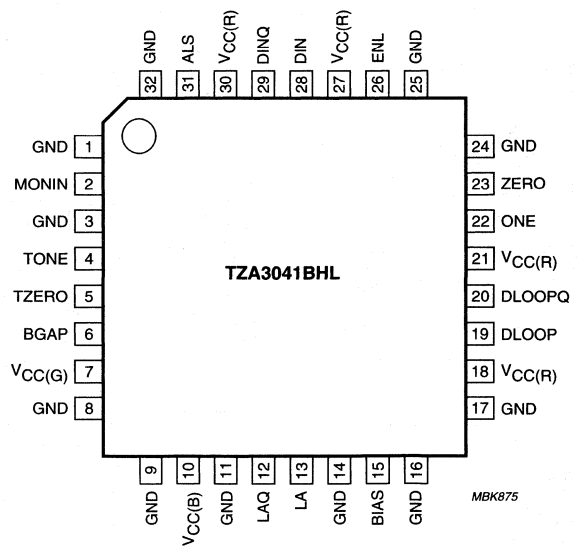


Fig.4 Pin configuration: TZA3041BHL.

Gigabit Ethernet/Fibre Channel transimpedance amplifier TZA3043

FEATURES

- Wide dynamic range, typically 2.5 μA to 1.5 mA
- Differential transimpedance of 14 kΩ
- Wide bandwidth of 950 MHz
- Differential outputs
- On-chip AGC (Automatic Gain Control)
- No external components required
- Single supply voltage from 3.0 to 5.5 V
- Bias voltage for PIN diode
- Pin compatible with TZA3023 and SA5223.

APPLICATIONS

- Digital fibre optic receiver in medium and long haul optical telecommunications transmission systems or in high speed data networks
- Wideband RF gain block.

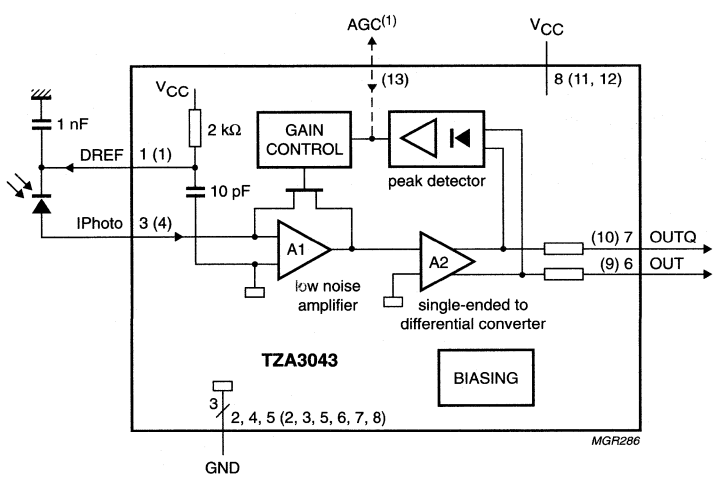
DESCRIPTION

The TZA3043 is a high speed transimpedance amplifier with AGC designed to be used in Gigabit Ethernet/Fibre Channel optical links. It amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and converts it to a differential output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3043T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TZA3043U	naked die	die in waffle pack carriers; die dimensions 0.960 × 1.210 mm	–

BLOCK DIAGRAM



(1) AGC analog I/O is only available on the TZA3043U (pad 13).
The numbers in brackets refer to the pad numbers of the naked die version.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
DREF	1	analog output	bias voltage for PIN diode (V_{CC}); cathode should be connected to this pin
GND	2	ground	ground
IPhoto	3	analog input	current input; anode of PIN diode should be connected to this pin; DC bias level of 822 mV is one diode voltage above ground
GND	4	ground	ground
GND	5	ground	ground
OUT	6	data output	data output; OUT goes HIGH when current flows into IPhoto (pin 3)
OUTQ	7	data output	compliment of OUT (pin 6)
V_{CC}	8	supply	supply voltage

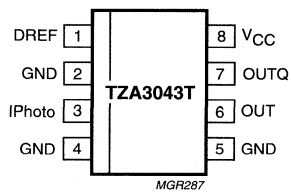


Fig.2 Pin configuration.

1.25 Gbits/s Gigabit Ethernet postamplifiers TZA3044T; TZA3044U

FEATURES

- Pin compatible with the NE/SA5224 and NE/SA5225 but with extended power supply range and less external component count
- Wideband operation from 1.0 kHz to 1.25 GHz typical
- Applicable in 1.25 Gbits/s Gigabit Ethernet receivers
- Single supply voltage from 3.0 to 5.5 V
- PECL (Positive Emitter Coupled Logic) compatible data outputs
- Programmable input signal level-detection to be adjusted using a single external resistor
- On-chip DC offset compensation without external capacitor
- Fully differential for excellent PSRR.

APPLICATIONS

- Digital fibre optic receiver for Gigabit Ethernet applications
- Wideband RF gain block.

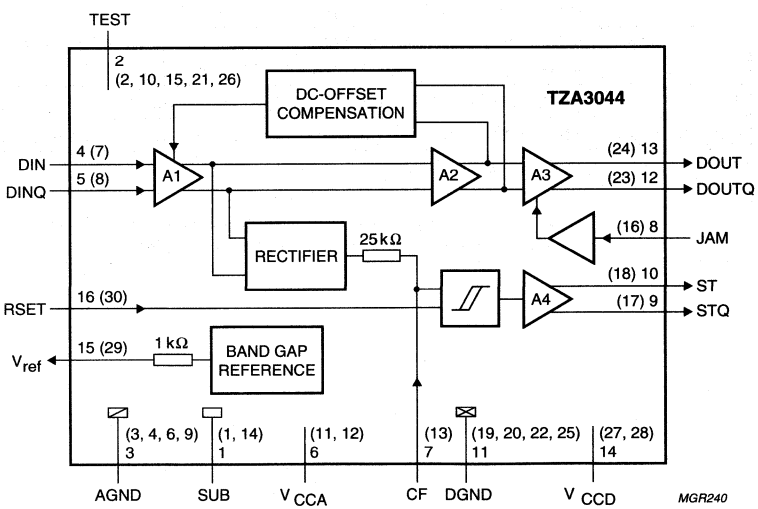
GENERAL DESCRIPTION

The TZA3044 is a high gain limiting amplifier that is designed to process signals from fibre optic preamplifiers like the TZA3043. It is pin compatible with the NE/SA5224 and NE/SA5225 but with extended power supply range, and needs less external components. Capable of operating at 1.25 Gbits/s, the chip has input signal level detection with a user-programmable threshold. The data and level-detection status outputs are differential outputs for optimum noise margin and ease of use.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3044T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TZA3044U	naked die	die in waffle pack carriers; die dimensions 1.58 × 1.58 mm	–

BLOCK DIAGRAM



The numbers in brackets refer to the pad numbers of the naked die version.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
SUB	1	substrate	substrate pin; must be at the same potential as AGND (pin 3)
TEST	2	test pin	for test purpose only; to be left open in the application
AGND	3	ground	analog ground; must be at the same potential as DGND (pin 11)
DIN	4	analog input	differential input; DC bias level is set internally at approximately 2.55 V; complimentary to DINQ (pin 5)
DINQ	5	analog input	differential input; DC bias level is set internally at approximately 2.55 V; complimentary to DIN (pin 4)
V_{CCA}	6	supply	analog supply voltage; must be at the same potential as V_{CCD} (pin 14)
CF	7	analog input	filter capacitor for input signal level detector; capacitor should be connected between this pin and V_{CCA} (pin 6)
JAM	8	PECL input	PECL-compatible input; controls the output buffers DOUT and DOUTQ (pins 13 and 12). When a LOW signal is applied, the outputs will follow the input signal. When a HIGH signal is applied, the DOUT and DOUTQ pins will latch into LOW and HIGH states, respectively. When left unconnected, this pin is actively pulled LOW (JAM OFF).
STQ	9	PECL output	PECL-compatible status output of the input signal level detector; when the input signal is below the user-programmed threshold level, this output is HIGH; complimentary to ST (pin 10)
ST	10	PECL output	PECL-compatible status output of the input signal level detector; when the input signal is below the user-programmed threshold level, this output is LOW; complimentary to STQ (pin 9)
DGND	11	ground	digital ground; must be at the same potential as AGND (pin 3)
DOUTQ	12	PECL output	PECL-compatible differential output; when JAM is HIGH, this pin will be forced into a HIGH condition; complimentary to DOUT (pin 13)
DOUT	13	PECL output	PECL-compatible differential output; when JAM is HIGH, this pin will be forced into a LOW condition; complimentary to DOUTQ (pin 12)
V_{CCD}	14	supply	digital supply voltage; must be at the same potential as V_{CCA} (pin 6)
V_{ref}	15	analog output	band gap reference voltage; typical value is 1.2 V; internal series resistor of 1 kΩ
RSET	16	analog input	input signal level detector programming; nominal DC voltage is $V_{CCA} - 1.5$ V; threshold level is set by connecting an external resistor between RSET and V_{CCA} or by forcing a current into RSET; default value for this resistor is 180 kΩ which corresponds with approximately 4 mV (p-p) differential input signal

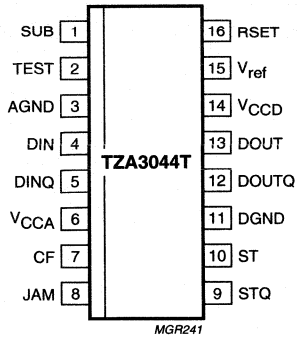


Fig.2 Pin configuration.

Section 7
Futurebus+/BTL Products

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Futurebus+ / BTL: A high performance standard for advanced computing and communication systems

INTRODUCTION

Futurebus+ specifications were developed by several participants from commercial and non-commercial sectors worldwide. These participants represent system-level companies, component manufacturers, equipment manufacturers and other engineering professionals. Philips Semiconductors has been actively involved in the development of the specifications. We now offer the most essential parts of Futurebus+ specification — the Arbitration Controller and BTL Transceivers.

Futurebus+ is an IEEE specification (IEEE896.1) that also includes the Backplane Transceiver Logic (BTL) specification (IEEE 1194). It is especially designed for high performance backplane-based computing that permits architectural consistency across a broad range of systems. It provides a 64-bit architecture and datapath extensions up to 256 bits.

Some of the major benefits of the protocol are due to its efficient support of fault tolerance, live insertion (a.k.a., hot insertion or hot swapping), high speed – low power dissipation, and room for extension. These benefits mainly stem from the BTL level support for the backplane.

BTL logic requires implementation of Schottky Diode, Bipolar output structures and CMOS internal logic. All these requirements necessitate the use of BiCMOS technology. Philips has implemented these ICs in the industry's most advanced BiCMOS process technology (QUBiC). Philips implements several logic ICs and ASSPs (Application Specific Standard Products) in this technology. Since the late 1980s, Philips has produced several million ICs using this process technology. Applications of QUBiC are ABT driver family, Custom ICs for automotive manufacturers, Mass Storage Electronics, and RF/Wireless Communication chip-sets, to name but a few.

Major Applications:

Figure 1 shows a typical computing or communications environment that utilizes the key features of Futurebus+ and BTL. Figure 2 shows a typical configuration of Philips Futurebus+ chip-set.

Figure 1 depicts an environment that needs live insertion and high-reliability all the time, such as Massively Parallel Computers, Fault Tolerant Computers, or Network Controller Systems, etc. Any such environment that requires a high speed backplane bus can use the Futurebus+/BTL transceivers. The main requirements of such backplane bus are Low Power Dissipation at high speed and the ability to swap boards while the system remains powered-up (i.e., Live Insertion).

Several of our major customers make use of the 7-bit, 8-bit or 9-bit BTL transceivers for conversion of BTL signals from the bus to TTL signals on board. These transceivers are now fully qualified and characterized for high volume production.

Table 1. Philips Futurebus+/BTL Product Offering

Part Number	Description	Special Feature
FB2031BB	Futurebus+ 9-bit transceiver	0 – 70°C
FB2031IBB	Futurebus+ 9-bit transceiver	–40 – +85°C
FB2041BB	Futurebus+ 7-bit transceiver	0 – 70°C
FB2041IBB	Futurebus+ 7-bit transceiver	–40 – +85°C
FB2033BB	Futurebus+ 8-bit transceiver	0 – 70°C
FB2040ABB	Futurebus+ 8-bit transceiver	0 – 70°C
FB2012AA	Futurebus+ Centralized Arbitration Controller	0 – 70°C

NOTES:
1. BB = 52-Pin Plastic Quad Flat Pack;
   A = 68-Pin Plastic Leaded Chip Carrier

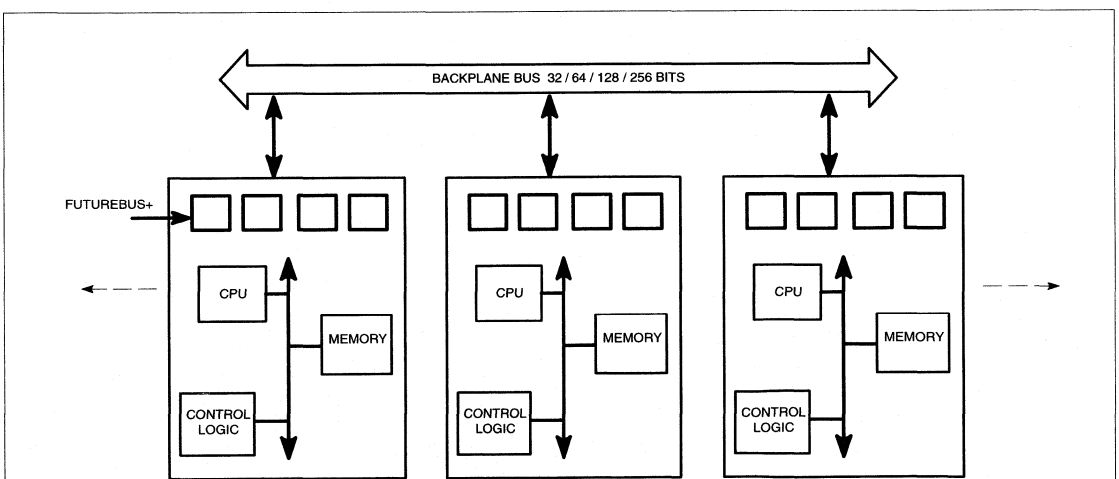


Figure 1. A Typical Application of Futurebus+/BTL Transceivers and Arbitration Controller

Futurebus+ / BTL: A high performance standard for advanced computing and communication systems

INTRODUCTION

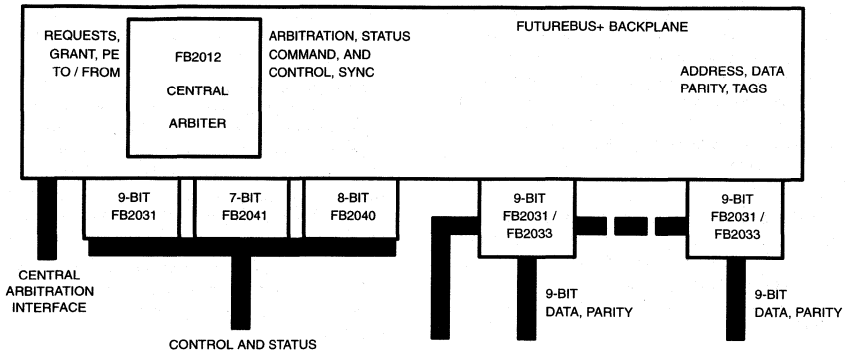


Figure 2. Futurebus+ Implementation with Philips Semiconductors Futurebus+ Chip-set

Key Features of Philips Futurebus+/BTL Chip-set:

The key features of Philips Futurebus+/BTL chip-set are as follows:

- Compatible with IEEE specifications of Futurebus+ (IEEE896) and BTL (IEEE1194)
- Most of the parts fully characterized over Commercial as well as Industrial temperature range
- Manufactured in high volume state-of-the-art 0.9µm BiCMOS technology (QUBiC)
- Arbitration Controllers implemented using centralized bus arbitration scheme providing higher performance than distributed arbitration
- 7-bit, 8-bit and 9-bit transceivers with:
  - An excellent EMI shielding due to isolated GND planes between BTL and TTL sides
  - Low propagation delays and well-controlled edge rates
- Product availability: Fully qualified and characterized products available for high volume production
- All four transceivers are Alternate Sourced by Texas Instruments

For more detailed information and samples, please contact the nearest Philips Semiconductors Sales Office.

9-bit latched/registered/pass-thru Futurebus+ transceiver FB2031

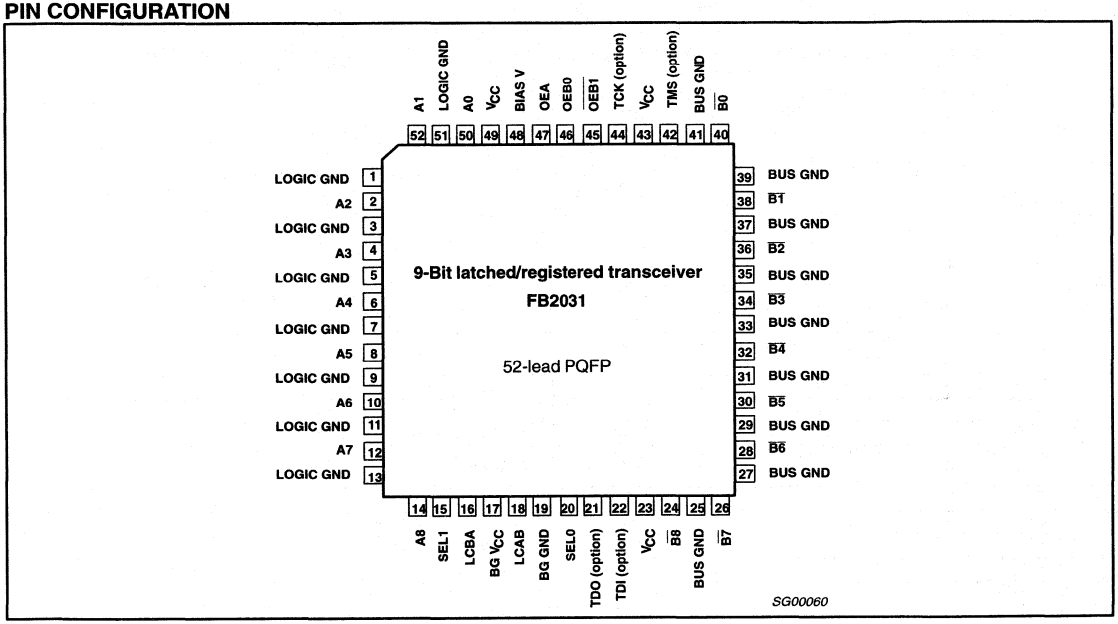
FEATURES

- Latched, registered or straight through in either A to B or B to A path
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Each BTL driver has a dedicated Bus GND for a signal return
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion

ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10%; T_{amb} = −40°C to +85°C	DRAWING NUMBER
52-pin Plastic Quad Flat Pack (QFP)	FB2031BB	CD3206BB	SOT379-1

PIN CONFIGURATION



9-bit latched/registered/pass-thru Futurebus+ transceiver FB2031

DESCRIPTION

The FB2031 is a 9-bit latched/registered transceiver featuring a latched, registered or pass-thru mode in either the A-to-B or B-to-A direction. The FB2031 is intended to provide the electrical interface to a high performance wired-OR bus.

The TTL-level side (A port) has a common I/O. The common I/O, open collector B port operates at BTL signal levels. The logic element for data flow in each direction is controlled by two mode select inputs (SEL0 and SEL1). A "00" configures latches in both directions. A "10" configures thru mode in both directions. A "01" configures register mode in both directions. A "11" configures register mode in the A-to-B direction and latch mode in the B-to-A direction.

When configured in the buffer mode, the inverse of the input data appears at the output port. In the register mode, data is stored on the rising edge of the appropriate clock input (LCAB or LCBA). In the latch mode, clock pins serve as transparent-Low latch enables. Regardless of the mode, data is inverted from input to output.

The 3-State A port is enabled by asserting a High level on OEA. The B port has two output enables, OEB0 and $\overline{OEB1}$. Only when OEB0 is High and $\overline{OEB1}$ is Low is the output enabled.

When either OEB0 is Low or $\overline{OEB1}$ is High, the B port is inactive and is pulled to the level of the pullup voltage. New data can be entered in the register and latched modes or can be retained while the associated outputs are in 3-State (A port) or inactive (B port).

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to "Backplane Transceiver Logic" (see the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1V p-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

Output clamps are provided on the BTL outputs to further reduce switching noise. The "V_{OH}" clamp reduces inductive ringing effects during a Low-to-High transition. The "V_{OH}" clamp is always active. The other clamp, the "trapped reflection" clamp, clamps out ringing below the BTL 0.5V V_{OL} level. This clamp remains active for approximately 100ns after a High-to-Low transition.

To support live insertion, OEB0 is held Low during power on/off cycles to insure glitch-free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 5V level while V_{CC} is Low. The BIAS V pin is a low current input which will reverse-bias the BTL driver series Schottky diode, and also bias the B port output pins to a voltage between 1.62V and 2.1V. This bias function is in accordance with IEEE BTL Standard 1194.1. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated inside the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

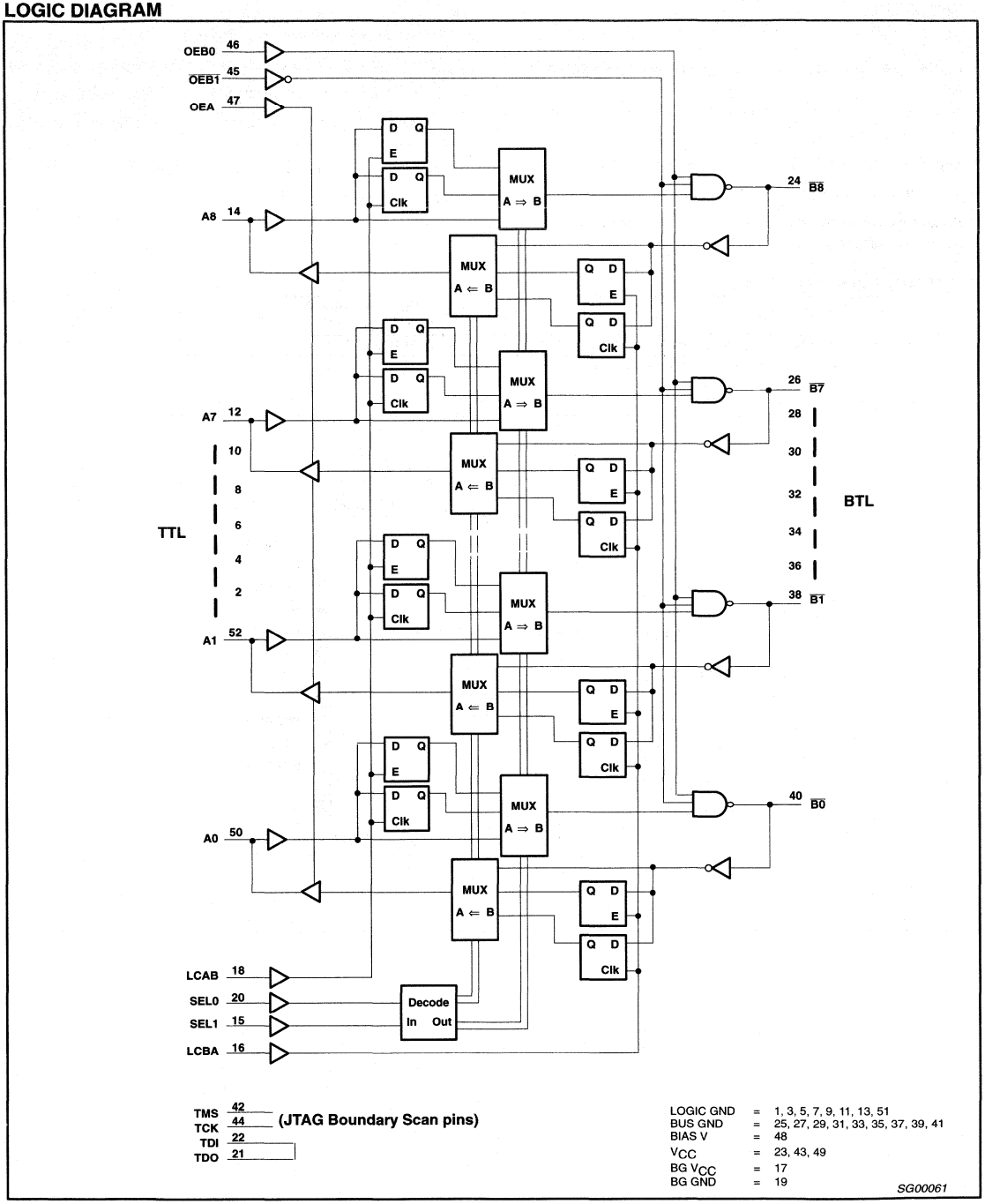
Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be infrequent and impossible to troubleshoot.

As with any high power device, thermal considerations are critical. It is recommended that airflow (300lfpm) and/or thermal mounting be used to ensure proper junction temperature.

PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
A0 – A8	50, 52, 2, 4, 6, 8, 10, 12, 14	I/O	BiCMOS data inputs/3-State outputs (TTL)
$\overline{B0}$ – $\overline{B8}$	40, 38, 36, 34, 32, 30, 28, 26, 24	I/O	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	46	Input	Enables the B outputs when High
$\overline{OEB1}$	45	Input	Enables the B outputs when Low
OEA	47	Input	Enables the A outputs when High
BUS GND	25, 27, 29, 31, 33, 35, 37, 39, 41	GND	Bus ground (0V)
LOGIC GND	51, 1, 3, 5, 7, 9, 11, 13	GND	Logic ground (0V)
V_{CC}	23, 43, 49	Power	Positive supply voltage
BIAS V	48	Power	Live insertion pre-bias pin
BG V_{CC}	17	Power	Band Gap threshold voltage reference
BG GND	19	GND	Band Gap threshold voltage reference ground
SEL0	20	Input	Mode select
SEL1	15	Input	Mode select
LCAB	18	Input	A to B clock/latch enable (transparent latch when Low)
LCBA	16	Input	B to A clock/latch enable (transparent latch when Low)
TMS	42	Input	Test Mode Select (optional, if not implemented then no connect)
TCK	44	Input	Test Clock (optional, if not implemented then no connect)
TDI	22	Input	Test Data In (optional, if not implemented then no connect)
TDO	21	Output	Test Data Out (optional, if not implemented then shorted to TDI)

LOGIC DIAGRAM



8-bit latched/registered/pass-thru Futurebus+ universal interface transceiver

FB2033

FEATURES

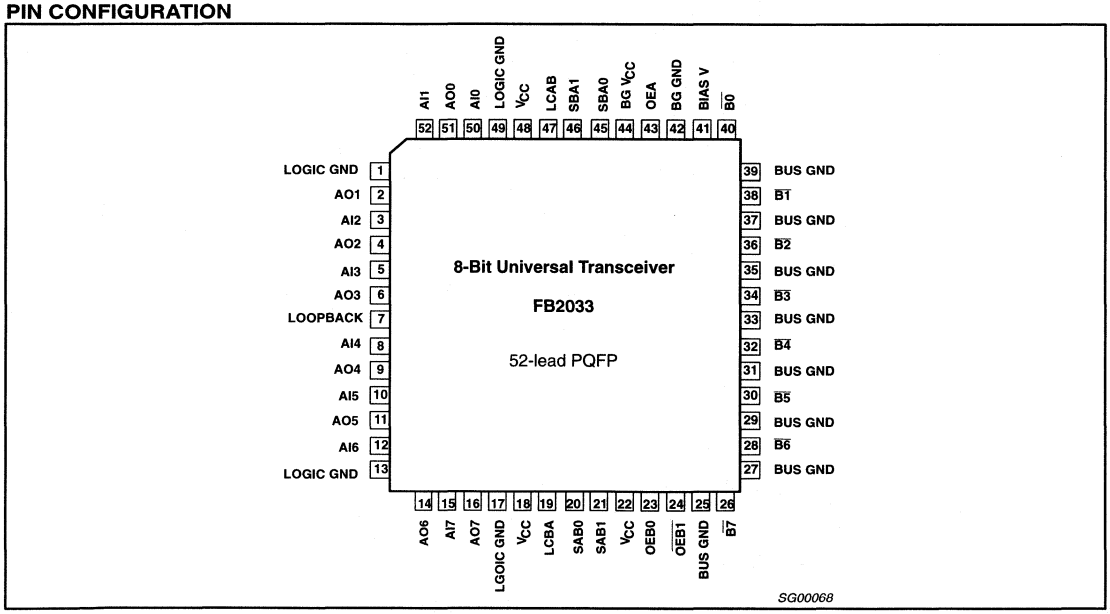
- 8-bit transceivers
- Latched, registered or straight through in either A to B or B to A path
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω
- High drive 100mA BTL Open Collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Each BTL driver has a dedicated Bus GND for a signal return
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C	DRAWING NUMBER
52-pin Plastic Quad Flat Pack (QFP)	FB2033BB	SOT379-1

NOTE: Thermal mounting or forced air is recommended

PIN CONFIGURATION



8-bit latched/registered/pass-thru Futurebus+ universal interface transceiver

FB2033

DESCRIPTION

The FB2033 is an 8-bit transceiver featuring a split input (AI) and output (AO) bus on the TTL-level side.

The common I/O, open collector B port operates at BTL signal levels. The logic element for data flow in each direction is controlled by two pairs of mode select inputs (SBA0 and SBA1 for B-to-A, SAB0 and SAB1 for A-to-B). It can be configured as a buffer, a register, or a D-type latch.

When configured in the buffer mode, the inverse of the input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (LCAB or LCBA). In the latch mode, clock pins serve as transparent-High latch enables. Regardless of the mode, data is inverted from input to output.

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the Loopback input. When the Loopback input is High the output of the selected A-to-B logic element (not inverted) becomes the B-to-A input.

The 3-State AO port is enabled by asserting a High level on OEA. The B port has two output enables, OEB0 and $\overline{OEB1}$. Only when OEB0 is High and $\overline{OEB1}$ is Low is the output enabled. When either OEB0 is Low or $\overline{OEB1}$ is High, the B-port is inactive and is pulled to the level of the pull-up voltage. New data can be entered in the flip-flop and latched modes or can be retained while the associated outputs are in 3-State (AO port) or inactive (B port).

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port ensure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to "Backplane Transceiver Logic" (see the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1V p-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

Output clamps are provided on the BTL outputs to further reduce switching noise. The "V_{OH}" clamp reduces inductive ringing effects during a Low-to-High transition. The "V_{OH}" clamp is always active. The other clamp, the "trapped reflection" clamp, clamps out ringing below the BTL 0.5V V_{OL} level. This clamp remains active for approximately 100ns after a High-to-Low transition.

To support live insertion, OEB0 is held Low during power on/off cycles to ensure glitch- free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 5V level while V_{CC} is Low. The BIAS V pin is a low current input which will reverse-bias the BTL driver series Schottky diode, and also bias the B port output pins to a voltage between 1.62V and 2.1V. This bias function is in accordance with IEEE BTL Standard 1194.1. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated inside the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

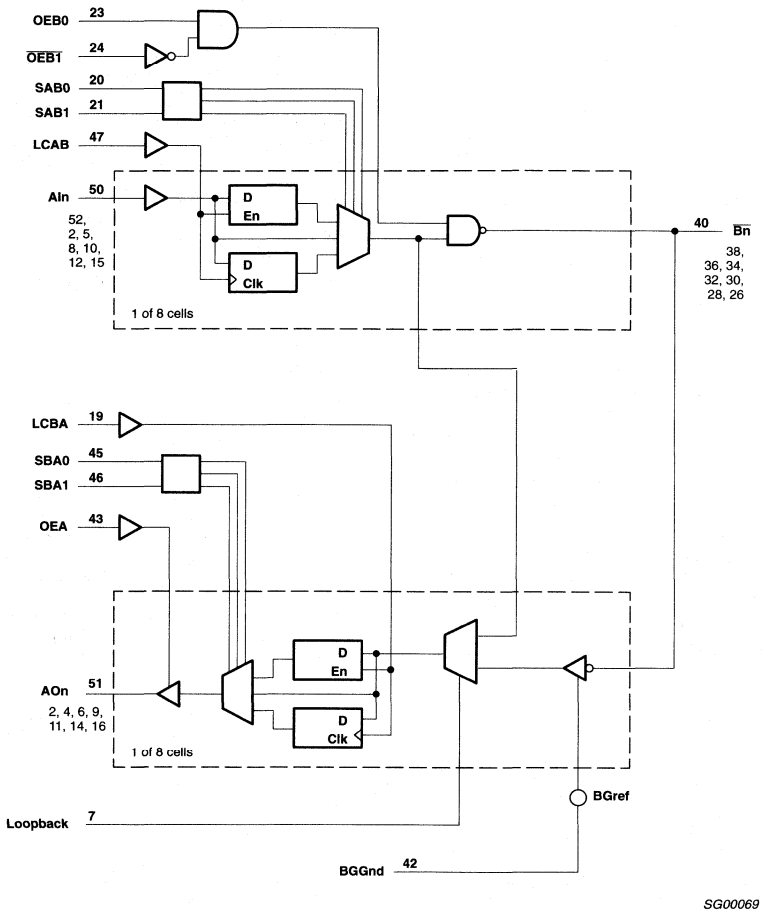
Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be very infrequent and impossible to trouble- shoot.

As with any high power device thermal considerations are critical. It is recommended that airflow (300lfpm) and/or thermal mounting be used to ensure proper junction temperature.

PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
AI0 – AI7	50, 52, 3, 5, 8, 10, 12, 15	Input	Data inputs (TTL)
AO0 – AO7	51, 2, 4, 6, 9, 11, 14, 16	Output	3-State outputs (TTL)
$\overline{B0}$ – $\overline{B7}$	40, 38, 36, 34, 32, 30, 28, 26	I/O	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	23	Input	Enables the B outputs when High
$\overline{OEB1}$	24	Input	Enables the B outputs when Low
OEA	43	Input	Enables the AO outputs when High
BUS GND	39, 37, 35, 33, 31, 29, 27, 25	GND	Bus ground (0V)
LOGIC GND	1, 13, 17, 49	GND	Logic ground (0V)
V_{CC}	18, 22, 48	Power	Positive supply voltage
BIAS V	41	Power	Live insertion pre-bias pin
BG V_{CC}	44	Power	Band Gap threshold voltage reference
BG GND	42	GND	Band Gap threshold voltage reference ground
SABn	20, 21	Input	Mode select from AI to $\overline{B}$
SBAn	45, 46	Input	Mode select from $\overline{B}$ to AO
LCAB	47	Input	A-to-B clock/latch enable (transparent latch when High)
LCBA	19	Input	B-to-A clock/latch enable (transparent latch when High)
Loopback	7	Input	Enables loopback function when High (from AIn to AOn)

LOGIC DIAGRAM



8-bit Futurebus+ transceiver | FB2040A

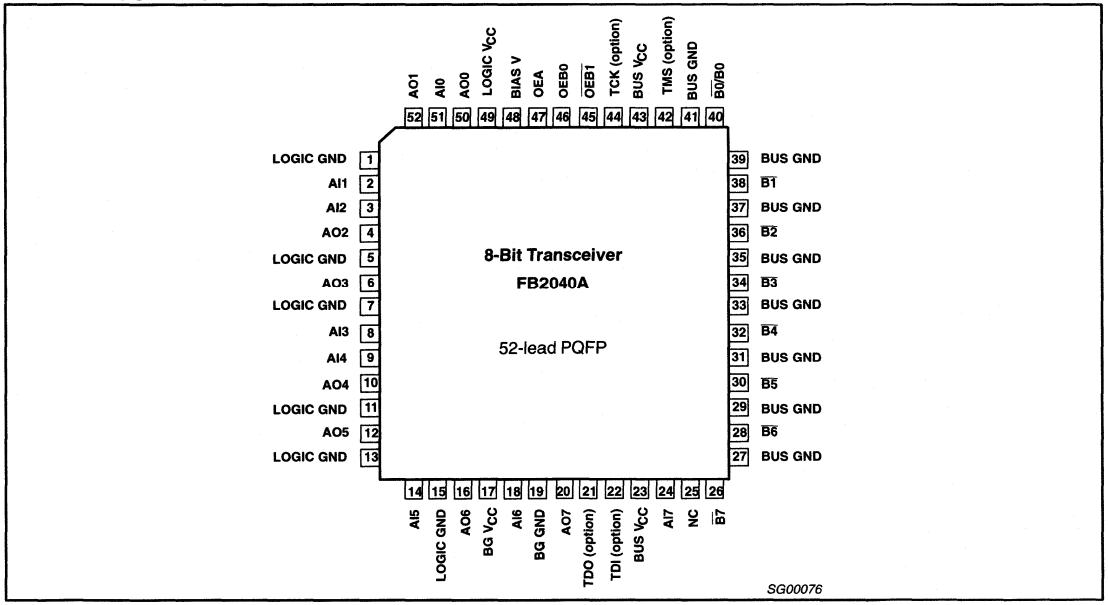
FEATURES

- 8-bit BTL transceivers
- Separate I/O on TTL A-port
- Inverting
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Each BTL driver has a dedicated Bus GND for a signal return
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flat Pack

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C	DRAWING NUMBER
52-pin Plastic Quad Flat Pack (QFP)	FB2040BB	SOT379-1

PIN CONFIGURATION



DESCRIPTION

The FB2040A is an 8-bit bidirectional BTL transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. The FB2040A is an inverting transceiver.

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to "Backplane Transceiver Logic" (See the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1Vp-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

The A-port operates at TTL levels with separate I/O. The 3-state A-port drivers are enabled when OEA goes High after an extra 6ns

delay which is built in to provide a break-before-make function. When OEA goes Low, A-port drivers become High impedance without any extra delay. During power on/off cycles, the A-port drivers are held in a High impedance state when V_{CC} is below 2.5V.

The B-port has two output enables, OEB0 and $\overline{OEB1}$. When OEB0 is High and $\overline{OEB1}$ is Low the output is enabled. When OEB0 is Low or if $\overline{OEB1}$ is High, the B-port is inactive and is at the level of the backplane signal.

To support live insertion, OEB0 is held Low during power on/off cycles to insure glitch free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 5V level while V_{CC} is Low. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated in the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be very infrequent and impossible to trouble-shoot.

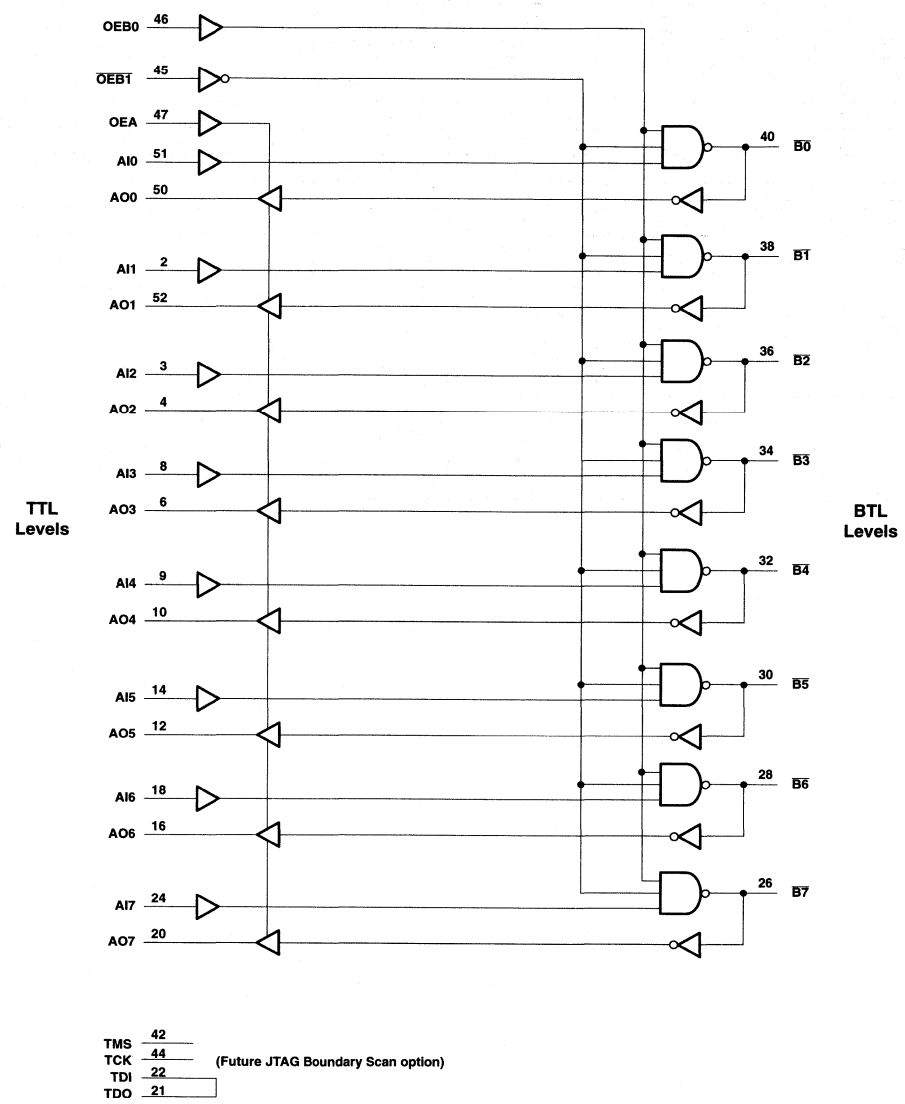
The LOGIC V_{CC} and BUS V_{CC} pins are also isolated internally to minimize noise and may be externally decoupled separately or simply tied together.

JTAG boundary scan pins are provided with signals TMS, TCK, TDI and TDO. TMS and TCK are no-connects (no bond wires) and TDI and TDO are shorted together internally. Boundary scan functionality is not implemented at this time.

PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
AI0 – AI7	51, 2, 3, 8, 9, 14, 18, 24	Input	Data inputs (TTL)
AO0 – AO7	50, 52, 4, 6, 10, 12, 16, 20	Output	3-state outputs (TTL)
$\overline{B0}$ – $\overline{B7}$	40, 38, 36, 34, 32, 30, 28, 26	I/O	Data inputs/Open Collector outputs. High current drive (BTL)
OEB0	46	Input	Enables the B outputs when High
$\overline{OEB1}$	45	Input	Enables the B outputs when Low
OEA	47	Input	Enables the A outputs when High
BUS GND	41, 39, 37, 35, 33, 31, 29, 27	GND	Bus ground (0V)
LOGIC GND	1, 5, 7, 11, 13, 15	GND	Logic ground (0V)
BUS V_{CC}	23, 43	Power	Positive supply voltage
LOGIC V_{CC}	49	Power	Positive supply voltage
BG V_{CC}	17	Power	Band Gap threshold voltage reference
BG GND	19	GND	Band Gap threshold voltage reference ground
BIAS V	48	Power	Live insertion pre-bias pin
TMS	42	Input	Test Mode Select (optional, if not implemented then no-connect)
TCK	44	Input	Test Clock (optional, if not implemented then no-connect)
TDI	22	Input	Test Data In (optional, if not implemented then shorted to TDO)
TDO	21	Output	Test Data Out (optional, if not implemented then shorted to TDI)
NC	25	NC	No Connect

LOGIC DIAGRAM FOR FB2040



NC = 25
LOGIC V_{CC} = 49
LOGIC GND = 1, 5, 7, 11, 13, 15
BUS V_{CC} = 23, 43
BUS GND = 27, 29, 31, 33, 35, 37, 39, 41
BIAS V = 48
BG V_{CC} = 17
BG GND = 19

SG00077

7-bit Futurebus+ transceiver FB2041

DESCRIPTION

The FB2041 is a 7-bit bidirectional BTL transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. The FB2041 is an inverting transceiver.

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

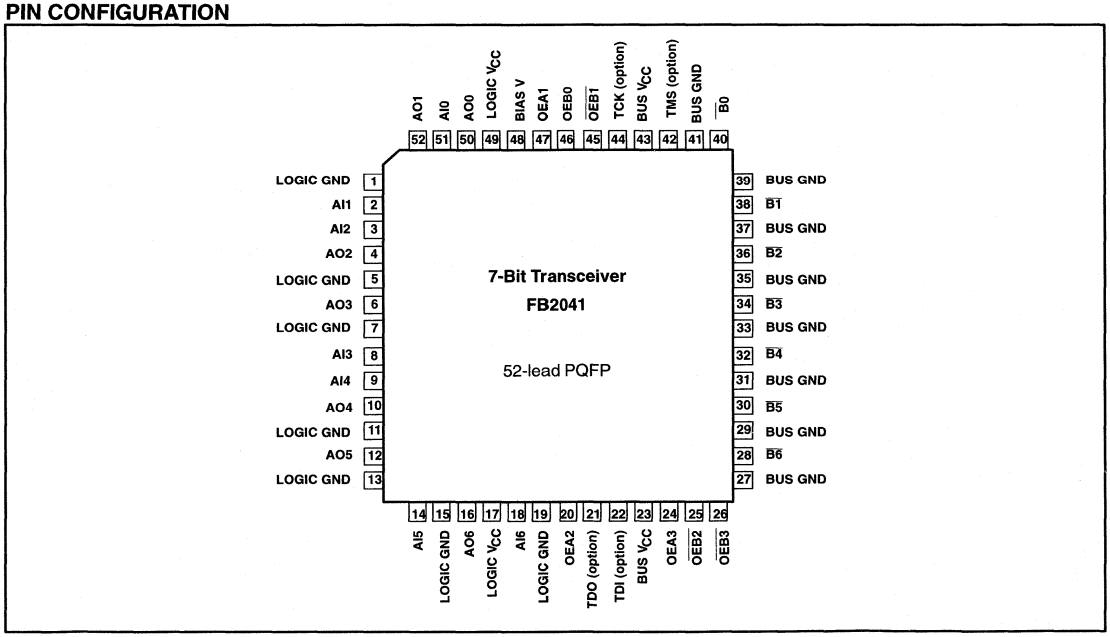
FEATURES

- 7-bit BTL transceiver
- Separate I/O on TTL A-port
- Inverting
- Three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Each BTL driver has a dedicated Bus GND for a signal return
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flatpack

ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0 to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10%; T_{amb} = -40 to +85°C	DWG No.
52-pin Plastic Quad Flatpack	FB2041BB	CD3207BB	SOT379-1

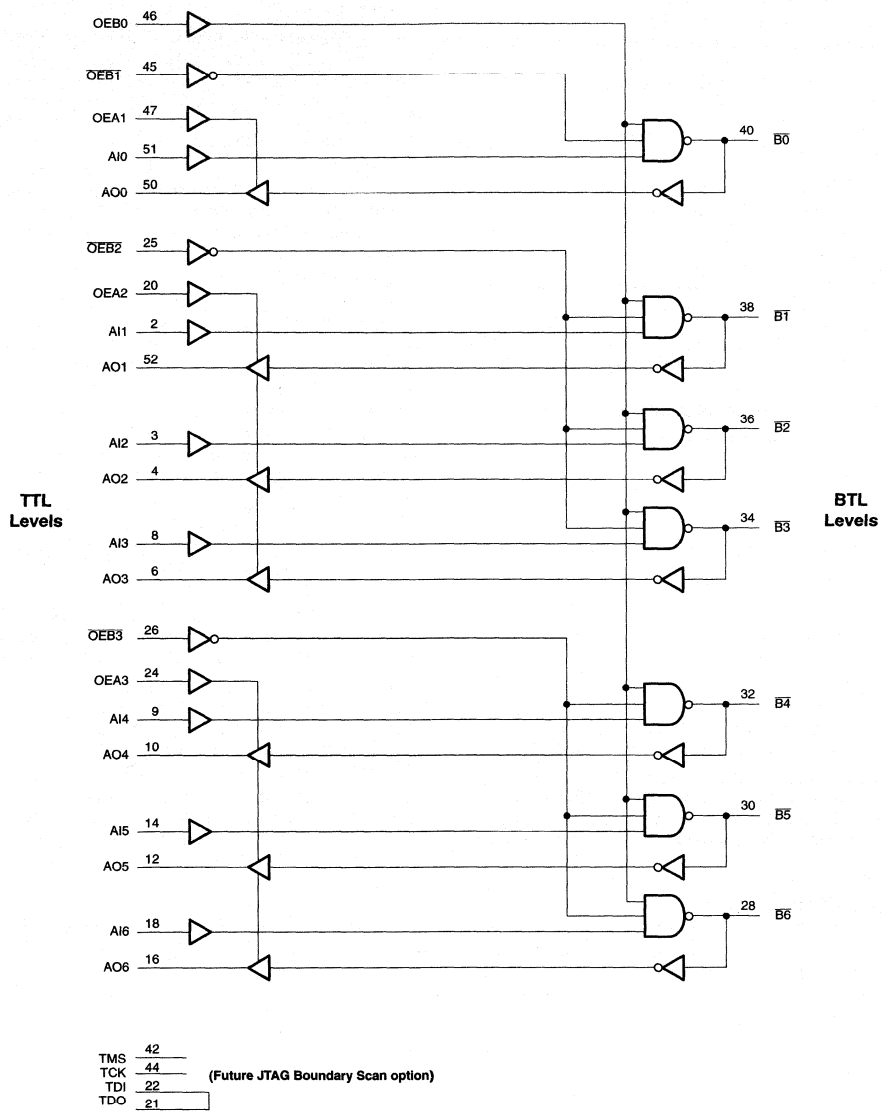
PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
AI0 – AI6	51, 2, 3, 8, 9, 14, 18	Input	Data inputs (TTL)
AO0 – AO6	50, 52, 4, 6, 10, 12, 16	Output	3-state outputs (TTL)
$\overline{B0}$ – $\overline{B6}$	40, 38, 36, 34, 32, 30, 28	I/O	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	46	Input	Enables the Bn outputs when High
$\overline{OEB1}$	45	Input	Enables the B0 output when Low
$\overline{OEB2}$	25	Input	Enables the B1 – B3 outputs when Low
$\overline{OEB3}$	26	Input	Enables the B4 – B6 outputs when Low
OEA1	47	Input	Enables the A0 outputs when High
OEA2	20	Input	Enables the A1 – A3 outputs when High
OEA3	24	Input	Enables the A4 – A6 outputs when High
BUS GND	41, 39, 37, 35, 33, 31, 29, 27	GND	Bus ground (0V)
LOGIC GND	1, 5, 7, 11, 13, 15, 19	GND	Logic ground (0V)
BUS V_{CC}	23, 43	Power	Positive supply voltage
LOGIC V_{CC}	17, 49	Power	Positive supply voltage
BIAS V	48	Power	Positive supply voltage
TMS	42	Input	Test Mode Select (no-connect)
TCK	44	Input	Test Clock (no-connect)
TDI	22	Input	Test Data In (shorted to TDO)
TDO	21	Output	Test Data Out (TDI)

LOGIC DIAGRAM



LOGIC V_{CC} = 17, 49
LOGIC GND = 1, 5, 7, 11, 13, 15, 19
BUS V_{CC} = 23, 43
BUS GND = 27, 29, 31, 33, 35, 37, 39, 41
BIAS V = 48

SG00071

3.3V BTL 7-bit Futurebus+ transceiver (standard A-port)

FBL2041
FBL2041I

FEATURES

- 7-bit BTL transceiver
- Separate I/O on TTL A-port
- Inverting
- Three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Each BTL driver has a dedicated Bus GND for a signal return
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flatpack
- 5V compatible I/O on A-port
- Industrial temperature range option available as FBL2041I

DESCRIPTION

The FBL2041/FBL2041I is a 7-bit bidirectional BTL transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. The FBL2041 is an inverting transceiver.

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The FBL2041/FBL2041I is pin and function compatible with FB2041 but operates at a 3.3V supply voltage, greatly reducing power consumption.

The B-port interfaces to "Backplane Transceiver Logic" (See the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1Vp-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

There are three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement. The TTL/BTL output drivers for bit 0 are enabled with OEA1/$\overline{\text{OEB1}}$, output drivers for bits 1–2–3 are enabled with OEA2/$\overline{\text{OEB2}}$ and output drivers for bits 4–5–6 are enabled with OEA3/$\overline{\text{OEB3}}$.

The A-port operates at TTL levels with separate I/O. The 3-state A-port drivers are enabled when OEAn goes High after an extra 6ns delay which is built in to provide a break-before-make function. When OEAn goes Low, A-port drivers become High impedance without any extra delay. During power on/off cycles, the A-port drivers are held in a High impedance state when V_{CC} is below 1.3V.

The B-port has an output enable, OEB0, which affects all seven drivers. When OEB0 is High and $\overline{\text{OEBn}}$ is Low the output driver will be enabled. When OEB0 is Low or if $\overline{\text{OEBn}}$ is High, the B-port drivers will be inactive and at the level of the backplane signal.

To support live insertion, OEB0 is held Low during power on/off cycles to insure glitch free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 3.3V level while V_{CC} is Low. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated in the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be very infrequent and impossible to trouble-shoot.

JTAG boundary scan functionality is provided as an option with signals TMS, TCK, TDI and TDO. When this option is not present, TMS and TCK are no-connects (no bond wires) and TDI and TDO are shorted together internally.

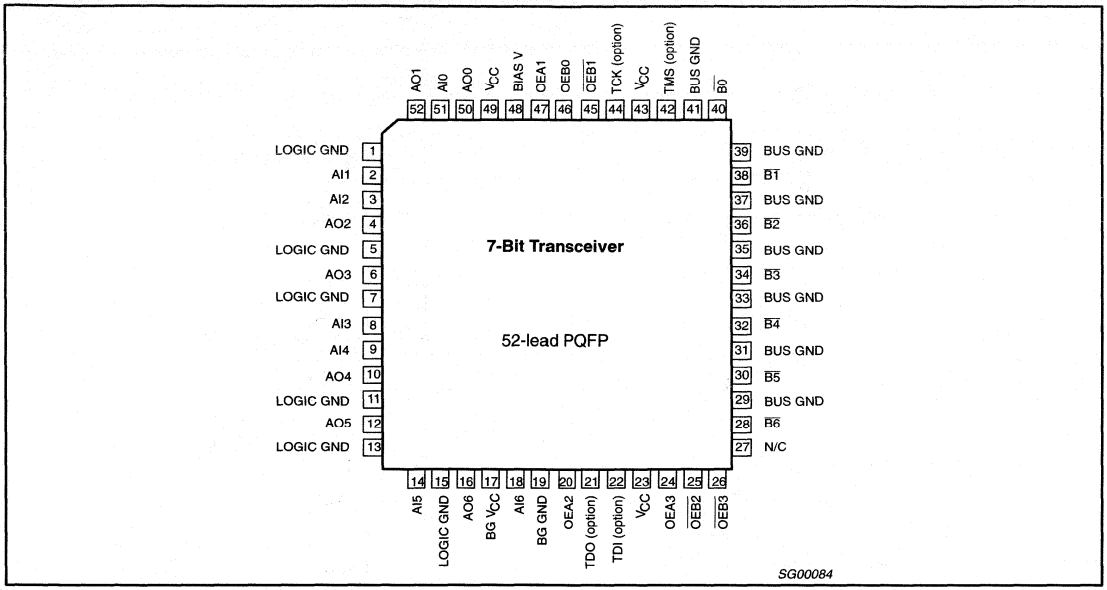
ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE V_{CC} = 3.3V±10%; T_{amb} = 0 to +70°C	INDUSTRIAL RANGE V_{CC} = 3.3V±10%; T_{amb} = –40 to +85°C	DWG No.
52-pin Plastic Quad Flatpack	FBL2041 BB	FBL2041I BB	SOT379-1

3.3V BTL 7-bit Futurebus+ transceiver (standard A-port)

FBL2041
FBL2041I

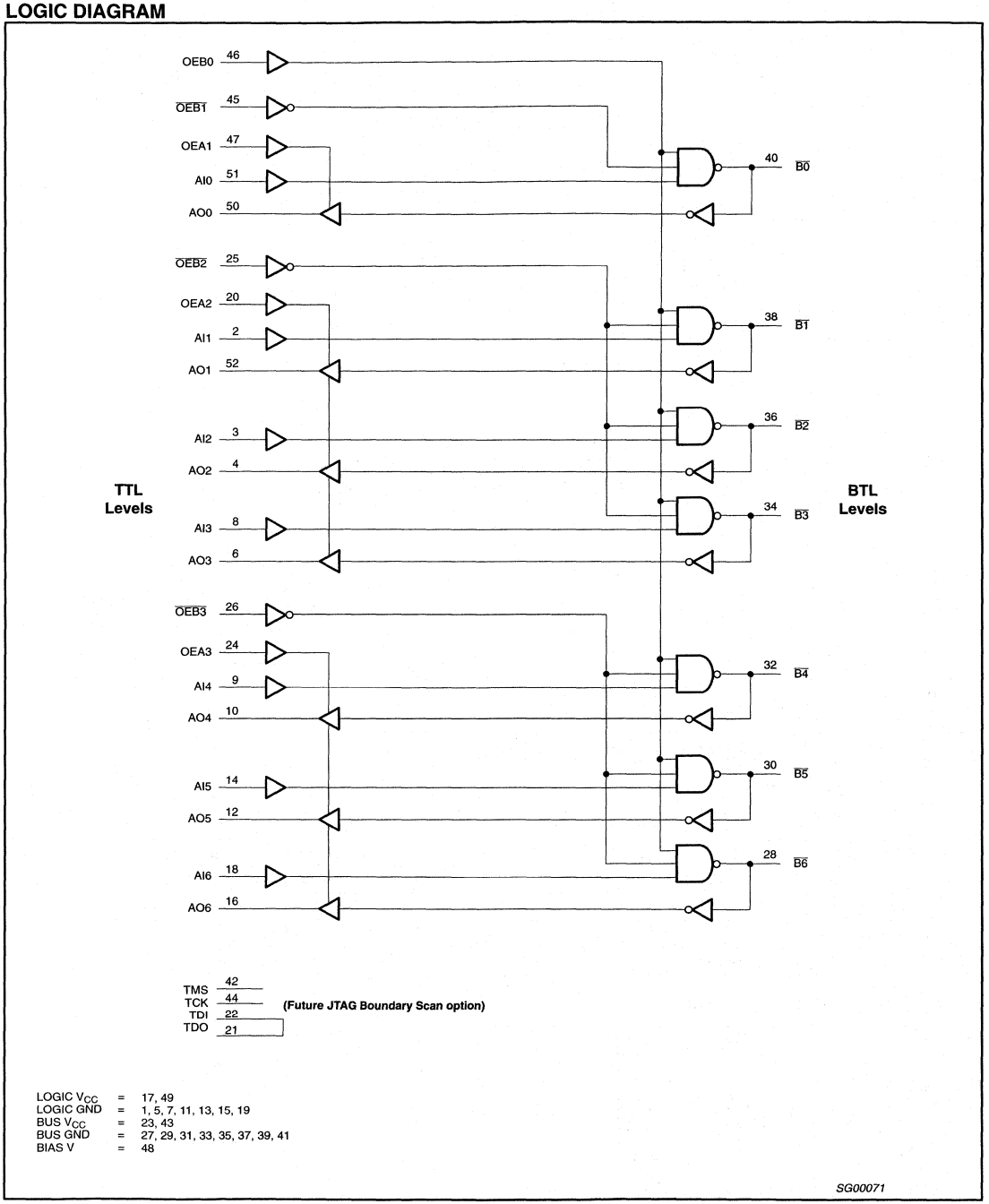
PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
AI0 – AI6	51, 2, 3, 8, 9, 14, 18	Input	Data inputs (TTL)
AO0 – AO6	50, 52, 4, 6, 10, 12, 16	Output	3-State outputs (TTL)
$\overline{B0}$ – $\overline{B6}$	40, 38, 36, 34, 32, 30, 28	I/O	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	46	Input	Enables the Bn outputs when High
$\overline{OEB1}$	45	Input	Enables the B0 output when Low
$\overline{OEB2}$	25	Input	Enables the B1 – B3 outputs when Low
$\overline{OEB3}$	26	Input	Enables the B4 – B6 outputs when Low
OEA1	47	Input	Enables the A0 outputs when High
OEA2	20	Input	Enables the A1 – A3 outputs when High
OEA3	24	Input	Enables the A4 – A6 outputs when High
BUS GND	41, 39, 37, 35, 33, 31, 29	GND	Bus ground (0V)
LOGIC GND	1, 5, 7, 11, 13, 15	GND	Logic ground (0V)
LOGIC/bus V_{CC}	23, 43, 49	Power	Positive supply voltage
BG V_{CC}	17	Power	Positive supply voltage BAND GAP
BIAS V	48	Power	Positive supply voltage
TMS	42	Input	Test Mode Select (no-connect)
TCK	44	Input	Test Clock (no-connect)
TDI	22	Input	Test Data In (shorted to TDO)
TDO	21	Output	Test Data Out (TDI)
BG GND	19	GND	BAND GAP GROUND (0V)

LOGIC DIAGRAM



LOGIC V_{CC} = 17, 49
LOGIC GND = 1, 5, 7, 11, 13, 15, 19
BUS V_{CC} = 23, 43
BUS GND = 27, 29, 31, 33, 35, 37, 39, 41
BIAS V = 48

SG00071

3.3V BTL 7-bit Futurebus+ transceiver (standard A-port) FBL22041

FEATURES

- 7-bit BTL transceiver
- Separate I/O on TTL A-port
- Inverting
- Three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Each BTL driver has a dedicated Bus GND for a signal return
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flatpack
- 5V compatible I/O on A-port
- The A port includes a series resistor of 30Ω making external terminating resistors unnecessary

DESCRIPTION

The FBL22041 is a 7-bit bidirectional BTL transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. The FBL22041 is an inverting transceiver.

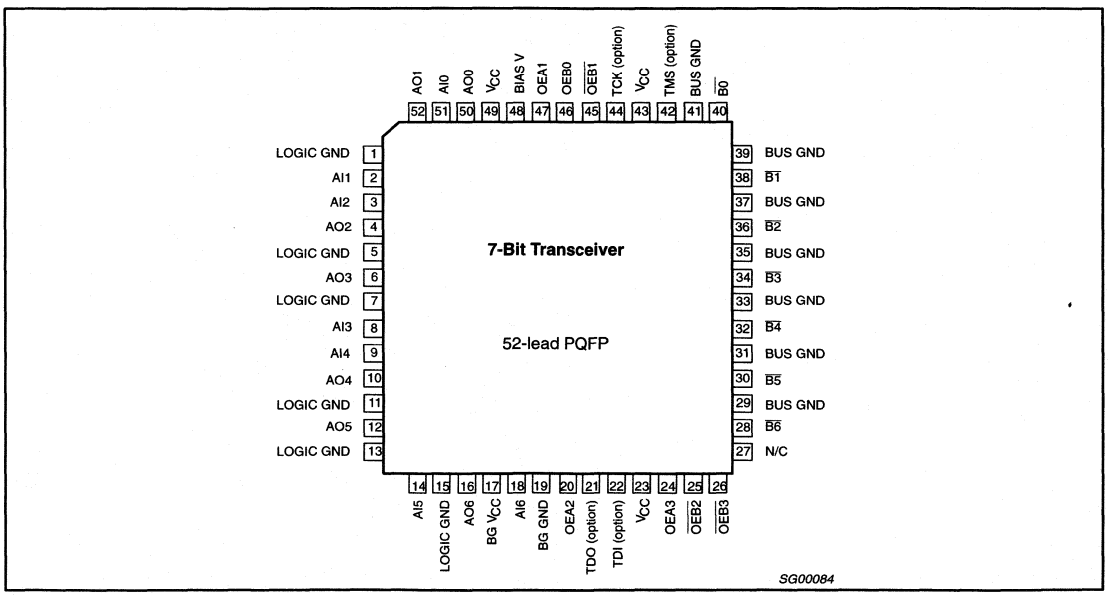
The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The FBL22041 is designed with a 30Ω series resistance in both the HIGH and LOW states of the output.

The FBL22041 is pin and function compatible with FB2041 but operates at a 3.3V supply voltage, greatly reducing power consumption.

ORDERING INFORMATION

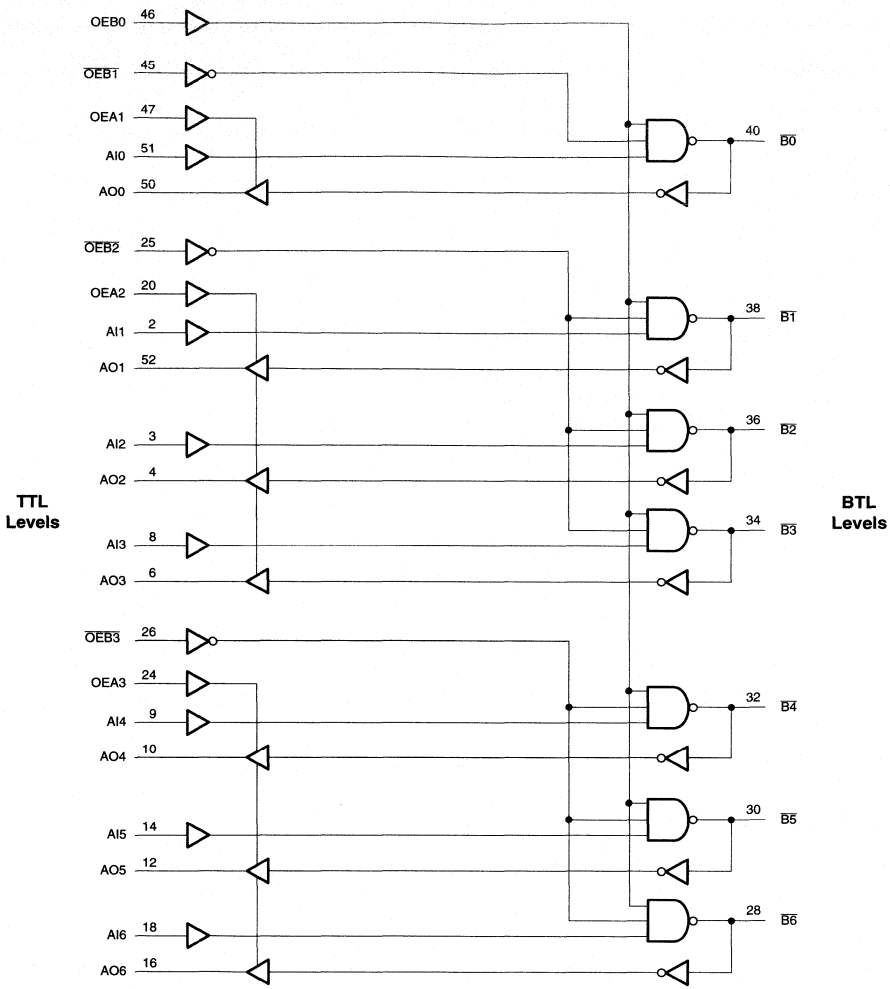
PACKAGE	COMMERCIAL RANGE V_{CC} = 3.3V±10%; T_{amb} = 0 to +70°C	DWG No.
52-pin Plastic Quad Flatpack	FBL22041BB	SOT379-1



PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
ai0 – ai6	51, 2, 3, 8, 9, 14, 18	Input	Data inputs (TTL)
aO0 – aO6	50, 52, 4, 6, 10, 12, 16	Output	3-state outputs (TTL)
$\overline{b0}$ – $\overline{b6}$	40, 38, 36, 34, 32, 30, 28	i/o	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	46	Input	Enables the Bn outputs when High
OEB1	45	Input	Enables the B0 output when Low
OEB2	25	Input	Enables the B1 – B3 outputs when Low
OEB3	26	Input	Enables the B4 – B6 outputs when Low
OEA1	47	Input	Enables the A0 outputs when High
OEA2	20	Input	Enables the A1 – A3 outputs when High
OEA3	24	Input	Enables the A4 – A6 outputs when High
bus gnd	41, 39, 37, 35, 33, 31, 29	GND	Bus ground (0V)
LOGIC gnd	1, 5, 7, 11, 13, 15	GND	Logic ground (0V)
LOGIC/bus V_{CC}	23, 43, 49	Power	Positive supply voltage
BG V_{CC}	17	Power	Positive supply voltage BAND GAP
BIAS V	48	Power	Positive supply voltage
TMS	42	Input	Test Mode Select (no-connect)
Tck	44	Input	Test Clock (no-connect)
Tdi	22	Input	Test Data In (shorted to TDO)
Tdo	21	Output	Test Data Out (TDI)
BG GND	19	GND	BAND GAP GROUND (0V)

LOGIC DIAGRAM



LOGIC V_{CC} = 17, 49
LOGIC GND = 1, 5, 7, 11, 13, 15, 19
BUS V_{CC} = 23, 43
BUS GND = 27, 29, 31, 33, 35, 37, 39, 41
BIAS V = 48

SG00071

Section 8
Wireless Local Area Network

CONTENTS

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SA7016	1.3GHz low voltage fractional-N synthesizer	312
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SA8026	2.5GHz low voltage fractional–N dual synthesizer	319
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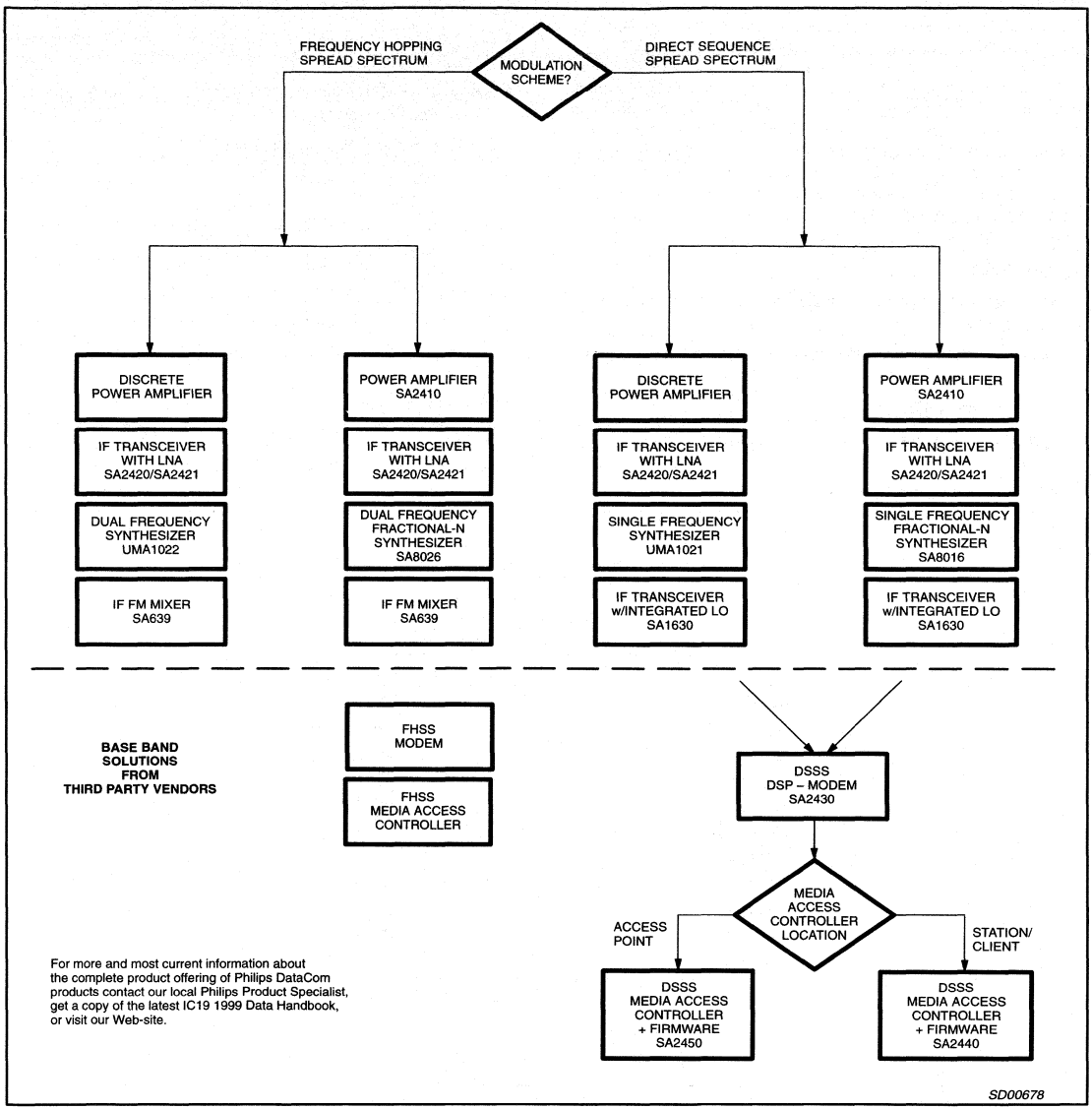
Wireless LAN selection guide



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IF quadrature transceiver SA1630

DESCRIPTION

The SA1630 is a 70–400 MHz I/Q transceiver for wireless LAN. The Receive Path contains a digitally gain controlled linear IF amplifier, a pair of quadrature down conversion mixers and a pair of baseband amplifiers. The transmit path contains a pair of quadrature up conversion mixers that transposes a quadrature baseband input signal up to IF frequency. An external VCO signal is divided internally and provides quadrature local oscillator signals for the mixers. Another divider chain, reference divider and phase detector are provided to avoid the need for an external synthesizer. To keep power consumption to a minimum the transmit, receive and local oscillator functions can be powered down under digital control.

FEATURES

- Low supply voltage operation of 2.7V for main chip and 2.9V for charge pump.
- Low current consumption: 33.5 mA in RX, 26.5 mA in TX, typical at 3V.
- Flexible power up/down options.
- Optional 2.5V regulated reference voltage available during transmit.
- Input IF frequency range of 70–400 MHz.
- Internal IF PLL for synthesizing the local IF oscillator signal.
- Bandwidth of baseband Tx inputs is 20 MHz and that of baseband Rx outputs is 8.5MHz.
- Designed for IEEE 802.11 wireless LAN using Direct Sequence Spread Spectrum modulation.
- Control registers power up in a default state.
- Only a standard reference input frequency required, choice of 8, 11, 22 or 44 MHz.
- Digital gain control of 70 dB in steps of 2 dB.
- Rx Baseband amplifiers are capable of driving 1kΩ ||15pF
- Rx Baseband o/p's clamp symmetrically, above 1Vp–p in order to prevent dc bias shift under overdrive conditions.
- Package: LQFP–48, PCMCIA compatible

APPLICATIONS

- IF circuitry for IEEE 802.11 DSSS wireless LAN.
- Applications for high speed wireless data.

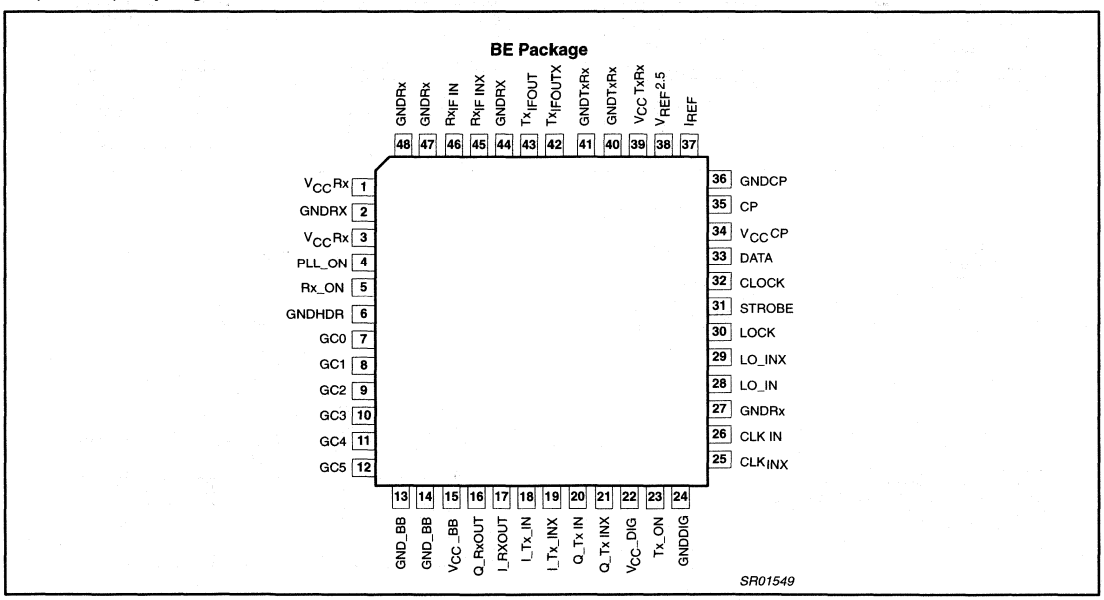


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48–Pin Plastic Low Profile Quad Flat package	–40 to +85°C	SA1630BE	SOT313–2

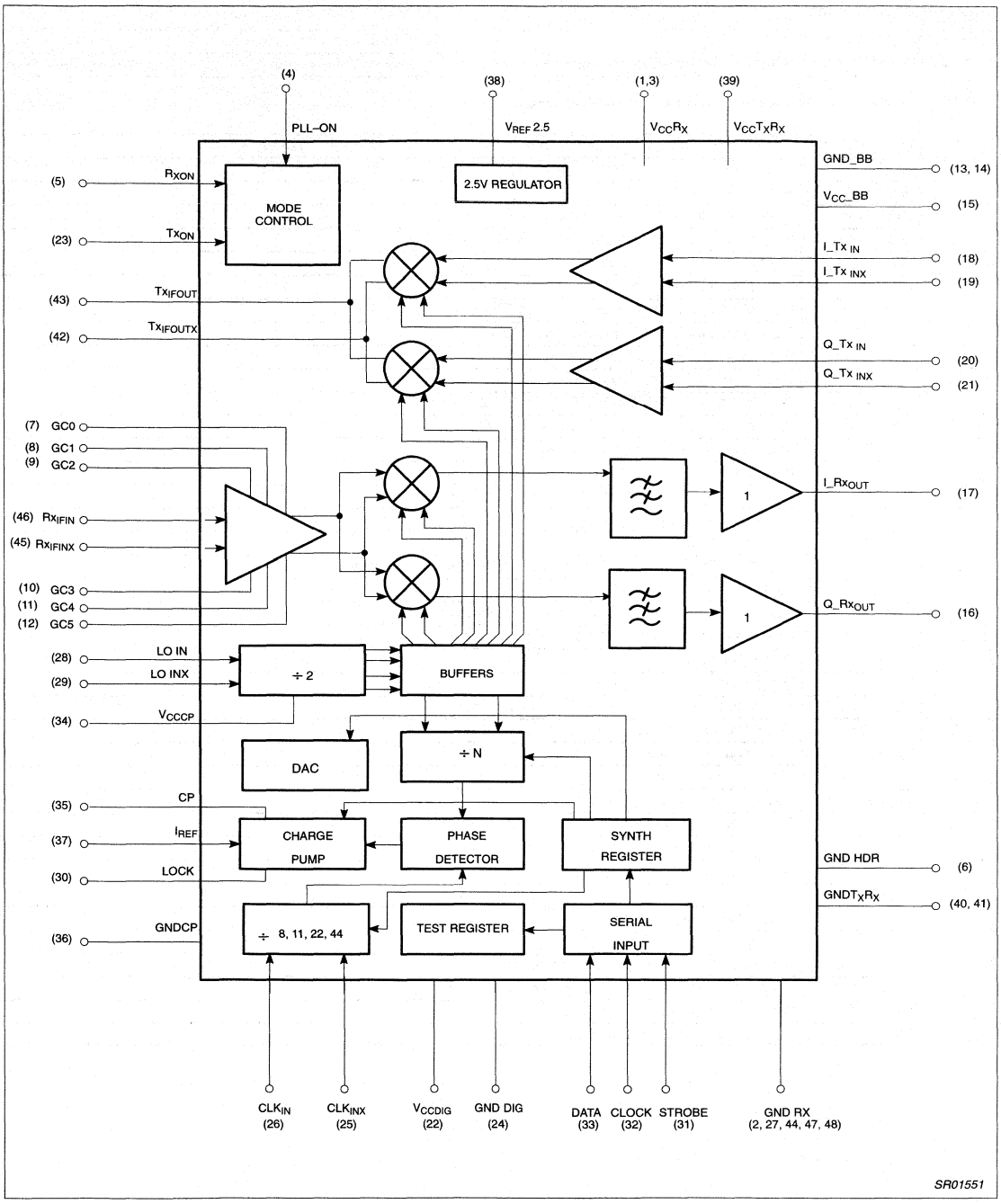


Figure 2. Block Diagram

PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1, 3	V_{CC}Rx	Supply Pin for Rx section (IF circuits)
2, 27, 44,47, 48	GNDRx	Ground pins for Rx section (IF circuits)
4	PLL_ON	One of the three digital CMOS logic control inputs to the mode control section
5	Rx_ON	One of the three digital CMOS logic control inputs to the mode control section
6	GNDHDR	Substrate ground
7	GC0	Control bit 0 for IF VGA gain control, CMOS input
8	GC1	Control bit 1 for IF VGA gain control, CMOS input
9	GC2	Control bit 2 for IF VGA gain control, CMOS input
10	GC3	Control bit 3 for IF VGA gain control, CMOS input
11	GC4	Control bit 4 for IF VGA gain control, CMOS input
12	GC5	Control bit 5 for IF VGA gain control, CMOS input
13, 14	GND_BB	Ground pin for Rx baseband circuits
15	V_{CC}_BB	Supply Pin for Rx Baseband circuits
16	Q_RXOUT	Quadrature–phase Rx baseband output, single–ended
17	I_RxOUT	In–phase Rx baseband output, single–ended
18	I_Tx IN	In–phase differential Tx baseband input, positive
19	I_Tx INX	In–phase differential Tx baseband input, negative
20	Q_Tx IN	Quadrature differential Tx baseband input, positive
21	Q_Tx INX	Quadrature differential Tx baseband input, negative
22	V_{CC}_DIG	Supply for digital circuits
23	Tx_ON	One of the Three digital CMOS logic control inputs to the mode control section
24	GNDDIG	Digital ground
25	CLK INX	Differential reference input for synthesizer, negative
26	CLK IN	Differential reference input for synthesizer, positive
28	LO_IN	Differential LO input,positive
29	LO INX	Differential LO input, negative
30	LOCK	Test control output and synthesizer lock indicator
31	STROBE	Serial bus strobe input
32	CLOCK	Serial bus clock input
33	DATA	Serial bus data input
34	V_{CC}CP	Supply for charge pump circuits
35	CP	Charge pump output
36	GNDCP	Ground for charge pump circuits
37	I_{REF}	Charge pump reference current
38	V_{REF}2.5	Reference voltage of 2.5V available for external use
39	V_{CC}TxRx	Supply pin used by Tx circuits
40,41	GNDTxRx	Ground pins used by Tx circuits
42	TxIFOUTX	Differential transmitter IF output (open collector), positive
43	TxIFOUT	Differential transmitter IF output (open collector), negative
45	RxIF INX	Differential receiver IF input, negative
46	RxIF IN	Differential receiver IF input, positive

Low voltage IF I/Q transceiver SA1638

DESCRIPTION

The SA1638 is a combined Rx and Tx IF I/Q circuit. The receive path contains an IF amplifier, a pair of quadrature down-mixers, and a pair of baseband filters and amplifiers. A second pair of mixers in the transmit path transposes a quadrature baseband input up to the IF frequency. An external VCO signal is divided down internally and buffered to provide quadrature local oscillator signals for the mixers. A further divider chain, reference divider and phase detector are provided to avoid the need for an external IF synthesizer. Rx or Tx path or the entire circuit may be powered down by logic inputs. On-board voltage regulators are provided to allow direct connection to a battery supply.

FEATURES

- Direct supply: 3.3V to 7.5V
- Two DC regulators giving 3.0V output
- Low current consumption: 18mA for Rx or 22mA for Tx
- Input/output IF frequency from 70-400 MHz
- Internal IF PLL for synthesizing the local oscillator signal
- High performance on-board integrated receive filters with bandwidth tunable between 50-850 kHz
- Switchable alternative bandwidth setting available to allow channel bandwidth flexibility in operation
- Designed for a widely used I and Q baseband GSM interface
- Control registers power up in a default state
- Optional DC offset trim capability to <200mV
- Only a standard reference input frequency required, choice of 13, 26, 39 or 52MHz
- Fully compatible with SA1620 GSM RF front-end (see Figure 9, included in CD-ROM version)

APPLICATIONS

- IF circuitry for GSM 900MHz hand-held units
- IF circuitry for PCN (DCS1800) hand-held units
- Quadrature up and down mixer stage

PIN CONFIGURATION

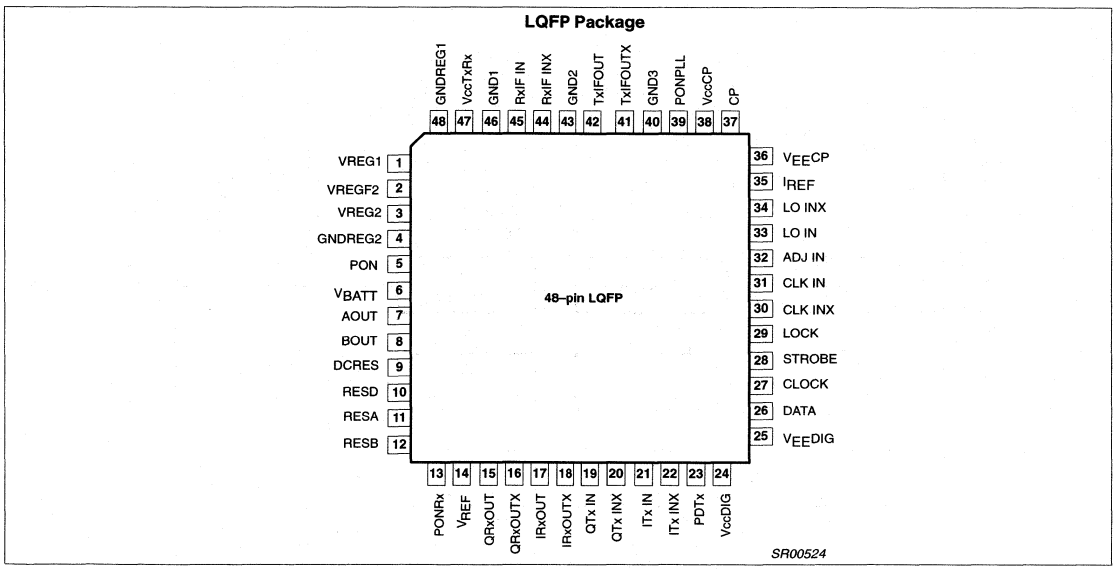


Figure 1. SA1638 Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
48-Pin Thin Quad Flat Pack (LQFP)	-40 to +85°C	SA1638BE	SOT313-2

BLOCK DIAGRAM

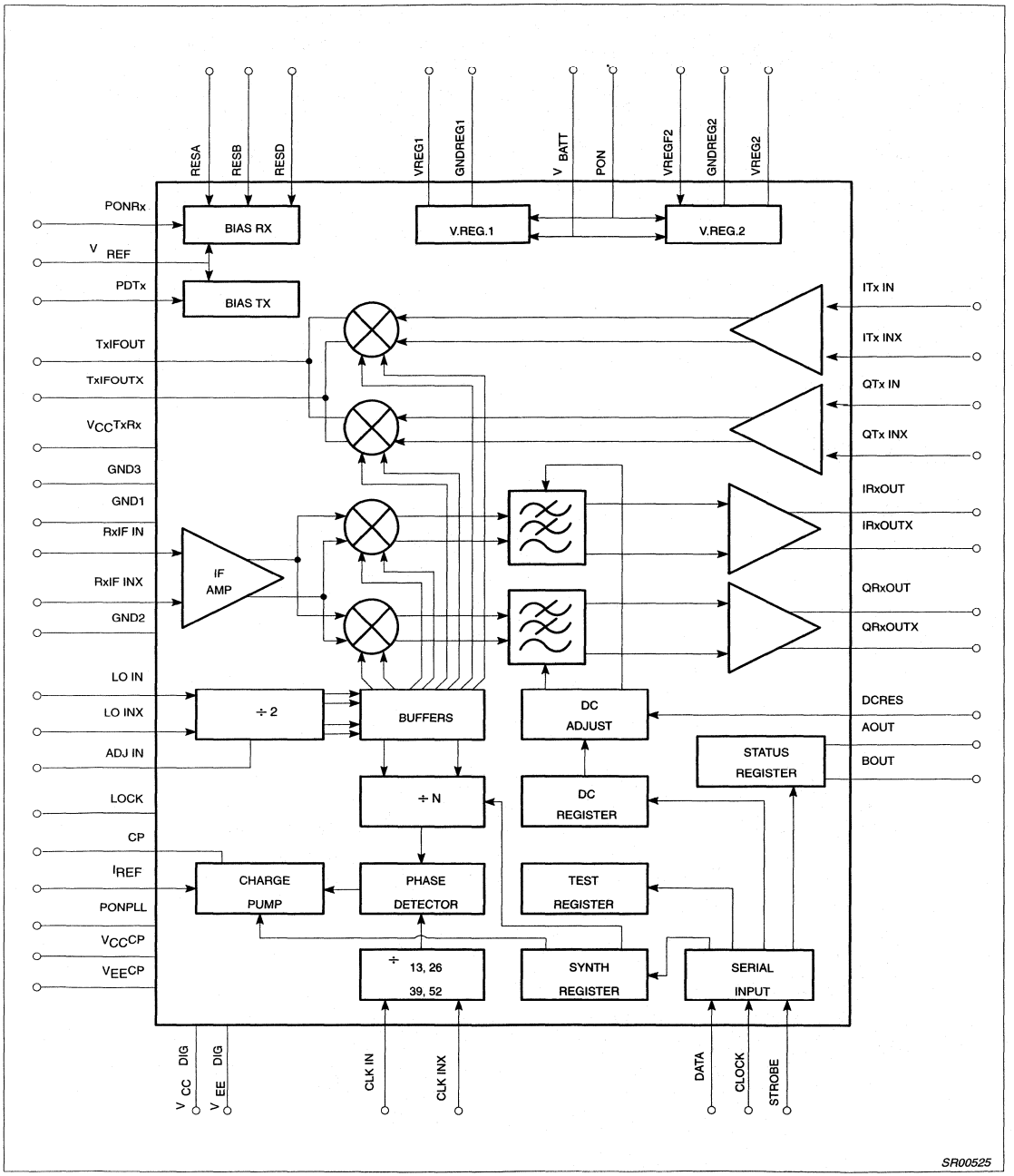


Figure 2. SA1638 Block Diagram

PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1	VREG1	Output voltage of regulator 1
2	VREGF2	Feedback of regulator 2
3	VREG2	Output voltage of regulator 2
4	GNDREG2	Ground of regulator 2
5	PON	Power-on input for voltage regulators 1 and 2 (active high)
6	V_{BATT}	Input voltage for regulators 1 and 2
7	AOUT	Programmable logic output (see Figure 9, included in CD-ROM version)
8	BOUT	Programmable logic output (see Figure 9, included in CD-ROM version)
9	DCRES	Reference current setting resistor for DC offset circuit
10	RESD	Additional external current defining resistor for filters
11	RESA	Principal external current defining resistor for filters
12	RESB	Principal external current defining resistor for filters
13	PONRx	Power-on input for Rx (active high)
14	V_{REF}	Reference voltage
15	QRxOUT	Differential receive baseband output
16	QRxOUTX	Differential receive baseband output
17	IRxOUT	Differential receive baseband output
18	IRxOUTX	Differential receive baseband output
19	QTx IN	Differential transmit baseband input
20	QTx INX	Differential transmit baseband input
21	ITx IN	Differential transmit baseband input
22	ITx INX	Differential transmit baseband input
23	PDTx	Power-on for transmitter (active low)
24	V_{CC}DIG	Digital circuit supply
25	V_{EE}DIG	Digital ground
26	DATA	Serial bus data input
27	CLOCK	Serial bus clock input
28	STROBE	Serial bus strobe input
29	LOCK	Test control/synthesizer lock indicator
30	CLK INX	Differential reference divider input
31	CLK IN	Differential reference divider input
32	ADJ IN	Used for test only. Do not connect
33	LO IN	Differential LO input
34	LO INX	Differential LO input
35	I_{REF}	Reference current setting for charge pump
36	V_{EE}CP	Charge pump ground
37	CP	Charge pump output
38	V_{CC}CP	Charge pump circuit supply
39	POnPLL	Power-on input for synthesizer circuits (active high)
40	GND3	Ground (internal connection to GND1 and GND2)
41	TxIFOUTX	Differential transmit IFoutput (open collector)
42	TxIFOUT	Differential transmit IFoutput (open collector)
43	GND2	Ground (internal connection to GND1 and GND3)
44	RxIF INX	Differential receive IF input
45	RxIF IN	Differential receive IF input
46	GND1	Ground (internal connection to GND2 and GND3)
47	V_{CC}TxRx	Transmit and receive circuits supply voltage (also feedback of Regulator 1)
48	GNDREG1	Ground of regulator 1

NOTE: There are no ESD protection diodes at Pins 41 and 42. Thus, open collector outputs may have increased DC voltage or higher AC peak voltage.

2.45GHz RF power amplifier and T/R switch SA2410

DESCRIPTION

The SA2410 is a GaAs monolithic power amplifier with an integrated T/R switch designed to meet requirements for 802.11 (WLAN). The SA2410 uses an on–chip 4 GHz oscillator to generate the negative bias, thus eliminating the need for a negative supply. It operates from 3V to 5.5V and consumes 125 mA with an output power of 18.5 dB (typ). It is suitable for other 2.45 GHz ISM band applications.

FEATURES

- V_{CC}=3V–5.5V
- No negative bias needed
- I_{CC}=125mA (typ) @ 3.3V
- P_{OUT}=18.5 dB(typ)
  IM3<–30dBc
  IM5<–50dBc
- Gain=29dB (typ)
- Attenuation range=16dB (typ)
- LQFP–32 package

APPLICATIONS

- 802.11 WLAN
- 2.4–2.5 GHz ISM BAND

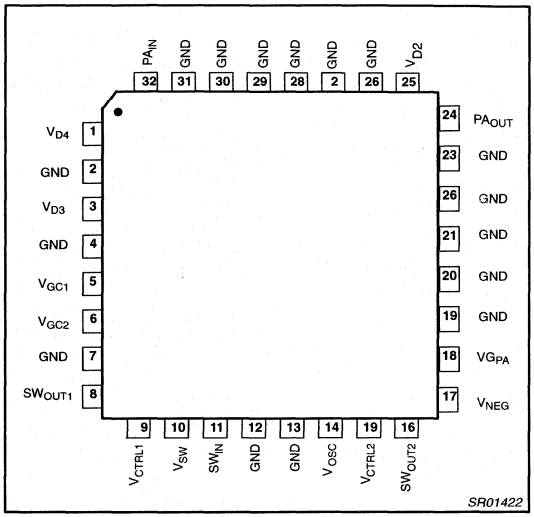


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
32–Pin Plastic Thin Quad Flat Package	–40° C+85°C	SA2410	SOT401–1

GENERAL SPECIFICATIONS

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T	Temperature		–40		+85	C
V_{CC}	Supply V		3		5.5	V
I_{CC}	Supply I	3.3 volts		125		mA
Power Amplifier						
f_{RF}	Frequency Range		2.4		2.5	GHz
IM3	IM3 2 tones		30			dBc
IM5	IM5 2 tones		50			dBc
T_{on}	Transmit power on	Including neg. supply			2	µs
T_{off}	Xmit power down				2	µs
Gain	Small signal gain			29		dB
P_{out}	Output power	IM3=30dBc IM5=50dBc 125mA@3.3 volts	17.5	18.5		dBm
Eff.	Efficiency			25		%
Δ Gt1	Gain variation with temp	–40 to +85°C		±3.5		dB
Δ Gt2	Gain variation with temp	0–70°C		±2.0		dB
Δ Gr	Ripple	2.45±0.05 GHz		±1		dB
Δ Gvd	Gain variation with supply	3.3 volts±0.3 V		0.5		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Negative voltage supply						
t_{on}	Power on time		10		100	nS
	4 GHz spur	Xmit Mode		TBD		dBm
Linear Gain Control						
Symbol	**Parameter**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
V_{GC}	Gain control voltage			TBD		Volt
C_{GC}	Input C at gain pin			TBD		pF
G_{CR}	Attenuation range			16		dB
Transmit/receive switch						
Symbol	**Parameter**	**Condition**	**Min**	**Typ**	**Max**	**Unit**
L_{tx}	Insertion loss T_x			1.3	2	dB
L_{rx}	Insertion loss R_x			1.3	2	dB
t_{sw}	Switch response time				400	nS
ISO_{PA}	Isolation switch to PA		30			dB
Z_{in}	Input impedance			50		Ω
Z_{out}	Output impedance			50		Ω
ISO_{SW}	Switch Isolation		17	19		dB

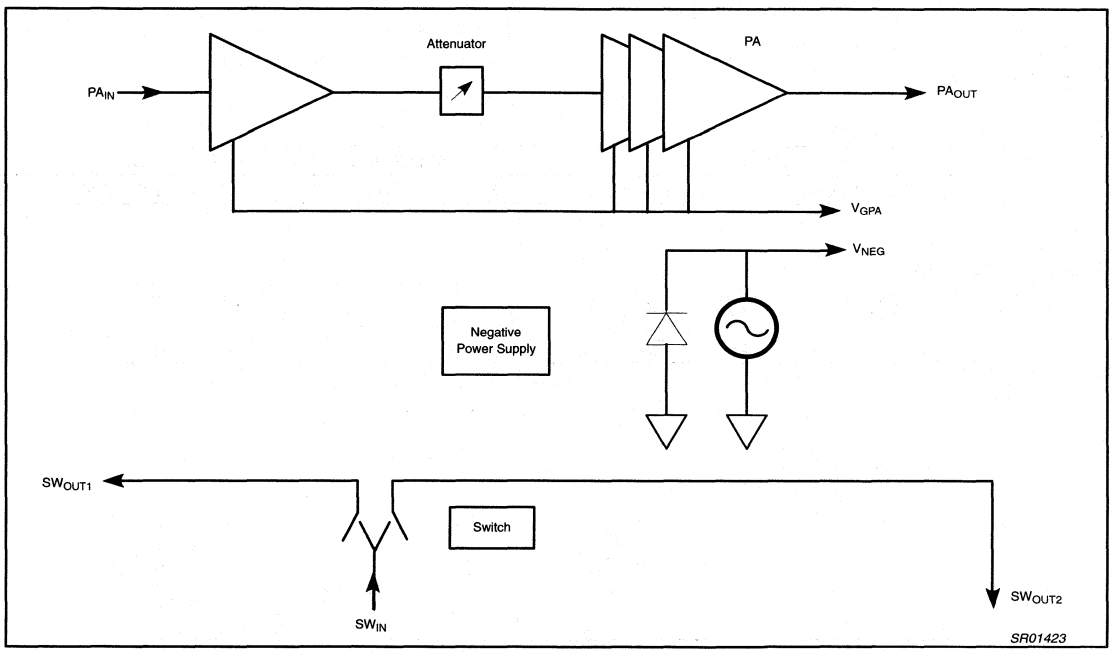


Figure 2. Block Diagram

Low voltage RF transceiver — 2.45 GHz SA2420

DESCRIPTION

The SA2420 transceiver is a combined low-noise amplifier, receive mixer, transmit mixer and LO buffer IC designed for high-performance low-power communication systems for 2.4-2.5GHz applications. The LNA has a 2.5dB noise figure at 2.45GHz with 14dB gain and an IP3 intercept of -3dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over the -40 to +85°C temperature range. The wide-dynamic-range receive mixer has a 10.9dB noise figure and an input IP3 of +2.8dBm at 2.45GHz. The nominal current drawn from a single 3V supply is 37mA in transmit mode and 22mA in receive mode.

FEATURES

- Low current consumption: 37mA nominal transmit mode and 22mA nominal receive mode
- Fabricated on a high volume, rugged BiCMOS technology
- High system power gain: 22.5dB (LNA + Mixer) at 2.45GHz
- TSSOP24 package
- Excellent gain stability versus temperature and supply voltage
- -10dBm LO input power can be used to drive the mixer
- Operates with either full or half frequency LO
- Wide IF range: 50–500MHz

PIN CONFIGURATION

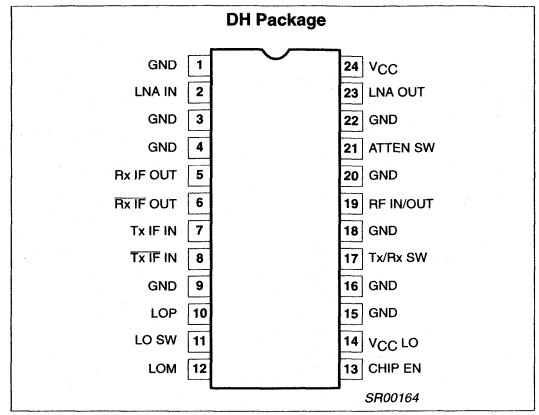


Figure 1. Pin Configuration

APPLICATIONS

- 2.45GHz WLAN front-end (802.11, ISM)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic Thin Shrink Small Outline Package (Surface-mount, TSSOP)	-40 to +85°C	SA2420DH	SOT355-1

BLOCK DIAGRAM

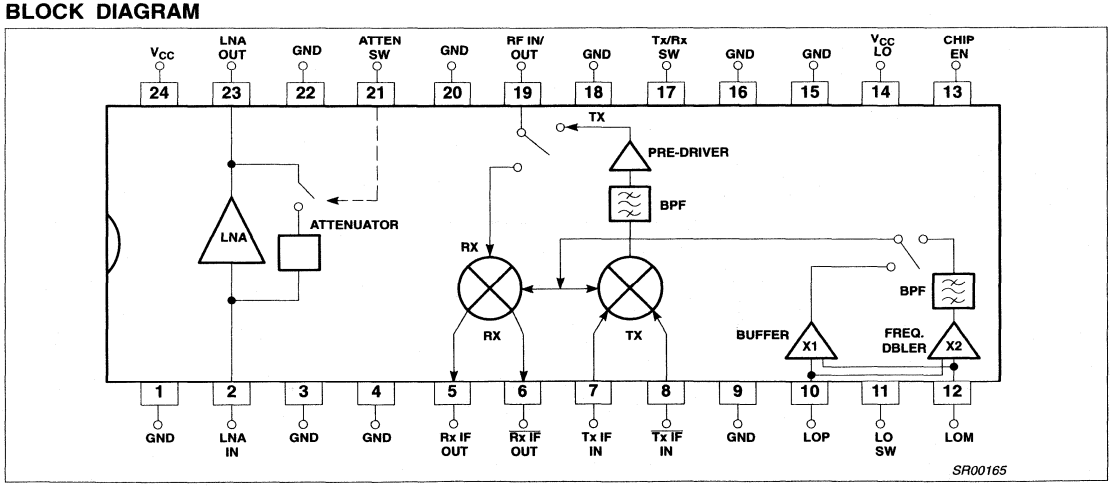


Figure 2. SA2420 Block Diagram

Low voltage RF transceiver — 2.45 GHz SA2421

DESCRIPTION

The SA2421 transceiver is a combined low-noise amplifier, receive mixer, transmit mixer and LO buffer IC designed for high-performance low-power communication systems for 2.4-2.5GHz applications. The LNA has a 2.5dB noise figure at 2.45GHz with 14dB gain and an IP3 intercept of -3dBm at the input. The gain is stabilized by on-chip compensation to vary less than ±0.2dB over the -40 to +85°C temperature range. The wide-dynamic-range receive mixer has a 10.9dB noise figure and an input IP3 of +2.8dBm at 2.45GHz. The nominal current drawn from a single 3V supply is 37mA in transmit mode and 22mA in receive mode. The SA2421 differs from the SA2420 only by removal of the Rx/Tx switch, thus making Rx and Tx available at all times.

FEATURES

- Low current consumption: 37mA nominal transmit mode and 22mA nominal receive mode
- Fabricated on a high volume, rugged BiCMOS technology
- High system power gain: 22.5dB (LNA + Mixer) at 2.45GHz
- TSSOP24 package
- Excellent gain stability versus temperature and supply voltage
- -10dBm LO input power can be used to drive the mixer
- Operates with either full or half frequency LO
- Wide IF range: 50–500MHz

PIN CONFIGURATION

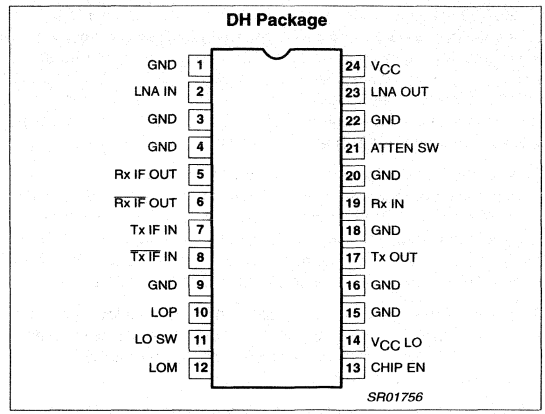


Figure 1. Pin Configuration

APPLICATIONS

- 2.45GHz WLAN front-end (802.11, ISM)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic Thin Shrink Small Outline Package (Surface-mount, TSSOP)	-40 to +85°C	SA2421DH	SOT355-1

BLOCK DIAGRAM

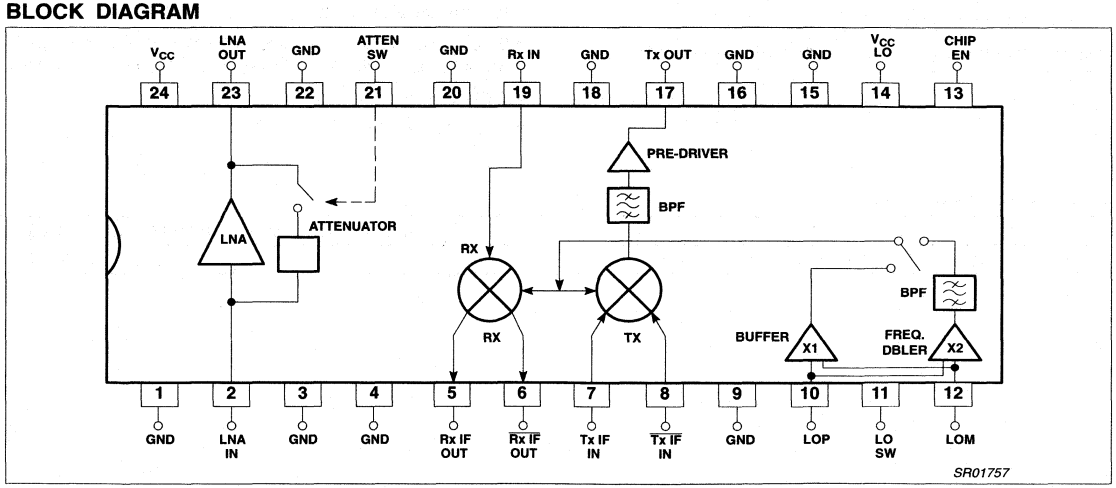


Figure 2. SA2421 Block Diagram

Low voltage mixer FM IF system with filter amplifier and data switch

SA639

DESCRIPTION

The SA639 is a low-voltage high performance monolithic FM IF system with high-speed RSSI incorporating a mixer/oscillator, two wideband limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), fast RSSI op amps, voltage regulator, wideband data output, post detection filter amplifier and data switch. The SA639 is available in 24-lead TSSOP (Thin shrink small outline package).

The SA639 was designed for high bandwidth portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The data output provides a minimum bandwidth of 1MHz to demodulate wideband data. The RSSI output is amplified and has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

The post-detection amplifier may be used to realize a low pass filter function. A programmable data switch routes a portion of the data signal to an external integration circuit that generates a data comparator reference voltage.

SA639 incorporates a power down mode which powers down the device when Pin 8 is high. Power down logic levels are CMOS and TTL compatible with high input impedance.

PIN CONFIGURATION

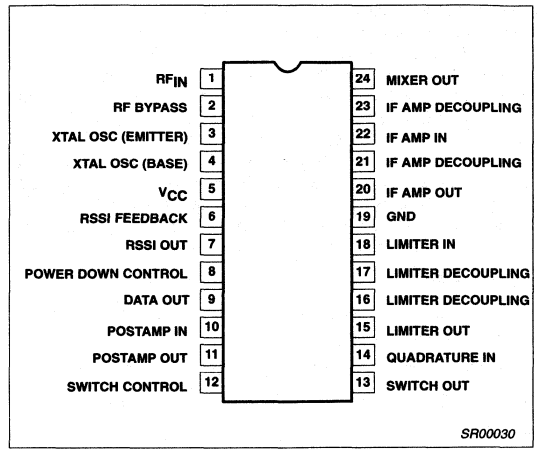


Figure 1. Pin Configuration

APPLICATIONS

- DECT (Digital European Cordless Telephone)
- FSK and ASK data receivers

FEATURES

- V_{CC} = 2.7 to 5.5V
- Low power consumption: 8.6mA typ at 3V
- Wideband data output (1MHz min.)
- Fast RSSI rise and fall times
- Mixer input to >500MHz
- Mixer conversion power gain of 9.2dB and noise figure of 11dB at 110MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 92dB of IF Amp/Limiter power gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 80dB
- RSSI output internal op amp
- Post detection amplifier for filtering
- Programmable data switch
- Excellent sensitivity: 2.24μV into 50Ω matching network for 10dB SNR (Signal to Noise Ratio) with RF at 110MHz and IF at 9.8MHz
- ESD hardened
- Power down mode

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic TSSOP (Thin Shrink Small Outline Package)	-40 to +85°C	SA639DH	SOT-355

BLOCK DIAGRAM

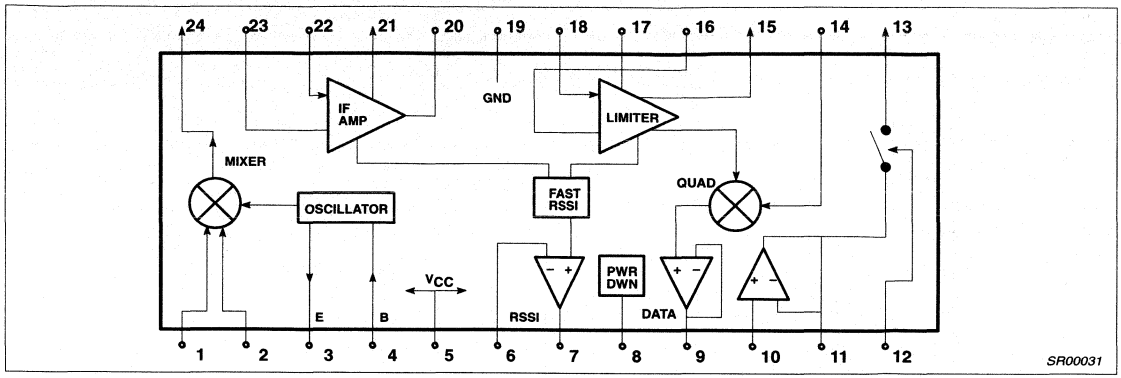
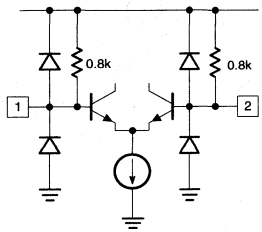
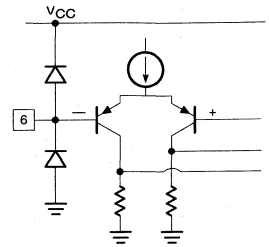


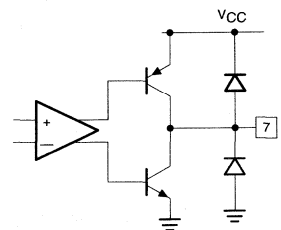
Figure 2. Block Diagram

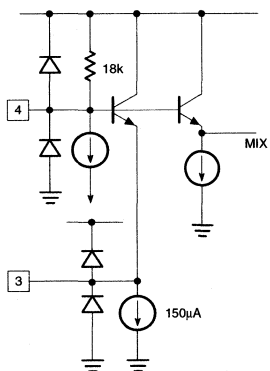
PIN FUNCTIONS All DC voltages measured with Pin 8 = Pin 12 = Pin 19 = 0V, Pin 5 = 3V and Pin 9 connected to Pin 10.

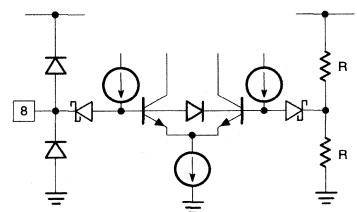
PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+1.07		6	RSSI FEEDBACK	+0.20	
2	RF BYPASS	+1.07		7	RSSI OUT	+0.20	
3	XTAL OSC	+1.57		8	POWER DOWN	0.00	
4	XTAL OSC	+2.32		9	DATA OUT	+1.7	
5	V_{CC}	+3.00		10	POST AMP IN	+1.70	

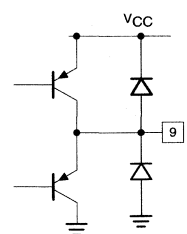


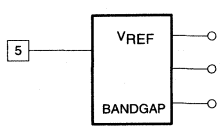


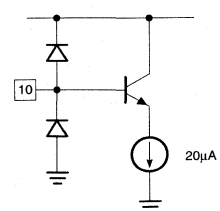








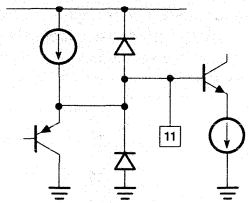
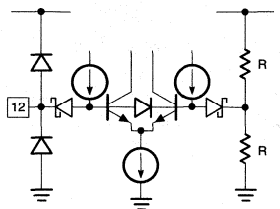
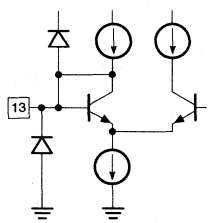
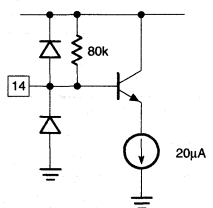
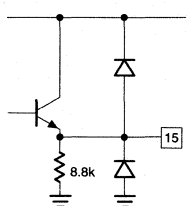
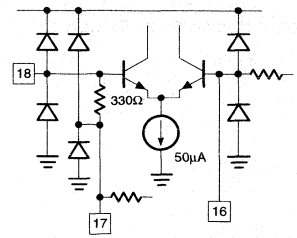
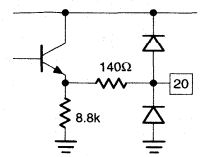
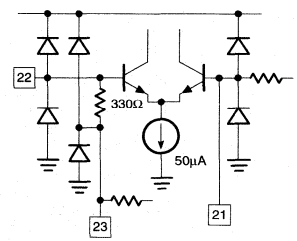
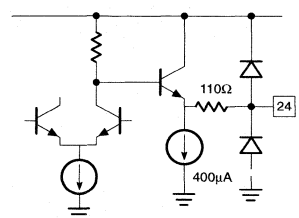




SR00032

Figure 3. Pin Functions

PIN FUNCTIONS (continued)

PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
11	POST AMP OUT	+1.70	
12	SWITCH CONTROL	0.00	
13	SWITCH OUT	+1.70	
14	QUAD IN	+3.00	
15	LIMITER OUT	+1.35	
16	LIMITER DECOUP	+1.23	
17	LIMITER COUPLING	+1.23	
18	LIMITER IN	+1.23	
19	GND	0	
20	IF AMP OUT	+1.22	
21	IF AMP DECOUP	+1.22	
22	IF AMP IN	+1.22	
23	IF AMP DECOUP	+1.22	
24	MIXER OUT	+1.03	

SR00033

Figure 4. Pin Functions (cont.)

1.3GHz low voltage fractional-N synthesizer SA7016

FEATURES

- Low phase noise
- Low power
- Fully programmable main divider
- Internal fractional spurious compensation
- Hardware and software power down

APPLICATIONS

- 500–1300 MHz wireless equipment
- Cellular phones
- Portable battery-powered radio equipment.

General description

The SA7016 BICMOS device integrates programmable dividers, charge pumps and a phase comparator to implement a phase-locked loop. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at VCO input frequencies up to 1.3 GHz. The synthesizer has fully programmable main and reference dividers. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DDCP} could be greater than or equal to V_{DD}.

The charge pump current (gain) is fixed by an external resistance at pin RSET (pin). Only passive loop filters are used; the charge-pump operates within a wide voltage compliance range to provide a wider tuning range.

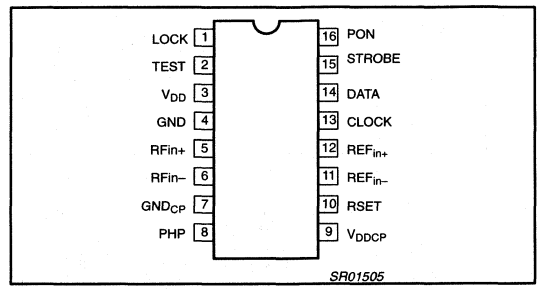


Figure 1. Pin Configuration

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	V_{DD}	2.7	–	5.5	V
V_{DDCP}	Analog supply voltage	$V_{DDCP} \geq V_{DD}$	2.7	–	5.5	V
$I_{DDCP}+I_{DD}$	Supply current		–	6.2	7.3	mA
$I_{DDCP}+I_{DD}$	Total supply current in power-down mode		–	1	–	µA
f_{VCO}	Input frequency		500	–	1300	MHz
f_{REF}	Crystal reference input frequency		10	–	40	MHz
f_{PC}	Maximum phase comparator frequency		–		4	MHz
T_{amb}	Operating ambient temperature		–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA7016	TSSOP16	Plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403–1

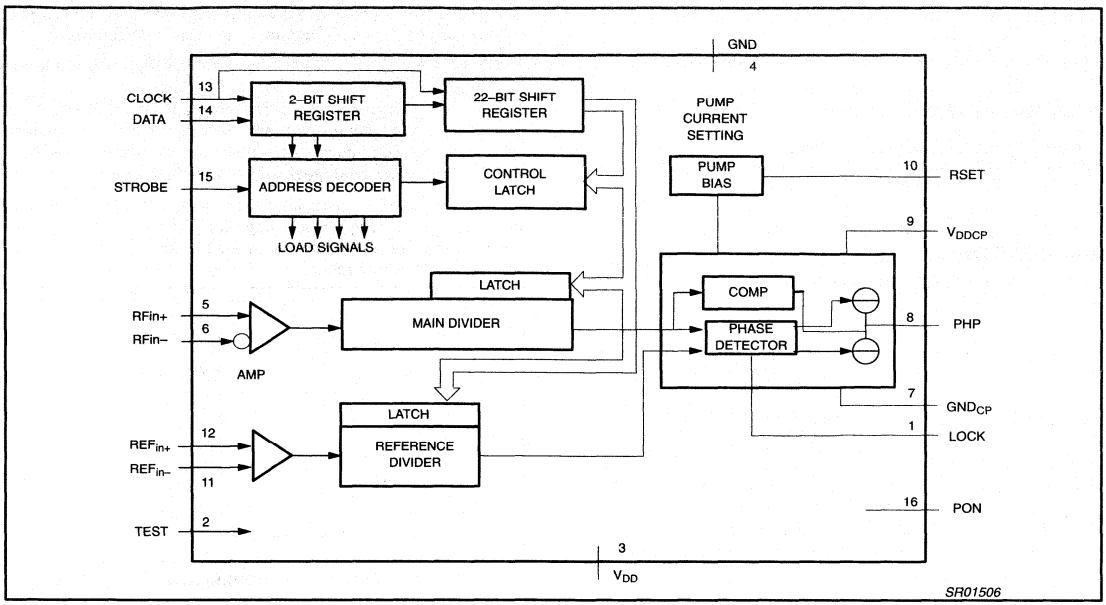


Figure 2. Block Diagram

PINNING

SYMBOL	PIN	DESCRIPTION
LOCK	1	Lock detect output
TEST	2	Test
V_{DD}	3	Digital supply
GND	4	Digital ground
RFin+	5	RF positive input to main divider
RFin–	6	RF negative input to main divider
GND_{CP}	7	Charge pump ground
PHP	8	Main NORMAL chargepump
V_{DDCP}	9	Charge pump supply voltage
RSET	10	External resistor from this pin to ground sets the chargepump current
REF_{in-}	11	Reference input
REF_{in+}	12	Reference input
CLOCK	13	Programming bus clock input
DATA	14	Programming bus data input
STROBE	15	Programming bus enable input
PON	16	Power down control

2.5GHz low voltage fractional-N synthesizer SA8016

FEATURES

- Low phase noise
- Low power
- Fully programmable main divider
- Internal fractional spurious compensation
- Hardware and software power down

APPLICATIONS

- 800–2500 MHz wireless equipment
- PCS
- Cellular phones
- WLAN
- Portable battery-powered radio equipment.

General description

The SA8016 BICMOS device integrates programmable dividers, charge pumps and a phase comparator to implement a phase-locked loop. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at VCO input frequencies up to 2.5 GHz. The synthesizer has fully programmable main and reference dividers. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DDCP} could be greater than or equal to V_{DD}.

The charge pump current (gain) is fixed by an external resistance at pin RSET (pin 10). Only passive loop filters are used; the charge-pump operates within a wide voltage compliance range to provide a wider tuning range.

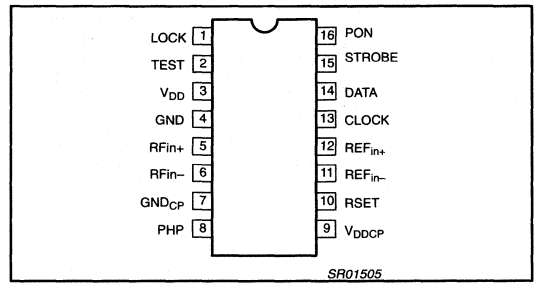


Figure 1. Pin Configuration

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	V_{DD}	2.7	–	5.5	V
V_{DDCP}	Analog supply voltage	$V_{DDCP} \geq V_{DD}$	2.7	–	5.5	V
$I_{DDCP}+I_{DD}$	Supply current		–	8.0	9.5	mA
$I_{DDCP}+I_{DD}$	Total supply current in power-down mode		–	1	–	µA
f_{VCO}	Input frequency		800	–	2500	MHz
f_{REF}	Crystal reference input frequency		10	–	40	MHz
f_{PC}	Maximum phase comparator frequency		–		4	MHz
T_{amb}	Operating ambient temperature		–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA8016	TSSOP16	Plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403–1

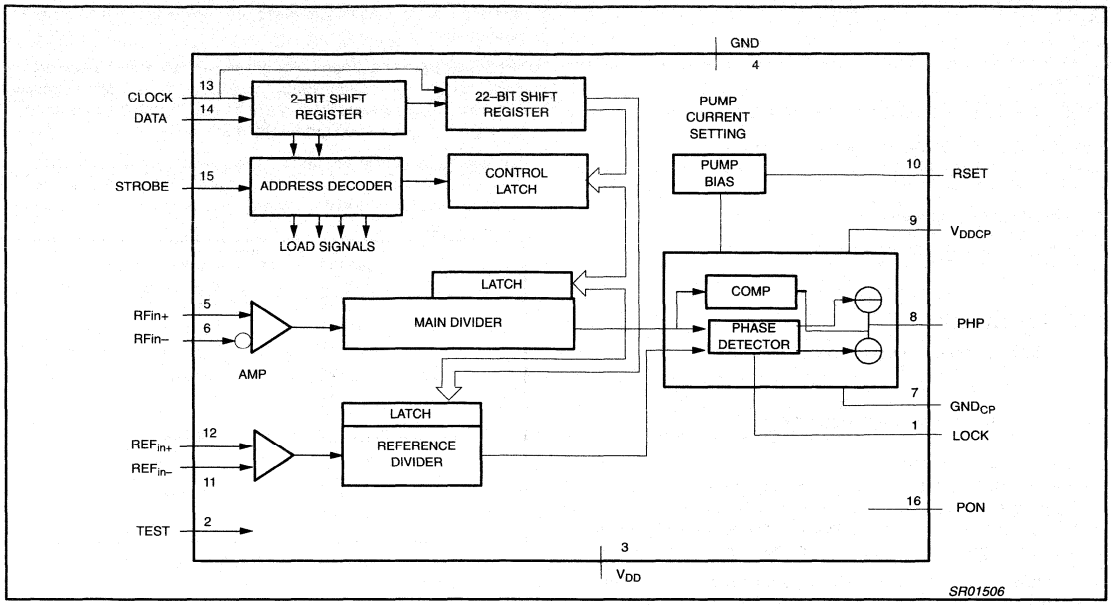


Figure 2. Block Diagram

PINNING

SYMBOL	PIN	DESCRIPTION
LOCK	1	Lock detect output
TEST	2	Test
V_{DD}	3	Digital supply
GND	4	Digital ground
RFin+	5	RF positive input to main divider
RFin–	6	RF negative input to main divider
GND_{CP}	7	Charge pump ground
PHP	8	Main NORMAL chargepump
V_{DDCP}	9	Charge pump supply voltage
RSET	10	External resistor from this pin to ground sets the chargepump current
REF_{in-}	11	Reference input
REF_{in+}	12	Reference input
CLOCK	13	Programming bus clock input
DATA	14	Programming bus data input
STROBE	15	Programming bus enable input
PON	16	Power down control

1.3GHz low voltage fractional-N dual synthesizer SA7026

FEATURES

- Low phase noise
- Low power
- Fully programmable main and auxiliary dividers
- NORMAL & INTEGRAL charge pumps outputs
- Fast Locking Adaptive mode design
- Internal fractional spurious compensation
- Hardware and software power down

APPLICATIONS

- 500–1300 MHz wireless equipment
- Cellular phones
- Portable battery-powered radio equipment.

General description

The SA7026 BICMOS device integrates programmable dividers, charge pumps and a phase comparator to implement a phase-locked loop. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at VCO input frequencies up to 1.3 GHz. The synthesizer has fully programmable main, auxiliary and reference dividers. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DDCP} could be greater than or equal to V_{DD}.

The charge pump current (gain) is fixed by an external resistance at pin RSET (pin). Only passive loop filters are used; the charge-pump operates within a wide voltage compliance range to provide a wider tuning range.

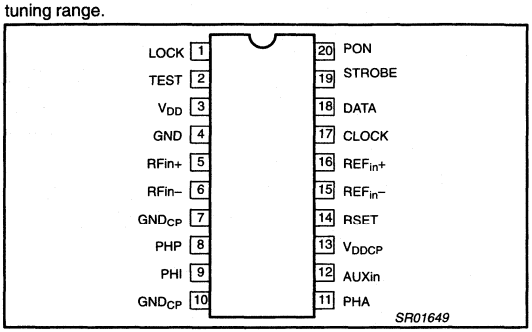


Figure 1. Pin Configuration

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	V_{DD}	2.7	–	5.5	V
V_{DDCP}	Analog supply voltage	$V_{DDCP} \geq V_{DD}$	2.7	–	5.5	V
$I_{DDCP}+I_{DD}$	Supply current	Main and Aux. on	–	7.5	8.8	mA
$I_{DDCP}+I_{DD}$	Total supply current in power-down mode		–	1	–	µA
f_{VCO}	Input frequency		500	–	1300	MHz
f_{AUX}	Input frequency		10	–	550	MHz
f_{REF}	Crystal reference input frequency		10	–	40	MHz
f_{PC}	Maximum phase comparator frequency		–		4	MHz
T_{amb}	Operating ambient temperature		–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA7026DK	TSSOP20	Plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360–1

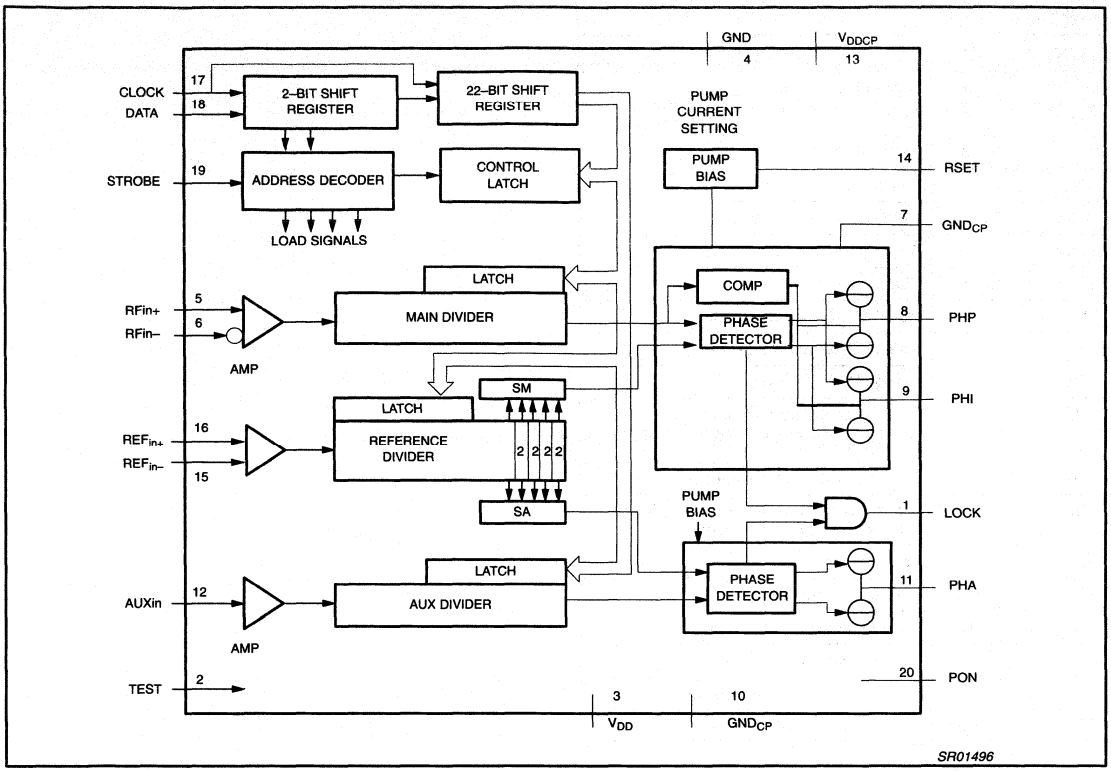


Figure 2. Block Diagram

PINNING

SYMBOL	PIN	DESCRIPTION
LOCK	1	Lock detect output
TEST	2	Test
V_{DD}	3	Digital supply
GND	4	Digital ground
RFin+	5	RF positive input to main divider
RFin–	6	RF negative input to main divider
GND_{CP}	7	Charge pump ground
PHP	8	Main NORMAL chargepump
PHI	9	Main INTEGRAL chargepump
GND_{CP}	10	Charge Pump Ground
PHA	11	Auxiliary chargepump output
AUXin	12	Input to auxiliary divider
V_{DDCP}	13	Charge pump supply voltage
RSET	14	External resistor from this pin to ground sets the chargepump current
REF_{in-}	15	Reference input
REF_{in+}	16	Reference input
CLOCK	17	Programming bus clock input
DATA	18	Programming bus data input
STROBE	19	Programming bus enable input
PON	20	Power down control

2.5GHz low voltage fractional–N dual synthesizer SA8026

FEATURES

- Low phase noise
- Low power
- Fully programmable main and auxiliary dividers
- NORMAL & INTEGRAL charge pumps outputs
- Fast Locking Adaptive mode design
- Internal fractional spurious compensation
- Hardware and software power down

APPLICATIONS

- 800 to 2500 MHz wireless equipment
- PCS
- Cellular phones
- WLAN
- Portable battery-powered radio equipment.

General description

The SA8026 BICMOS device integrates programmable dividers, charge pumps and a phase comparator to implement a phase-locked loop. The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at VCO input frequencies up to 2.5 GHz. The synthesizer has fully programmable main, auxiliary and reference dividers. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DDCP} could be greater than or equal to V_{DD} .

The charge pump current (gain) is fixed by an external resistance at pin RSET (pin). Only passive loop filters are used; the charge-pump operates within a wide voltage compliance range to provide a wider tuning range.

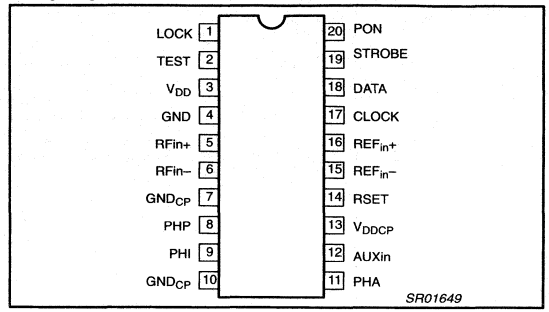


Figure 1. Pin Configuration

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage	V_{DD}	2.7	–	5.5	V
V_{DDCP}	Analog supply voltage	$V_{DDCP} \geq V_{DD}$	2.7	–	5.5	V
$I_{DDCP}+I_{DD}$	Supply current	Main and Aux. on	–	10.0	11.8	mA
$I_{DDCP}+I_{DD}$	Total supply current in power-down mode		–	1	–	µA
f_{VCO}	Input frequency		800	–	2500	MHz
f_{AUX}	Input frequency		10	–	550	MHz
f_{REF}	Crystal reference input frequency		10	–	40	MHz
f_{PC}	Maximum phase comparator frequency		–		4	MHz
T_{amb}	Operating ambient temperature		–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SA8026DH	TSSOP20	Plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360–1

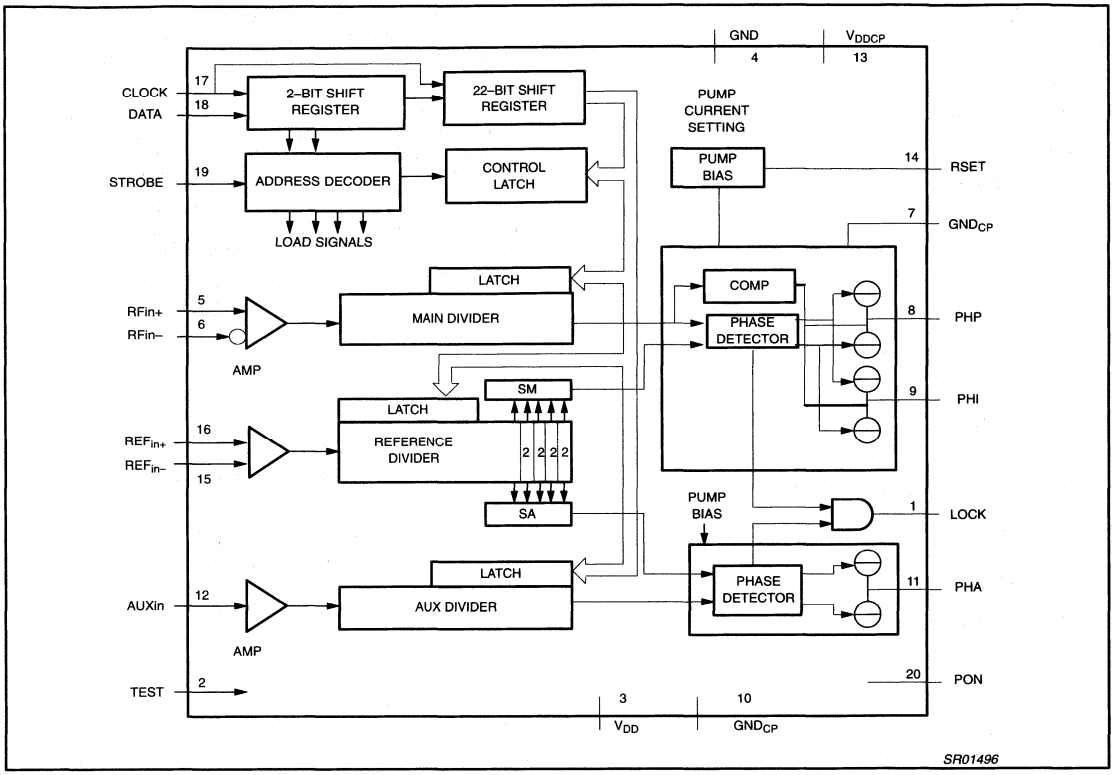


Figure 2. Block Diagram

PINNING

SYMBOL	PIN	DESCRIPTION
LOCK	1	Lock detect output
TEST	2	Test
V_{DD}	3	Digital supply
GND	4	Digital ground
RFin+	5	RF positive input to main divider
RFin–	6	RF negative input to main divider
GND_{CP}	7	Charge pump ground
PHP	8	Main NORMAL chargepump
PHI	9	Main INTEGRAL chargepump
GND_{CP}	10	Charge Pump Ground
PHA	11	Auxiliary chargepump output
AUXin	12	Input to auxiliary divider
V_{DDCP}	13	Charge pump supply voltage
RSET	14	External resistor from this pin to ground sets the chargepump current
REF_{in-}	15	Reference input
REF_{in+}	16	Reference input
CLOCK	17	Programming bus clock input
DATA	18	Programming bus data input
STROBE	19	Programming bus enable input
PON	20	Power down control

Low-voltage frequency synthesizer for radio telephones

UMA1021M

FEATURES

- Low phase noise
- Low current from 3 V supply
- Fully programmable main divider
- 3-line serial interface bus
- Independent fully programmable reference divider, driven from external crystal oscillator
- Dual charge pump outputs
- Hard and soft power-down control.

APPLICATIONS

- 900 MHz and 2 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1021M BICMOS device integrates a prescaler, programmable dividers, and a phase comparator to implement a phase-locked loop.

The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at RF input frequencies up to 2.2 GHz, with a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog (charge-pump) and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential (V_{DD}). V_{CC} must be equal to or greater than V_{DD} (e.g. V_{DD} = 3 V and V_{CC} = 5 V for wider VCO control voltage range).

The phase detector has two charge-pump outputs, CP and CPF, the latter of which is enabled directly at pin FAST. This permits the design of adaptive loops. The charge pump currents (phase detector gain) are fixed by an external resistance at pin I_{SET} and via the serial interface. Only a passive loop filter is necessary; the charge pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$; $V_{CC} \geq V_{DD}$	2.7	–	5.5	V
V_{CC}	charge-pump supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{DD} + I_{CC}$	supply current		–	10	–	mA
$I_{CC(pd)} + I_{DD(pd)}$	total supply current in power-down mode		–	5	–	µA
f_{RF}	RF input frequency		300	–	2200	MHz
f_{xtal}	crystal reference input frequency		3	–	35	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1021M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

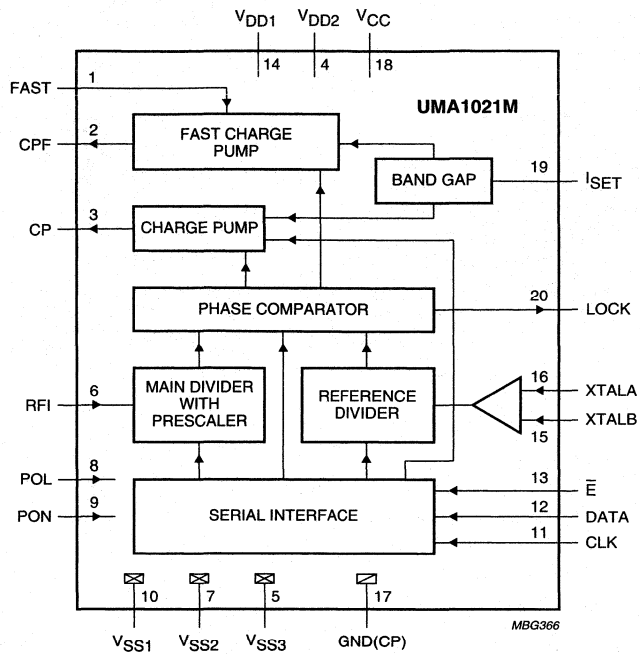


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	enable input for fast charge-pump output CPF
CPF	2	fast charge-pump output
CP	3	normal charge-pump output
V_{DD2}	4	power supply 2
V_{SS3}	5	ground 3
RFI	6	2 GHz main divider input
V_{SS2}	7	ground 2
POL	8	digital input to select polarity of power-on inputs (PON and sPON): POL = 0 for active LOW and POL = 1 for active HIGH
PON	9	power-on input
V_{SS1}	10	ground 1
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\overline{E}$	13	programming bus enable input
V_{DD1}	14	power supply 1
XTALB	15	complementary crystal frequency input from TCXO; if not used should be decoupled to ground
XTALA	16	crystal frequency input from TCXO; if not used should be decoupled to ground
GND(CP)	17	ground for charge-pump
V_{CC}	18	supply for charge-pump
I_{SET}	19	external resistor from this pin to ground sets the charge-pump currents
LOCK	20	out-of-lock detector output

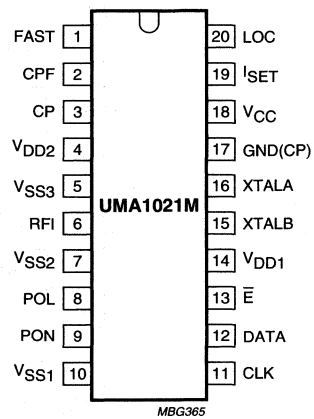


Fig.2 Pin configuration.

Low cost dual frequency synthesizer for radio telephones

UMA1022M

FEATURES

- Low phase noise
- Low current from 3 V supply
- Fully programmable dividers
- 3-line serial interface bus
- Input reference buffer configurable as an oscillator with external crystal resonator
- Wide compliance voltage charge pump outputs
- Two power-down input control pins.

APPLICATIONS

- 900 MHz and 2 GHz digital radio telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1022M BICMOS device integrates prescalers, programmable dividers, a crystal oscillator/buffer and phase comparators to implement two phase-locked loops. The device is designed to operate from 3 NiCd or a single LiIon cell in pocket phones, or from an external 3 V supply.

The synthesizers operate at RF input frequencies up to 2.1 GHz and 550 MHz. All divider ratios are supplied via a 3-wire serial programming bus. The reference divider uses a common, fully programmable part and a separate subdivider section. In this way the comparison frequencies are related to each other allowing optimum isolation between charge pump pulses.

Separate power and ground pins are provided to the analog (charge pump, prescaler) and digital (CMOS) circuits. An independent supply for the crystal oscillator section allows maximum frequency stability. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD} and V_{DDX} must be at the same potential. V_{CCA} and V_{CCB} must be equal to each other and equal to or greater than V_{DD} (e.g. V_{DD} = 3 V and V_{CCA} = 4 V for wider VCO control voltage range).

The charge pump currents (phase detector gain) are fixed by internal resistances and controlled by the serial interface. Only passive loop filters are necessary; the charge pumps function within a wide voltage compliance range to improve the overall system performance.

Suitable pin layout is chosen to minimize coupling and interference between signals entering or leaving the chip.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1022M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

Low cost dual frequency synthesizer for radio telephones

UMA1022M

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage	$V_{CCA} = V_{CCB} \geq V_{DD}$	2.7	3.0	4.0	V
V_{CCA}, V_{CCB}	analog supply voltages	$V_{CCA} = V_{CCB} \geq V_{DD}$	2.7	3.0	4.0	V
V_{DDX}	crystal reference supply voltage	$V_{DDX} = V_{DD}$	2.7	3.0	4.0	V
I_{tot}	all supply currents ($I_{DD} + I_{CCA} + I_{CCB} + I_{DDX}$) in active mode	$\overline{E} = 1$; $V_{CCA} = V_{CCB} = 3.0$ V; $V_{DDX} = V_{DD} = 3.0$ V;				
		XON = 0	–	14.65	–	mA
		XON = 1	–	15.9	–	mA
$I_{tot(pd)}$	total supply currents in power-down mode		–	40	–	µA
f_{RF}	RF input frequency		300	–	2100	MHz
f_{IF}	IF input frequency		50	–	550	MHz
f_{xtal}	crystal reference oscillator frequency		3	–	25	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

BLOCK DIAGRAM

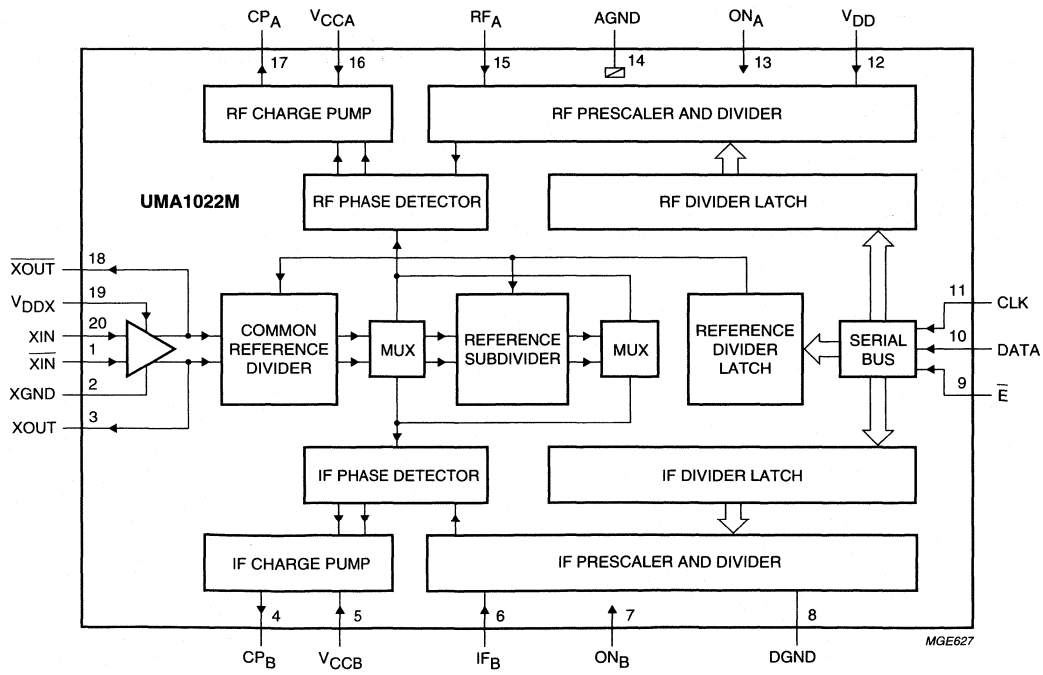


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{XIN}$	1	inverting crystal reference input
XGND	2	ground for crystal oscillator circuits
XOUT	3	crystal oscillator buffer output
CP_B	4	IF synthesizer charge pump output
V_{CCB}	5	analog supply to IF synthesizer
IF_B	6	IF VCO main divider input
ON_B	7	IF power-on input; ON_B = HIGH means IF synthesizer is active
DGND	8	digital circuits ground
$\overline{E}$	9	programming bus enable input
DATA	10	programming bus data input
CLK	11	programming bus clock input
V_{DD}	12	digital circuits supply voltage
ON_A	13	RF power-on input; ON_A = HIGH means RF synthesizer is active
AGND	14	analog circuits ground
RF_A	15	RF VCO main divider input
V_{CCA}	16	analog supply to RF synthesizer
CP_A	17	RF synthesizer charge pump output
$\overline{XOUT}$	18	inverting oscillator buffer output
V_{DDX}	19	supply voltage to crystal oscillator circuits
XIN	20	non-inverting crystal reference input

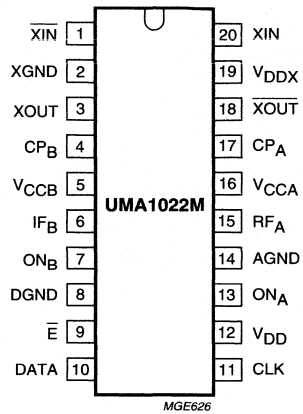


Fig.2 Pin configuration.

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SCN2681/SCN68681 and SCC2691 data communications — AN405

Note: The coding and flow charts will apply to all Philips UARTs. The reader will note most register names and bit assignments are the same through the product line. Principle differences in the several Philips UARTs will be found in the structures and control of input, output and I/O pins.

This SCN2681/SCN68681 and SCC2691 data communications applications note contains answers to some of the most frequently discussed user inquiries. There are three main sections: functions that are common to all three; functions that are unique to the SCN2681/SCN68681; and a typical SCC2691 application using the musical instrument digital interface (MIDI).

SCC2698B Octal universal asynchronous receiver/transmitter (Octal-UART) — AN410B

Note: This note is directed at the SC2698B. However its general coding and flow charts will apply to all Philips UARTs. The reader will note most register names and bit assignments are the same through the product line. Principle differences in the several Philips UARTs will be found in the structures and control of input, output and I/O pins.

The Philips Semiconductors SCC2698B Octal UART is composed of four blocks, each logically equivalent to a 2681 or 2692 DUART. Each block is composed of two channels, a counter/timer, and an

interrupt control section. The channels are matched to the blocks as shown in Figure 1. The blocks are indicated by capital letters A, B, C, and D; the channels are indicated by lower–case letters a, b, c, d, e, f, g, and h. All registers act either on a block or an individual channel.

SCC2692 differences from the SCN2681 — AN414

This application note discusses how to use the on–chip oscillator circuitry for the Philips Semiconductors UART and DUSCC/DMSC families of data communications devices; the SCC2691, SCC2692, SCN68681, SCN26562, SCN68562, SCN26542 and SCN68542.

SCC68692 differences from the SCN68681 AN415

The SCC68692 is a CMOS version of the SCN68681 DUART. The SCC68692 is functionally and pin–to–pin compatible with the SCN68681 and can be substituted into existing SCN68681 designs. There are a few additional features and differences in the SCC68692 which are discussed below.

All of the functional descriptions (except the oscillator pins and counter timer) apply to the SCC2692, SCC68692, SC26C92, and SC28L92.

SCC2698A differences from the SCC2698B AN421

The SCC2698B Octal UART is an enhanced version of the SCC2698A. This note discusses differences between the original A and the newer B version. It therefore subtitle operational characteristics of the 2698B that will be of value to users of the SC2698B. The B revision has been in production since 1990.

Extended baud rates for SCN2681, SCN68681, SCC2691, SCC2692, SCC68681 and SCC2698B

The Philips Semiconductors UART chips (EXCEPTING the SC26C94) all have two test modes which are accessed via a READ of the reserved registers at hex address 2 and A. Each time a read of either address is performed, a flip-flop at that address will toggle. Software must keep track of the state of these flop-flops since there is no internal indication of the sate of these flop-flops. They are reset to the non-test condition by a hardware reset of the chip. Other methods for resetting are described in the full version included on the CD-ROM.

Functional description of Philips arbitrating interrupt systems

This article is a brief description of Philips arbitrating interrupt systems. Bit alignments, interrupt type identification, and interrupt vector modification is explained.

Hardware and software verification procedure AN462

This procedure is suggested to verify the signal, bus, power connections and timing between the host (control processor), UART and printed circuit board. The following procedures may be executed and the results evaluated without recourse to any exotic test equipment (logic or protocol analyzers, oscilloscopes, etc). The assumption on which this is based requires that the processor must be able to read data from and write data to the UART and have some means of presenting those results to the human operator. If one can not be absolutely certain that simple reads and writes are properly executed then any other means of evaluating the UART connections will be suspicious.

Using the datacomm product's on-chip oscillator AN413

This application note discusses how to use the on-chip oscillator circuitry for the Philips Semiconductors UART and DUSCC families of data communications devices; the SCC2691, SCC2692, SCN68681, SCN26562, SCN68562.

User notes for the SCN68/26562 (NDUSCC) and SC68/26C562 (CDUSCC) — AN416

Questions and answers for some of the several operational modes of the DUSCC and CDUSCC. "Verbal" descriptions of register configurations are presented along with tested assembly code.

DUSCC initialization procedures — AN419

The Philips Semiconductors Dual Universal Serial Communications Controller (DUSCC) has forty–eight programmable registers, many of which have triple functions that vary with the protocol selected. This application note contains basic initialization instructions and examples Including: description of the input clock circuit; how to use interrupts with status; how to use the digital phase locked loop (DPLL); how to initialize the counter/timer as a system down counter and as a receive character counter. Also included are software examples for the asynchronous local loop back mode, for two synchronous modes (HDLC and BISYNC), and DMA handling.

Electrostatic discharge protection for the NE83Q92 or NE83C92 Ethernet transceiver — AN4004

This application brief describes techniques which may be used to prevent damage to the NE83Q92A under certain electrical overstress (EOS) test and environmental conditions. In particular reference is made to the test conditions specified by the International Electrotechnical Commission under the IEC 801-2 guideline. Two different types of external protection devices are discussed as alternate solutions to the potential problem of internal device damage as it applies to the use of the Philips NE83Q92A in an Ethernet environment. A third alternative, robust PC board design using electrostatic principles, is mentioned briefly.

50Mb/s fiber optic receivers — AB1432

This application brief describes the use of four Philips Semiconductors devices specifically designed for use as fiber optic receiver components.

SA5223—SONET applications note — AN1431

The SA5223 is a wideband variable gain transimpedance amplifier fabricated in Philips 1μm "QUBiC" BiCMOS technology. The device is primarily intended for Synchronous Optical Network (SONET) / (OC3) or the International Telecommunications Union, (ITU) Synchronous Transmission Module (STM) applications using NRZ or RZ data format at 155MB/s. The SA5223 has a spectral noise current density of 1.2pA/√Hz with an electrical dynamic range of 105dB. A Bit Error Rate (BER) of 10^{-10} is obtainable for an optical input level of -36dBmW_{AVG}.

A phase locked fiber optic system using FM modulation — AN1434

The purpose of the fiber link is to transmit broadband video and sound over moderate distances (2.5km) with existing low cost components and minimal complexity.

A family of wideband low noise transimpedance amplifiers — AN1435

Despite numerous advantages, the relatively high cost of fiber optic transmission prevented its wide-spread industrial acceptance. High bandwidth-distance products, a prerequisite for cost-effectiveness, could not be achieved with relatively inexpensive components. The latest technological advances on both transmitter and receiver sides, however, are about to change that.

Low cost, TTL fiber optic receivers for up to 100Mb/s NRZ — AN1443

This application note describes circuits belonging to the receiver part of the Philips Semiconductors HiFI-100 (High-performance Fiber-optic Interface) Fiber Optic Chip Set. It should be noted that the performance of each board reflects the capabilities of the system along with its external components and does not represent the maximum capabilities of the individual Integrated Circuits. Performance may vary depending on layout and/or external component values.

Fiber optic receiver applications note — AN4003

Describes the use, design, equations, practice, and PC board layout of Philips 100 Mb/s FDDI (Fiber Distributed Data Interface) devices.
Design cautions and test evaluations are discussed.

An FM/IF system for DECT and other high speed GFSK applications — AN1998

A Philips low voltage high performance monolithic FM/IF system, the SA639 is introduced to meet the increasing demand for high speed digital wireless PCS applications. In order to assist the system design, a SA639-based performance evaluation board has been developed according to the Digital European Cordless Telephone (DECT) specifications. This application note presents a detailed description of the SA639 FM/IF system, the evaluation board, and design information including circuit diagram, component list, and the board layout. The experimental performance evaluation procedures, measured bit error rate (BER), sensitivity to frequency off-set, and sensitivity to FM deviation variation of this system are also presented. Results indicate that the low voltage SA639 FM/IF system provides superior performance for high speed digital wireless applications.

UMA1021M low voltage frequency synthesizer — AN96083

The UMA1021M is a low noise, low power 2.2 GHz single synthesizer. It is intended for radio communication systems like GSM, DCS1800, PCS1900, DECT, PHS, DAMPS, ...where good noise performance and fast switching time are required.

A close in noise value of –90 dBc/Hz has been measured in the loop bandwidth of a typical GSM application.

OM5803 Transimpedance amplifier demoboard for 155/622/1250 Mbps — AN98081

A demoboard for 3 types of transimpedance amplifiers is described. The transimpedance amplifiers are TZA3033 (155 Mbps), TZA3023 (622 Mbps) and TZA3043 (1250 Mbps). The type number of the board is OM5803. Application information includes schematics and layouts.

OM5804 Receiver demoboard for 155/622/1250 Mbps — AN98082

A demoboard for 3 types of transimpedance amplifiers/limiting amplifier combinations is described. The transimpedance amplifiers/limiting amplifiers are TZA3033/TZA3034 (155 Mbps), TZA3023/TZA3024 (622 Mbps) and TZA3043/TZA3044 (1250 Mbps). The type number of the board is OM5804. Applications information includes schematics and layouts.

SA8025 Fractional-N synthesizer for 2GHz band applications — AN1891

The SA8025 is a 3V, 1.8GHz, SSOP 20-pin packaged fractional-N phase locked-loop (PLL) frequency synthesizer. It is targeted for systems like the Japan Personal Handy Phone System (PHS, formerly PHP) which demands fast switching time and good noise performance. Built on the QUBiC BiCMOS process, it has phase detectors with maximum frequency of 5MHz and an auxiliary synthesizer that can operate up to 150MHz. This design was based on the UMA1005 (all CMOS), an earlier version fractional-N synthesizer which requires an external prescaler for 1 and 2GHz applications. There is also a 1GHz version fractional-N PLL frequency synthesizer, the SA7025, available for systems operating under 1GHz. One should expect the performance of the SA8025 and SA7025 to be comparable to the UMA1005 with an extra prescaler. This application note will serve as a supplement to the application note for the UMA1005 (Report No: SCO/AN92002) or as a stand-alone document specifically for the SA8025.

Section 10
Package Outlines

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INTRODUCTION

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when though-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

THROUGH-HOLE MOUNTED PACKAGES

Table 1. Types of through-hole mounted packages

TYPE	DESCRIPTION
DIP	plastic dual in-line package
SDIP	plastic shrink dual in-line package
HDIP	plastic heat-dissipating dual in-line package
DBS	plastic dual in-line bent from a single in-line package
SIL	plastic single in-line package

Soldering by dipping or wave

The maximum permissible temperature of the solder is 260°C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24V) to the lead(s) of the package, below the seating plane or not more than 2mm above it. If the temperature of the soldering iron bit is less than 300°C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400°C, contact may be up to 5 seconds.

SURFACE MOUNTED PACKAGES

Table 2. Types of surface mounted packages

TYPE	DESCRIPTION
SO	plastic small outline package
SSOP	plastic shrink small outline package
TSSOP	plastic thin shrink small outline package
VSO	plastic very small outline package
QFP	plastic quad flat package
LQFP	plastic low profile quad flat package
SQFP	plastic shrink quad flat package
TQFP	plastic thin quad flat package
PLCC	plastic leaded chip carrier

Reflow soldering

Reflow soldering techniques are suitable for all SMD packages, ease of soldering varies with the type of package as indicated in Table 3.

The choice of heating method may be indluenced by larger plastic packages (QFP or PLCC with 44 leads, or more). If infrared or vapor phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information on moisture prevention, refer to the Drypack chapter in our *"Quality Reference Manual"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250°C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45°C.

Table 3. Suitability of surface mounted packages for various soldering methods

Rating from 'a' to 'd': **'a' indicates most suitable** (soldering is not difficult); **'d' indicates least suitable** (soldering is achievable with difficulty).

TYPE	REFLOW METHOD					DOUBLE WAVE METHOD
	INFRARED	HOT BELT	HOT GAS	VAPOR PHASE	RESISTANCE	
SO	a	a	a	a	d	a
SSOP	a	a	a	c	d	c
TSSOP	b	b	b	c	d	d
VSO	b	b	a	b	a	b
QFP	b	b	a	c	a	c
LQFP	b	b	a	c	d	d
SQFP	b	b	a	c	d	d
TQFP	b	b	a	c	d	d
PLCC	c	b	b	d	d	b

Wave soldering

Wave soldering is **not** recommended for SSOP, TSSOP, QFP, LQFP, SQFP or TQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- For SSOP, TSSOP and VSO packages, the longitudinal axis of the package footprint must be parallel to the solder flow **and** must incorporate solder theives at the downstream end.
- For QFP, LQFP and TQFP packages, the footprint must be at and angle of 45° to the board direction **and** must incorporate solder thieves downstream and at the side corners.

Even with these conditions, only consider wave soldering for the following package types:

- SO
- VSO
- PLCC
- SSOP **only with body width 4.4mm**, e.g., SSOP16 (SOT369-1) or SSOP20 (SOT266-1).
- QFP **except** QFP52 (SOT379-1), QFP100 (SOT317-1, SOT317-2 and SOT382-1) and QFP160 (SOT322-1); these are **not** suitable for wave soldering.
- LQFP **except** LQFP32 (SOT401-1), LQFP48 (SOT313-1, SOT313-2), LQFP64 (SOT314-2), LQFP80 (SOT315-1); these are **not** suitable for wave soldering.
- TQFP **except** TQFP64 (SOT357-1), TQFP80 (SOT375-1) and TQFP100 (SOT386-1); these are **not** suitable for wave soldering.

SQFP are **not** suitable for wave soldering.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260°C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150°C within 6 seconds. Typical dwell time is 4 seconds at 250°C.

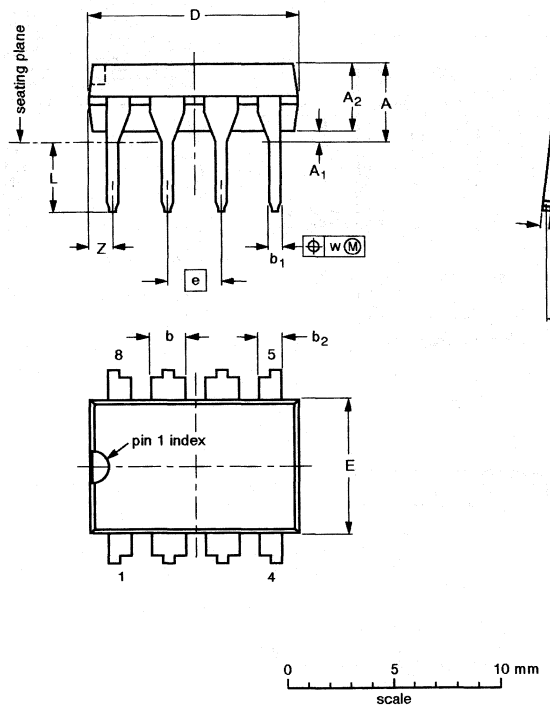
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300°C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320°C.

Package outlines

DIP8: plastic dual in-line package; 8 leads (300 mil) SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

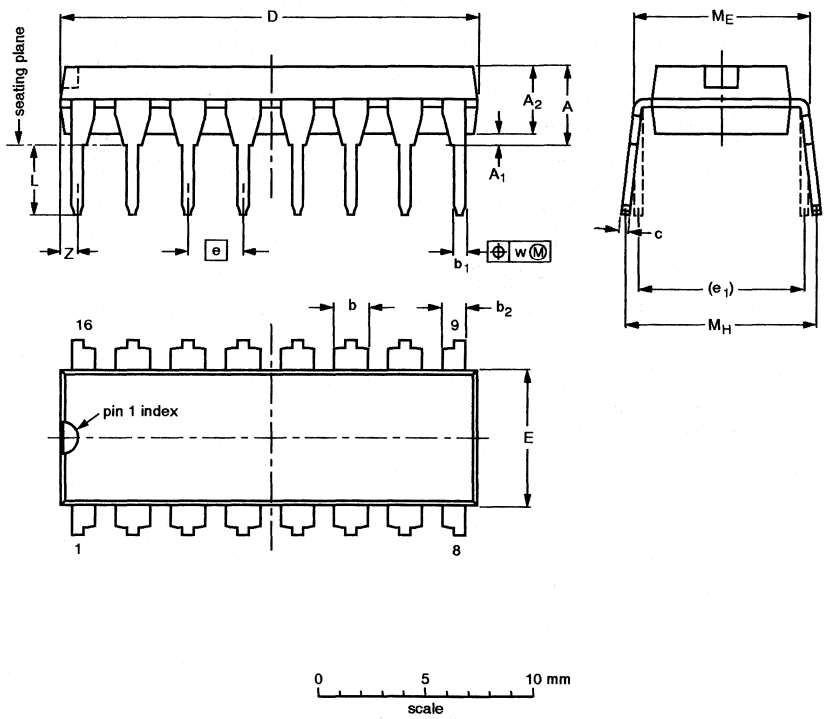
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

Package outlines

DIP16: plastic dual in-line package; 16 leads (300 mil) SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

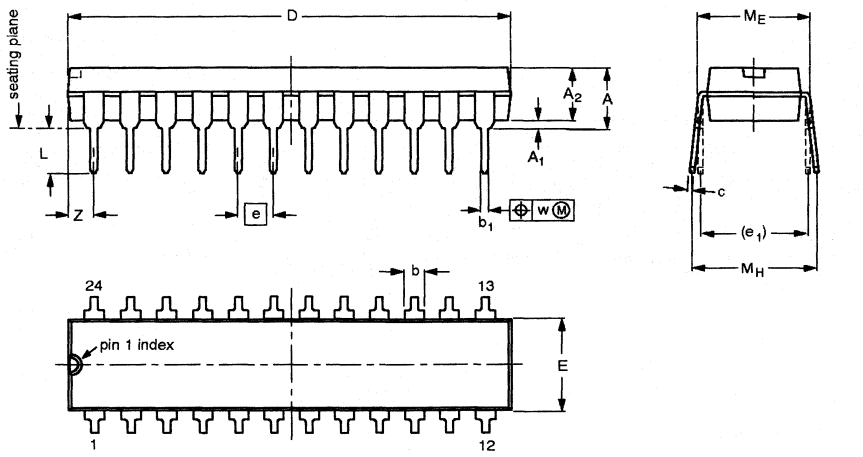
Note

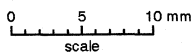
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

Package outlines

DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

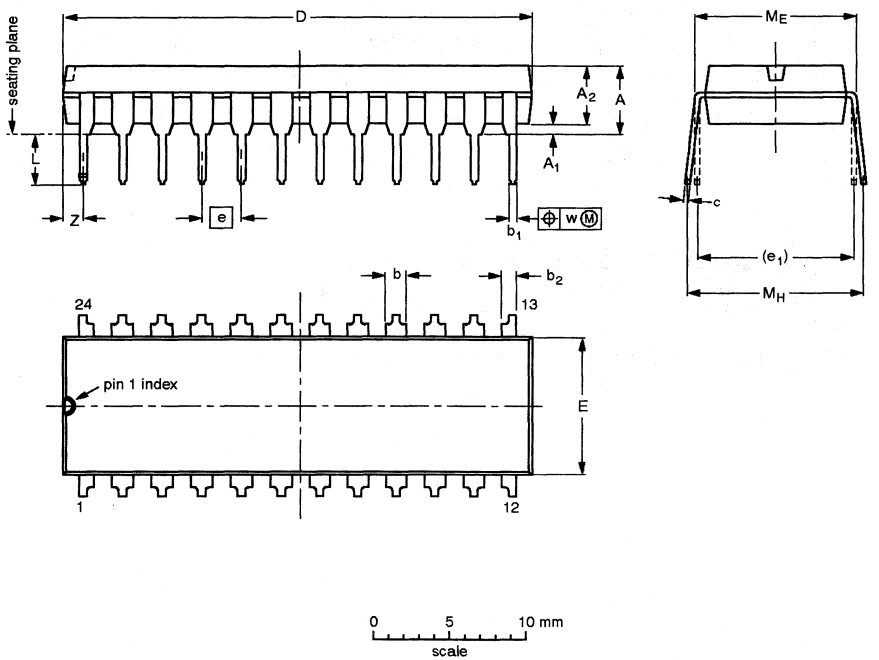
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

Package outlines

DIP24: plastic dual in-line package; 24 leads (400 mil) SOT248-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.83	0.51	3.94	1.63 1.14	0.56 0.43	1.07 0.86	0.36 0.25	30.61 30.23	9.40 8.76	2.54	10.16	3.51 3.05	10.72 10.16	12.57 10.16	0.25	1.40
inches	0.190	0.020	0.155	0.064 0.045	0.022 0.017	0.042 0.034	0.014 0.010	1.205 1.190	0.370 0.345	0.100	0.400	0.138 0.120	0.422 0.400	0.495 0.400	0.01	0.055

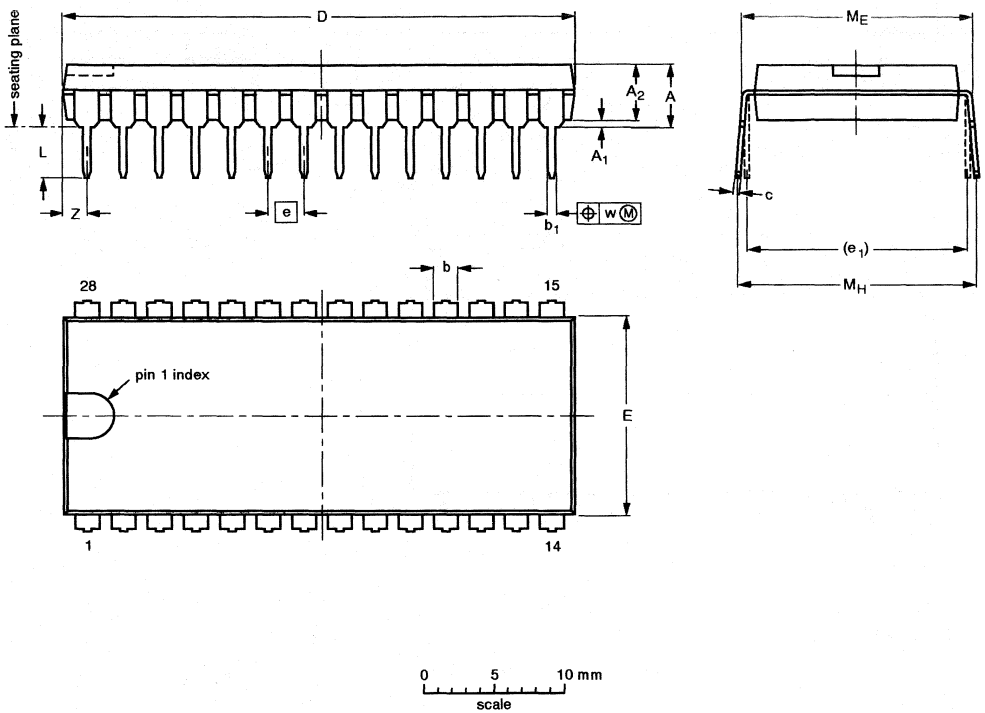
Note

1. Plastic or metal protrusions of 0.01 inch maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT248-1						95-03-11

Package outlines

DIP28: plastic dual in-line package; 28 leads (600 mil) SOT117-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

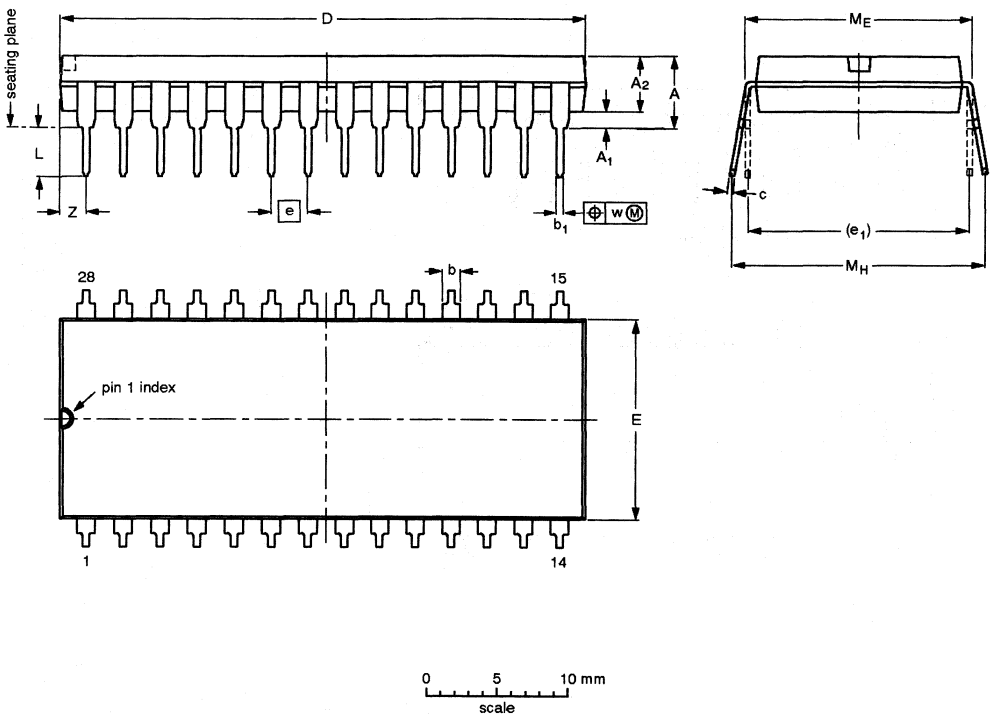
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

Package outlines

DIP28: plastic dual in-line package; 28 leads (600 mil); long body — SOT117-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	3.94	1.63 1.14	0.56 0.43	0.38 0.25	37.08 35.94	14.22 13.84	2.54	15.24	3.51 3.05	15.75 15.24	17.65 15.24	0.25	2.10
inches	0.200	0.020	0.155	0.064 0.045	0.022 0.017	0.015 0.010	1.460 1.415	0.560 0.545	0.100	0.600	0.138 0.120	0.62 0.60	0.695 0.600	0.01	0.083

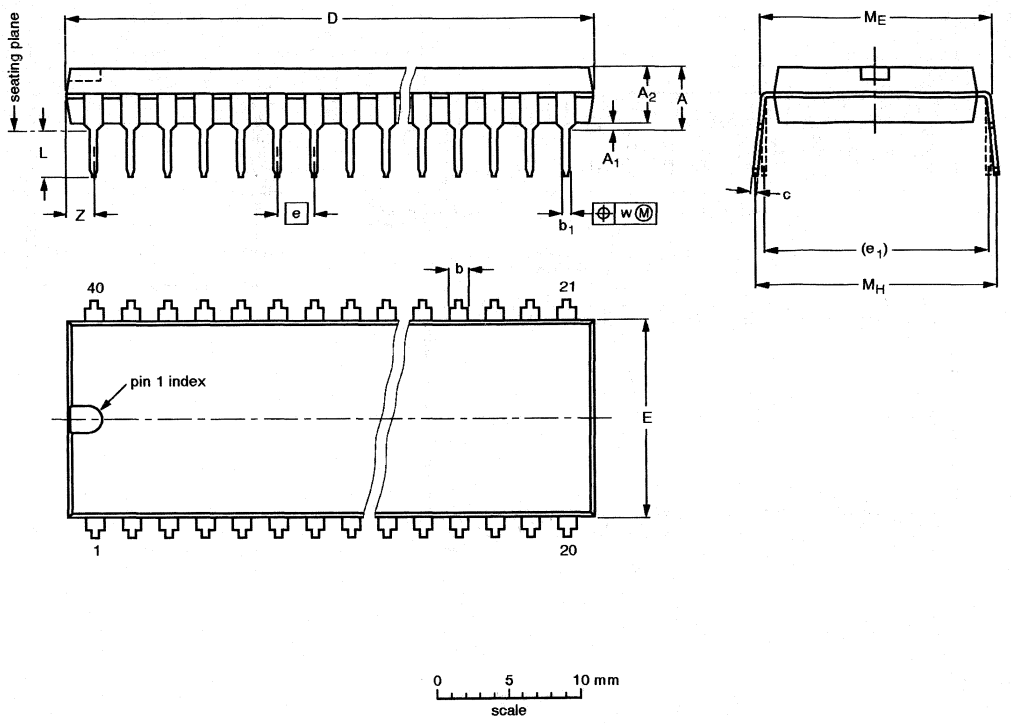
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-2		MS-011AB				95-03-11

Package outlines

DIP40: plastic dual in-line package; 40 leads (600 mil) SOT129-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

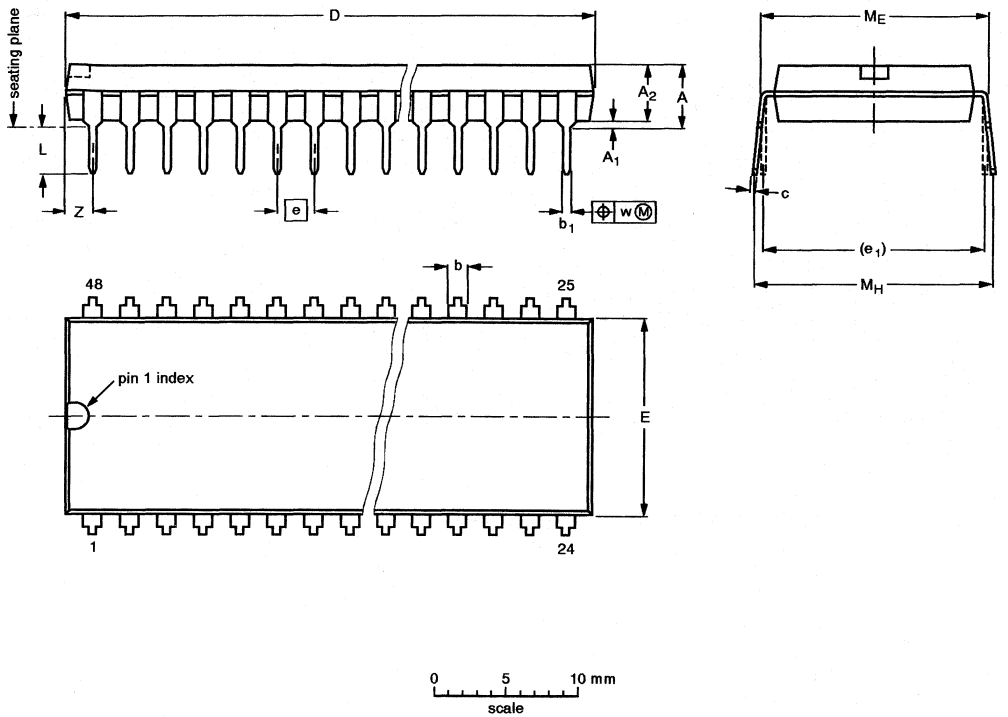
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

Package outlines

DIP48: plastic dual in-line package; 48 leads (600 mil) SOT240-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.9	0.36	4.06	1.4 1.14	0.53 0.38	0.36 0.23	62.60 61.60	14.22 13.56	2.54	15.24	3.90 3.05	15.88 15.24	18.46 15.24	0.254	2.1
inches	0.19	0.014	0.16	0.055 0.045	0.021 0.015	0.014 0.009	2.46 2.42	0.56 0.53	0.10	0.60	0.15 0.12	0.63 0.60	0.73 0.60	0.01	0.083

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

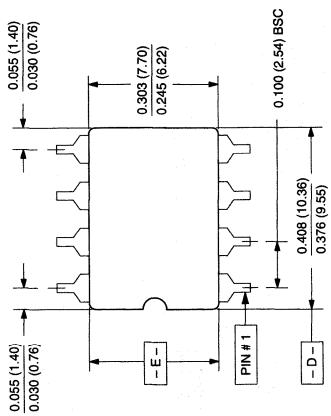
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT240-1						~~92-11-17~~ 95-01-25

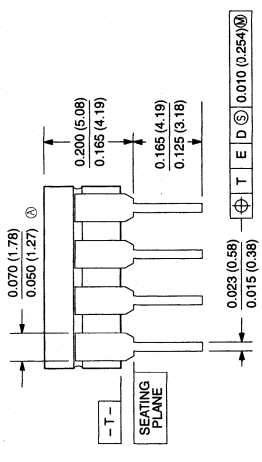
Package outlines

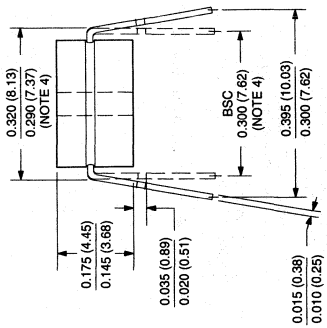
0580A 8-PIN (300 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE

NOTES:

1. Controlling dimension: Inches. Millimeters are shown in parentheses.
2. Dimension and tolerancing per ANSI Y14. 5M-1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #8 when viewed from the top.



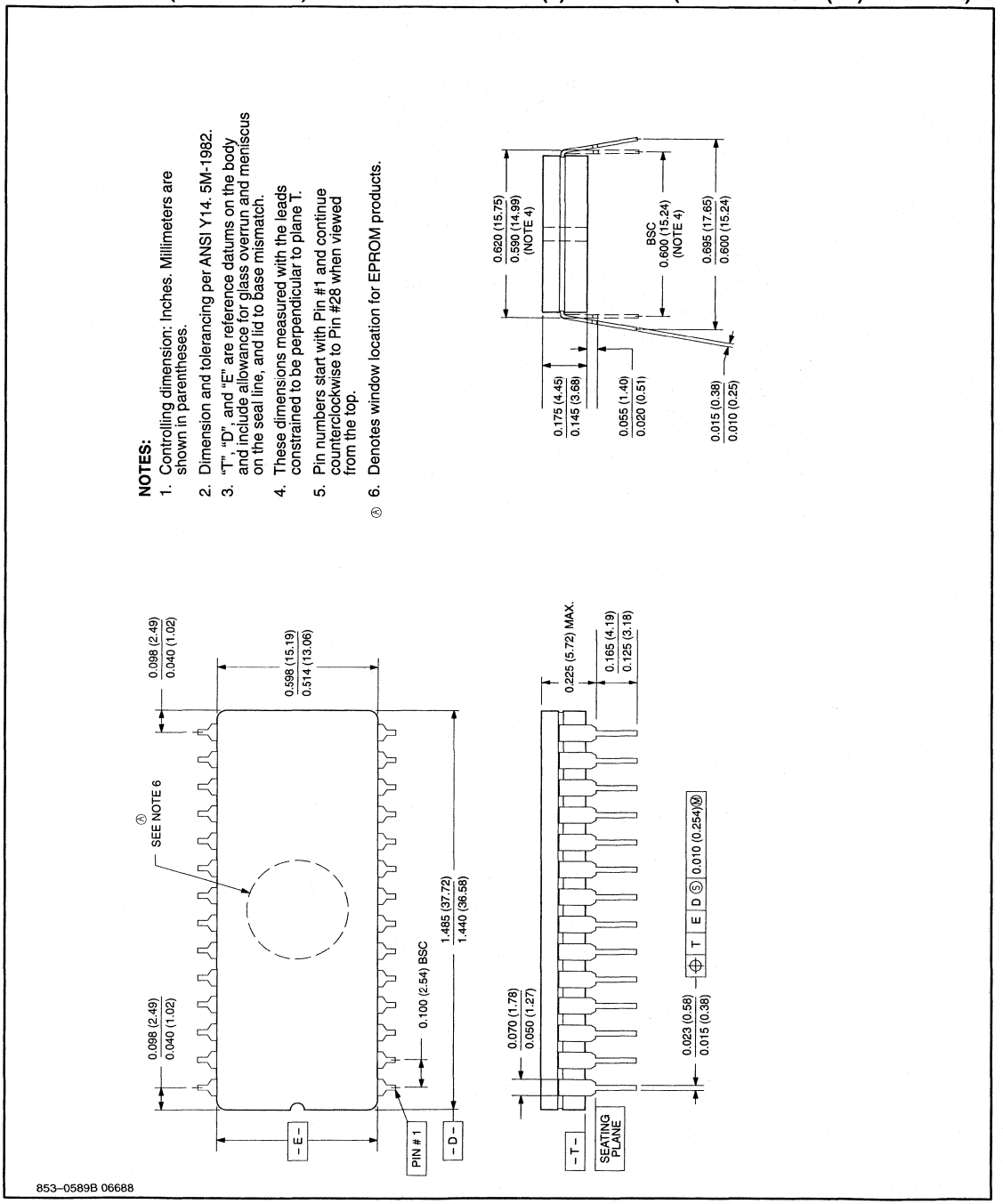




853–0580A 006688

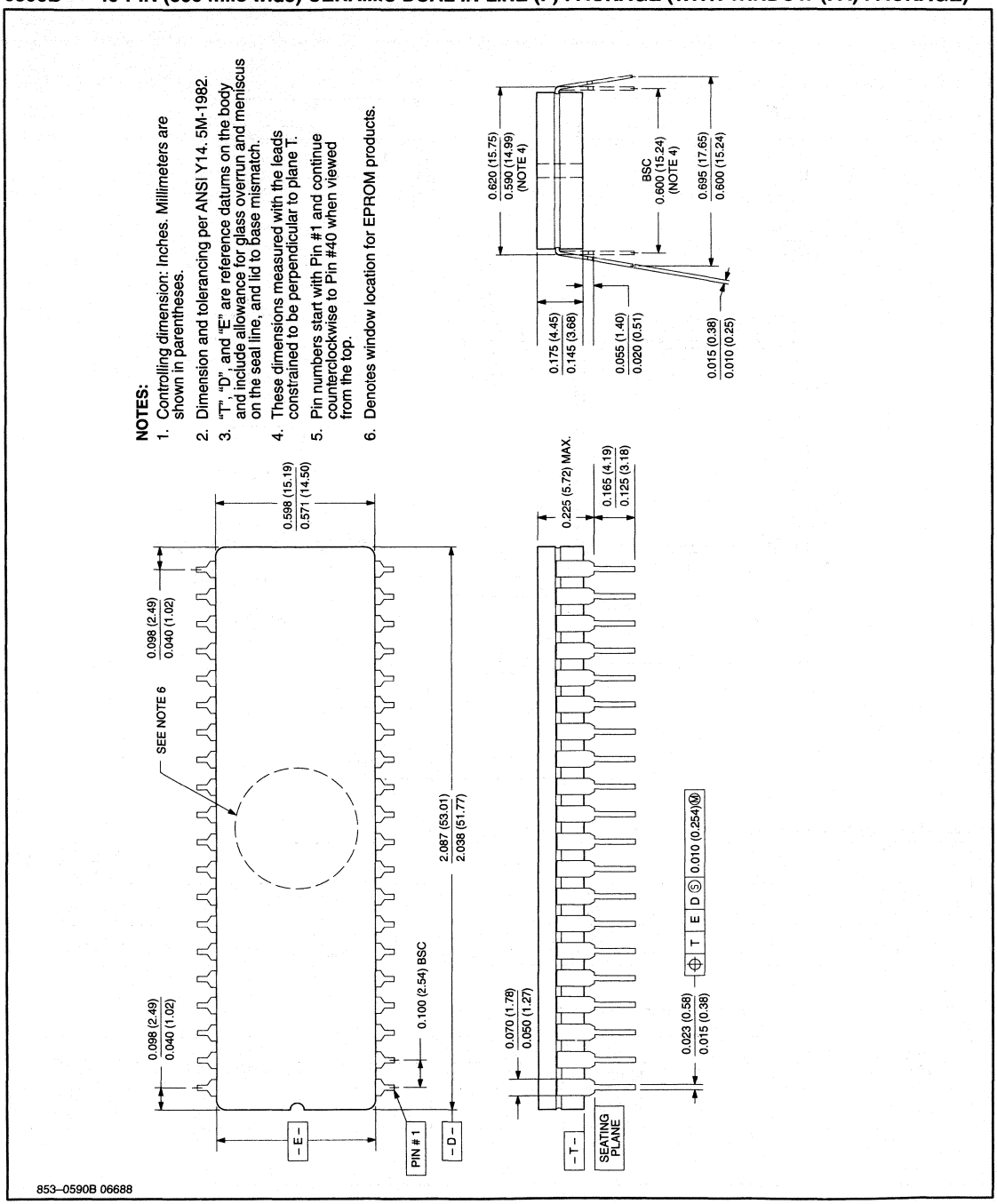
Package outlines

0589B 28-PIN (600 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE (WITH WINDOW (FA) PACKAGE)



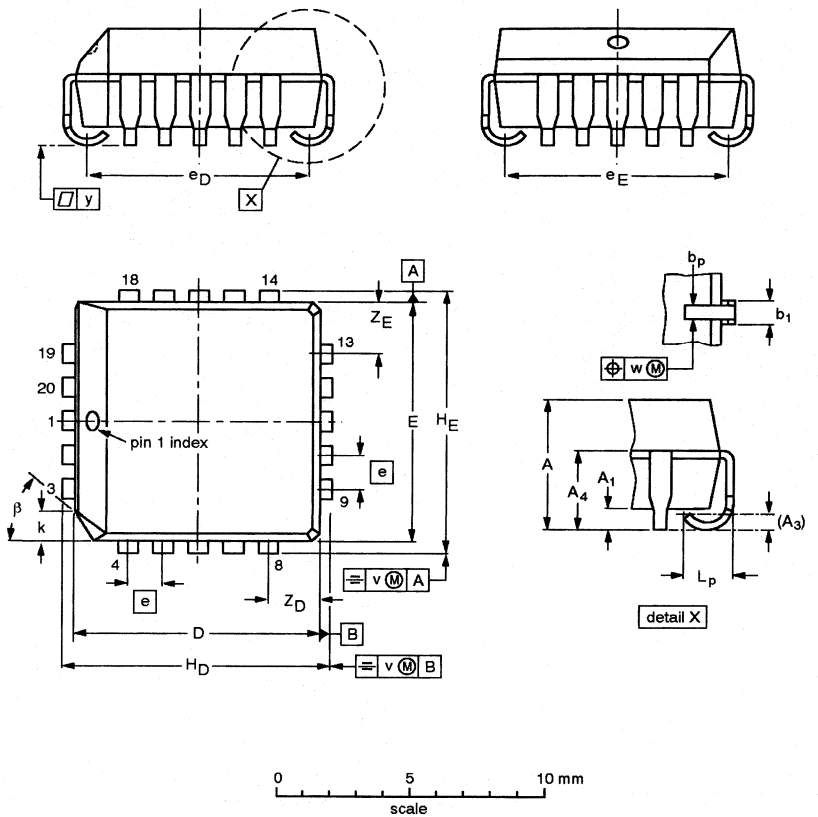
Package outlines

0590B 40-PIN (600 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE (WITH WINDOW (FA) PACKAGE)



Package outlines

PLCC20: plastic leaded chip carrier; 20 leads — SOT380-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	9.04 8.89	9.04 8.89	1.27	8.38 7.37	8.38 7.37	10.03 9.78	10.03 9.78	1.22 1.07	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.356 0.350	0.356 0.350	0.05	0.330 0.290	0.330 0.290	0.395 0.385	0.395 0.385	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

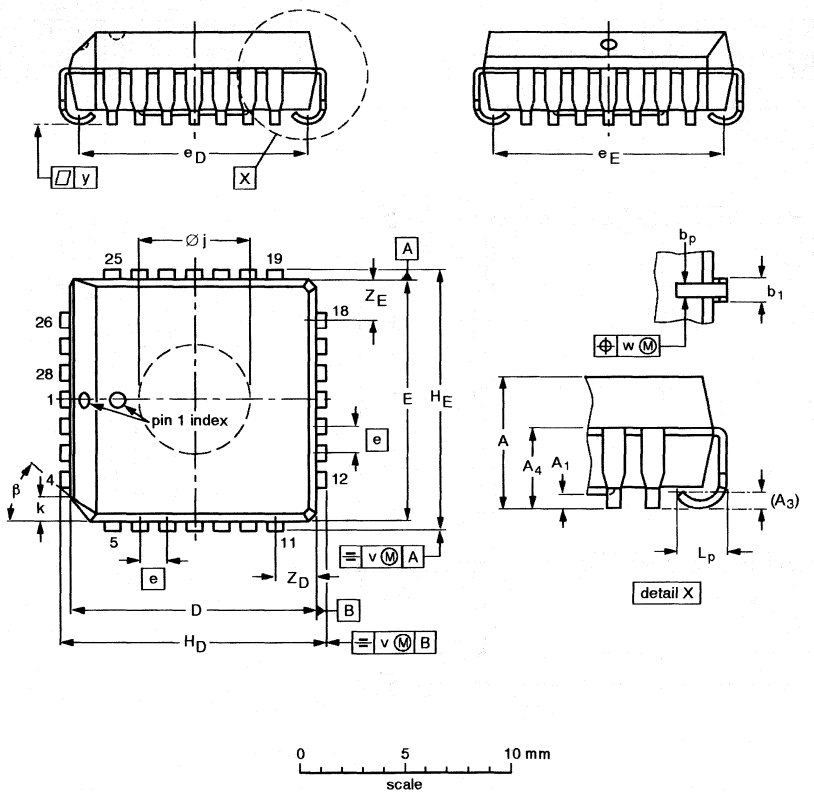
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT380-1		MO-047AA				~~95-02-25~~ 97-12-16

Package outlines

PLCC28: plastic leaded chip carrer; 28 leads; pedestal — SOT261-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	$Ø_j$	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	5.69 5.54	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.224 0.218	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

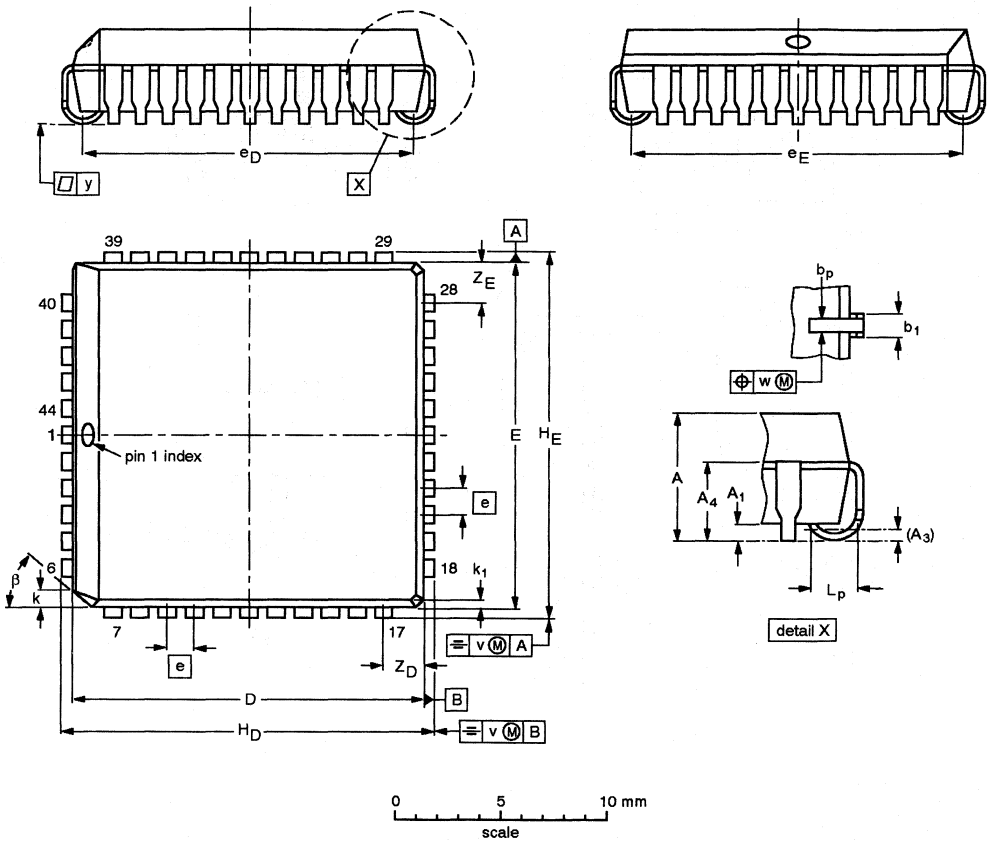
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT261-3		MO-047AB				~~95-02-25~~ 97-12-16

Package outlines

PLCC44: plastic leaded chip carrier; 44 leads — SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

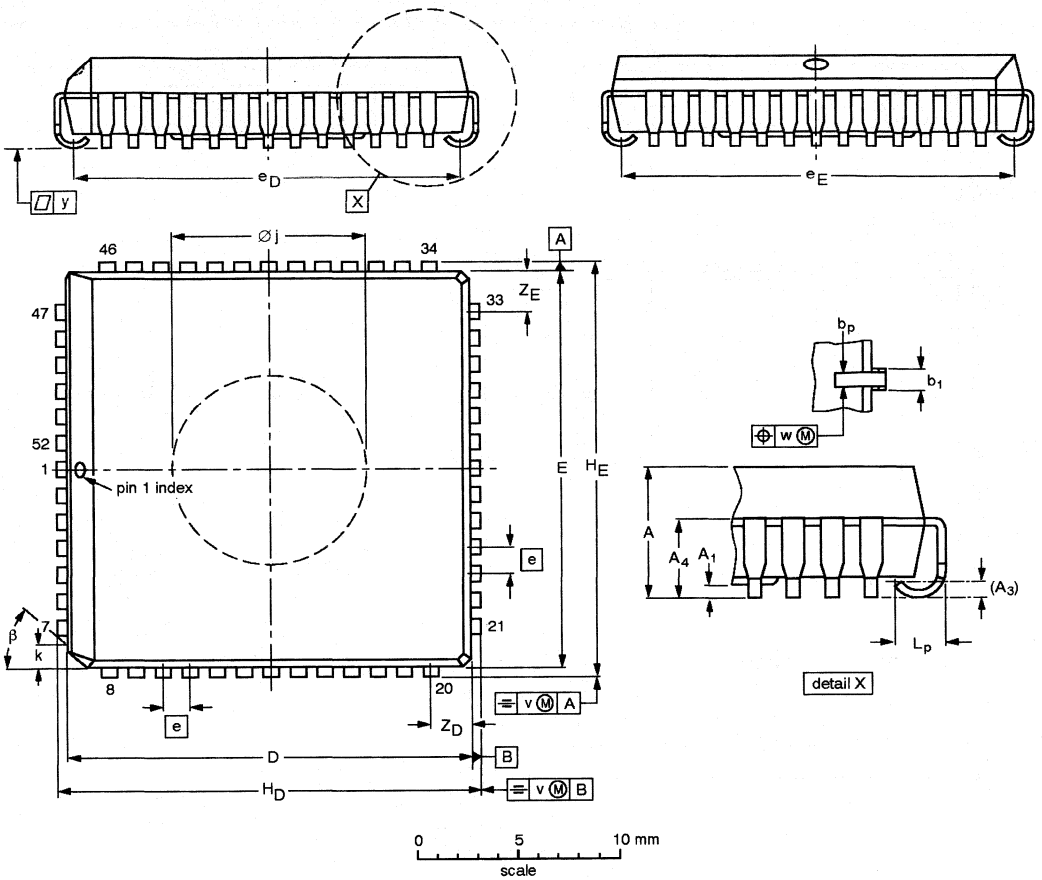
1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				~~95-02-25~~ 97-12-16

Package outlines

PLCC52: plastic leaded chip carrier; 52 leads; pedestal

SOT238-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	$Ø_j$	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	19.20 19.05	19.20 19.05	1.27	18.54 17.53	18.54 17.53	20.19 19.94	20.19 19.94	1.22 1.07	9.25 9.09	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.756 0.750	0.756 0.750	0.05	0.730 0.690	0.730 0.690	0.795 0.785	0.795 0.785	0.048 0.042	0.364 0.358	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

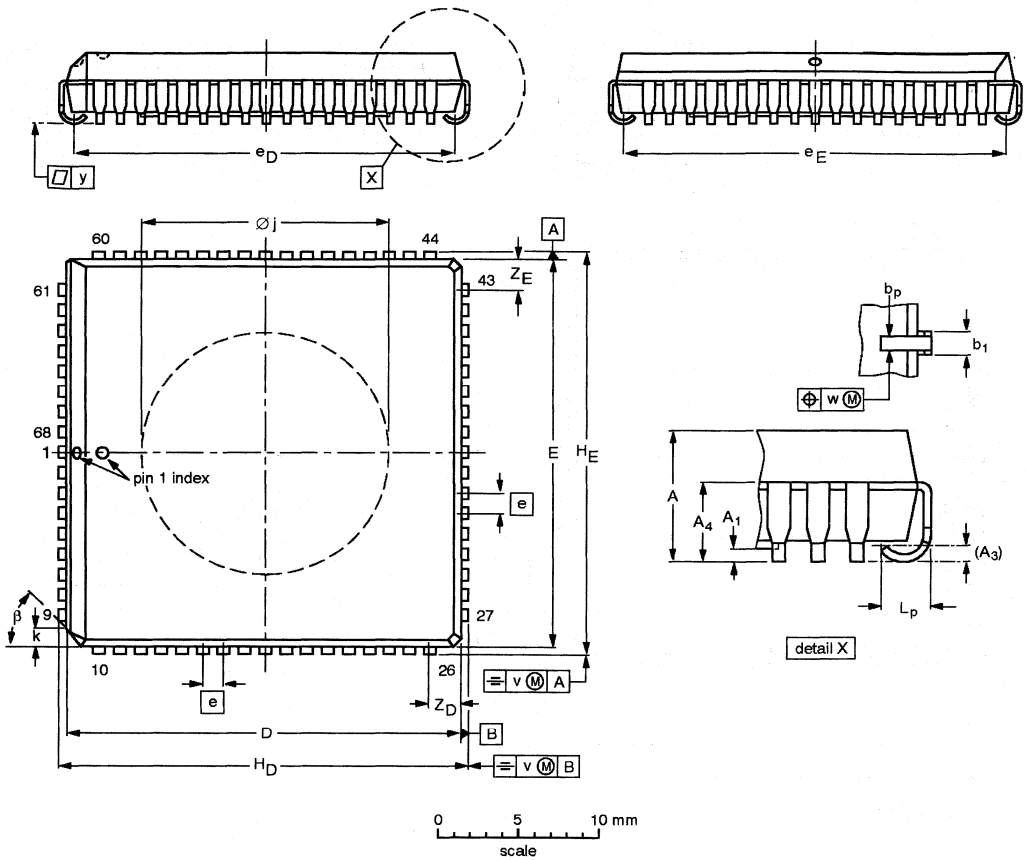
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT238-3		MO-047AD				~~95-02-25~~ 97-12-16

Package outlines

PLCC68: plastic leaded chip carrier; 68 leads; pedestal — SOT188-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	$Ø_j$	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	24.33 24.13	24.33 24.13	1.27	23.62 22.61	23.62 22.61	25.27 25.02	25.27 25.02	1.22 1.07	15.34 15.19	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.958 0.950	0.958 0.950	0.05	0.930 0.890	0.930 0.890	0.995 0.985	0.995 0.985	0.048 0.042	0.604 0.598	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

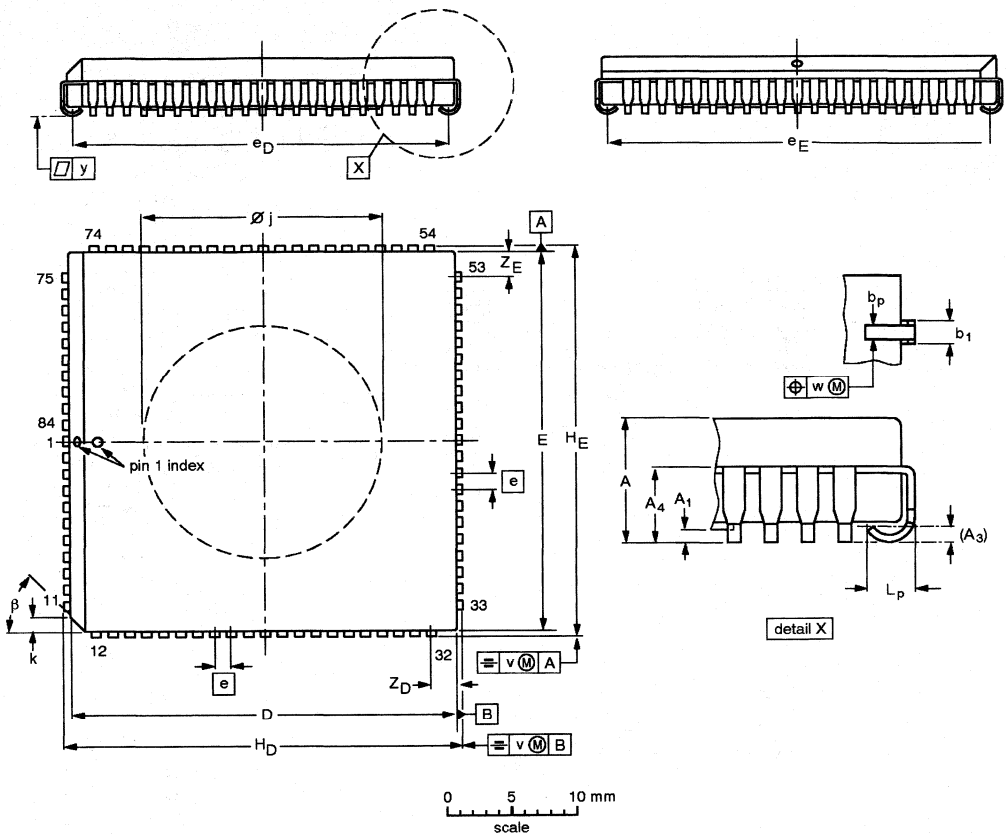
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT188-3	112E10	MO-047AE				~~95-02-25~~ 97-12-16

Package outlines

PLCC84: plastic leaded chip carrier; 84 leads; pedestal — SOT189-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	$Ø_j$	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	29.41 29.21	29.41 29.21	1.27	28.70 27.69	28.70 27.69	30.35 30.10	30.35 30.10	1.22 1.07	15.34 15.19	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	1.158 1.150	1.158 1.150	0.05	1.130 1.090	1.130 1.090	1.195 1.185	1.195 1.185	0.048 0.042	0.057 0.040	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

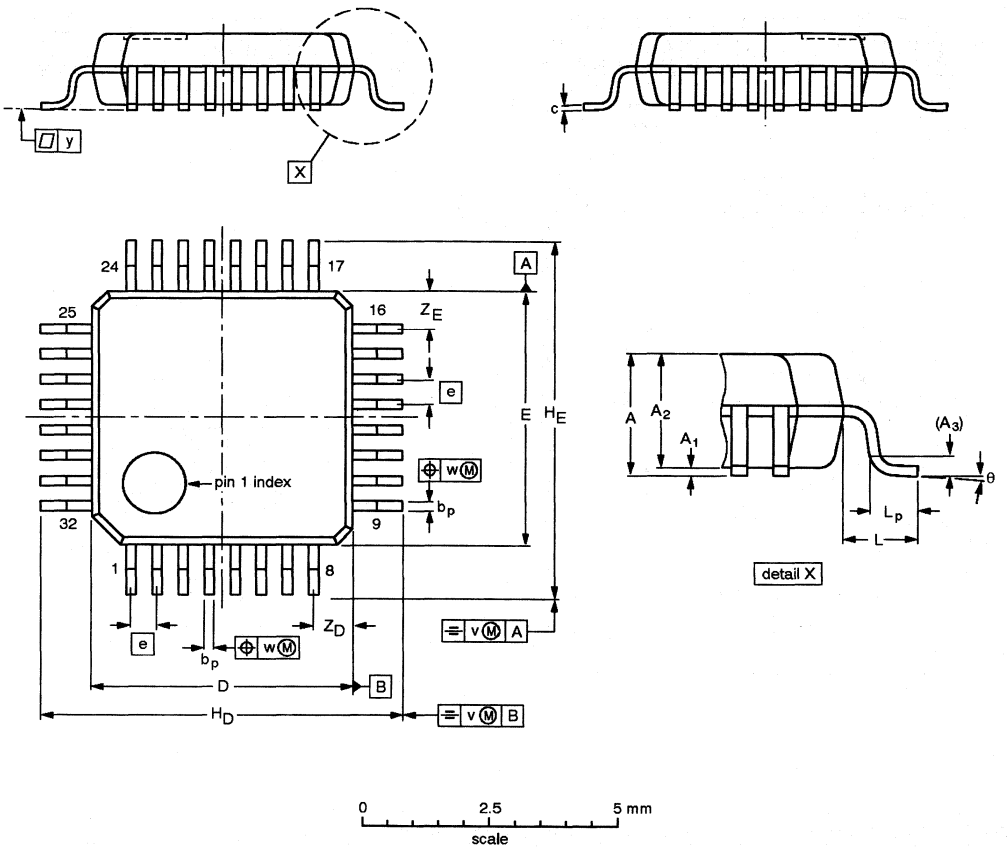
Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT189-3		MO-047AF				~~92-11-17~~ 95-02-25

Package outlines

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm — SOT401-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.15 0.05	1.5 1.3	0.25	0.27 0.17	0.18 0.12	5.1 4.9	5.1 4.9	0.5	7.15 6.85	7.15 6.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

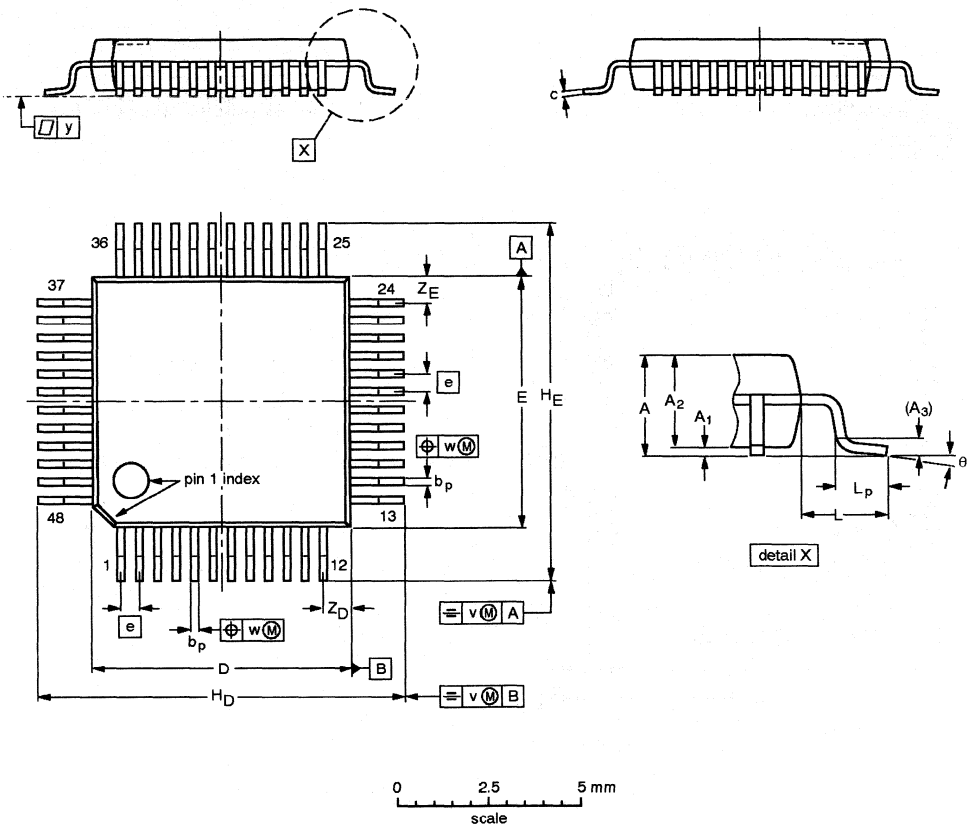
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT401-1						~~95-12-19~~ 97-08-04

Package outlines

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm — SOT313-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

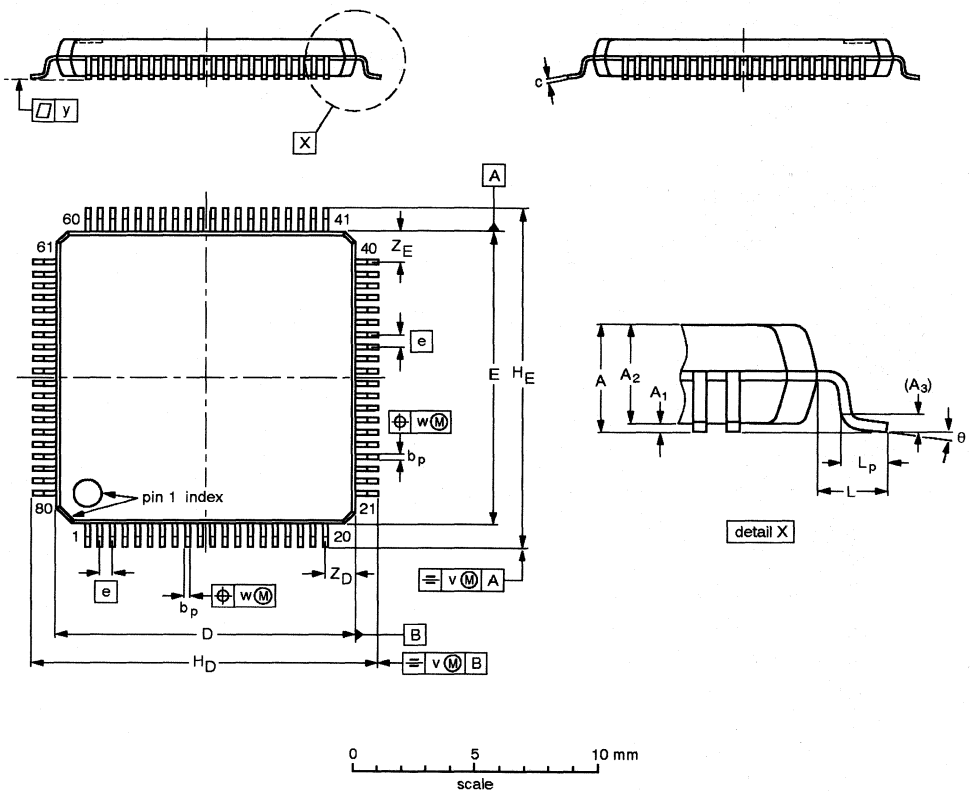
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~94-12-19~~ 97-08-01

Package outlines

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm — SOT315-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.27 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1.0	0.75 0.30	0.2	0.15	0.1	1.45 1.05	1.45 1.05	7° 0°

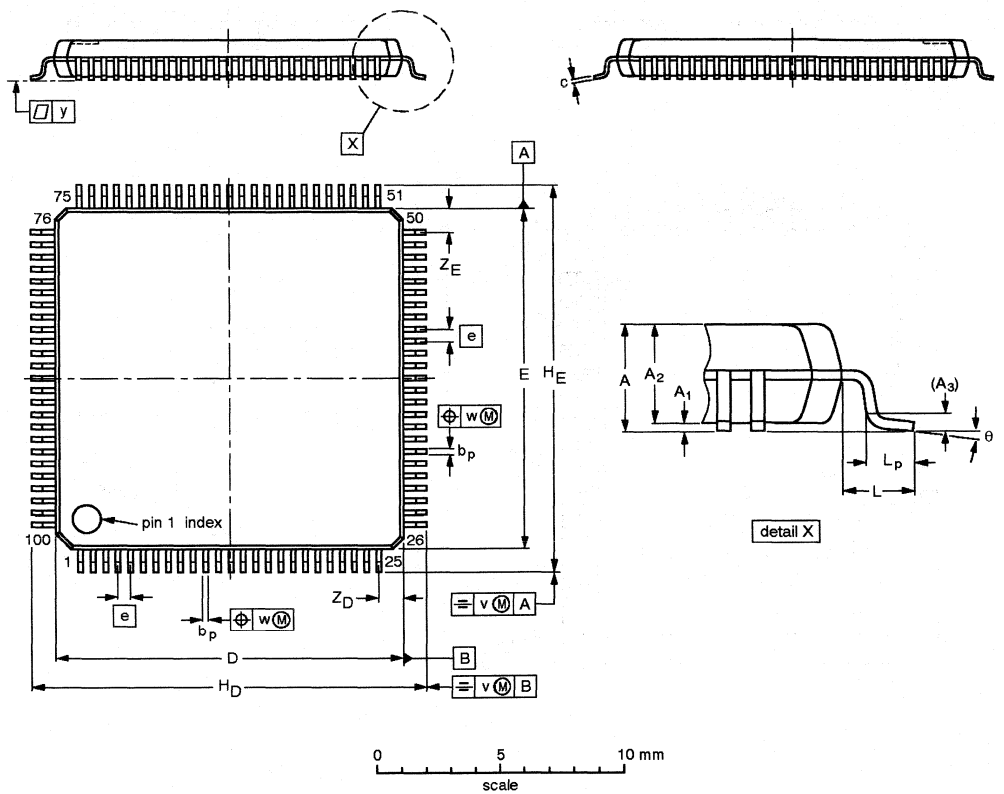
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT315-1						~~95-12-19~~ 97-07-15

Package outlines

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm — SOT407-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.5 1.3	0.25	0.28 0.16	0.18 0.12	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.2	0.12	0.1	1.15 0.85	1.15 0.85	7° 0°

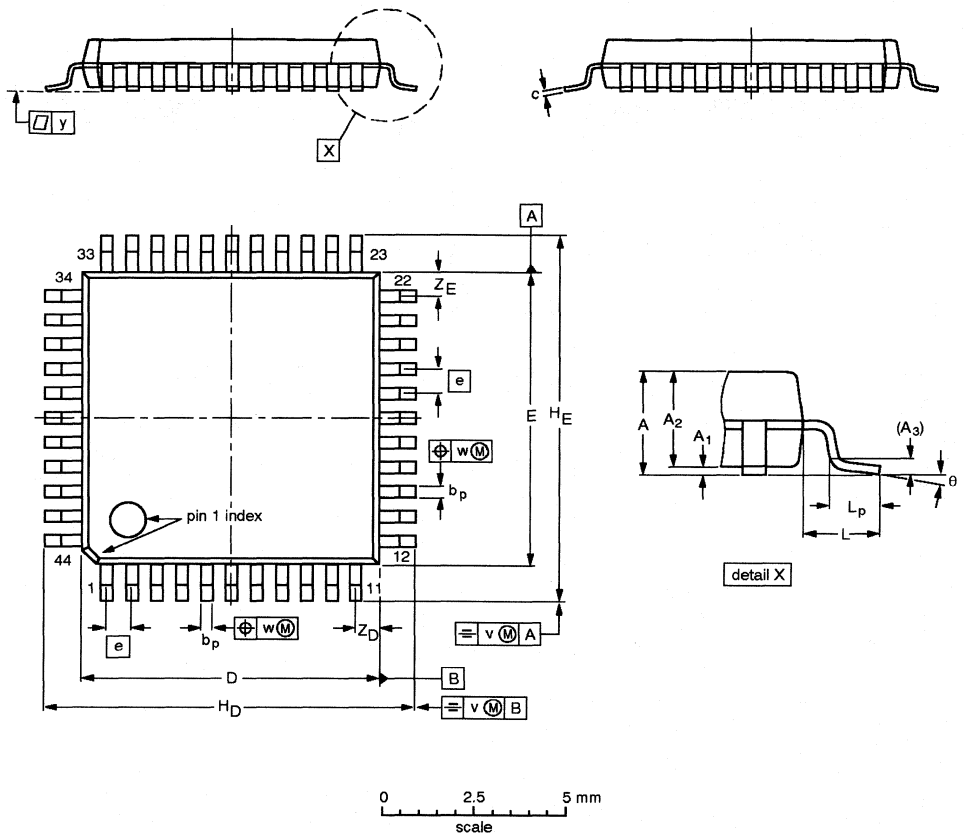
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1						~~95-12-19~~ 97-08-04

Package outlines

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm SOT307-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

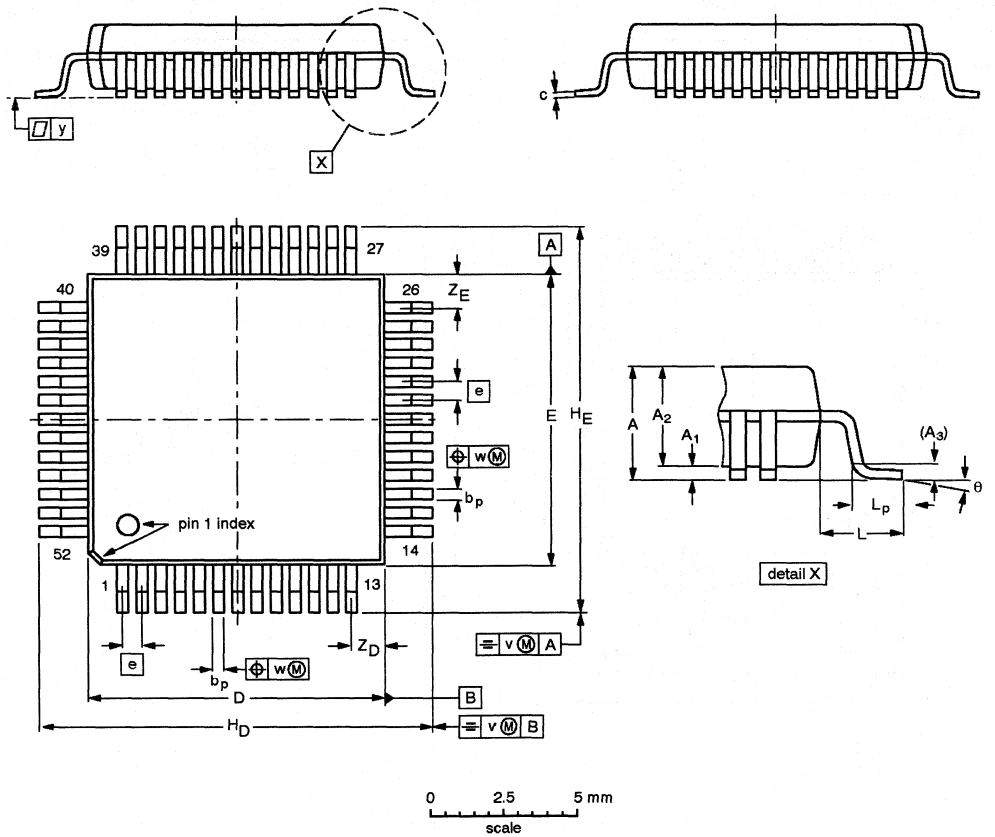
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~95-02-04~~ 97-08-01

Package outlines

QFP52: plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 x 10 x 2.0 mm SOT379-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.45	0.45 0.25	2.10 1.95	0.25	0.38 0.22	0.23 0.13	10.1 9.9	10.1 9.9	0.65	13.45 12.95	13.45 12.95	1.60	0.95 0.65	0.20	0.12	0.10	1.24 0.95	1.24 0.95	7° 0°

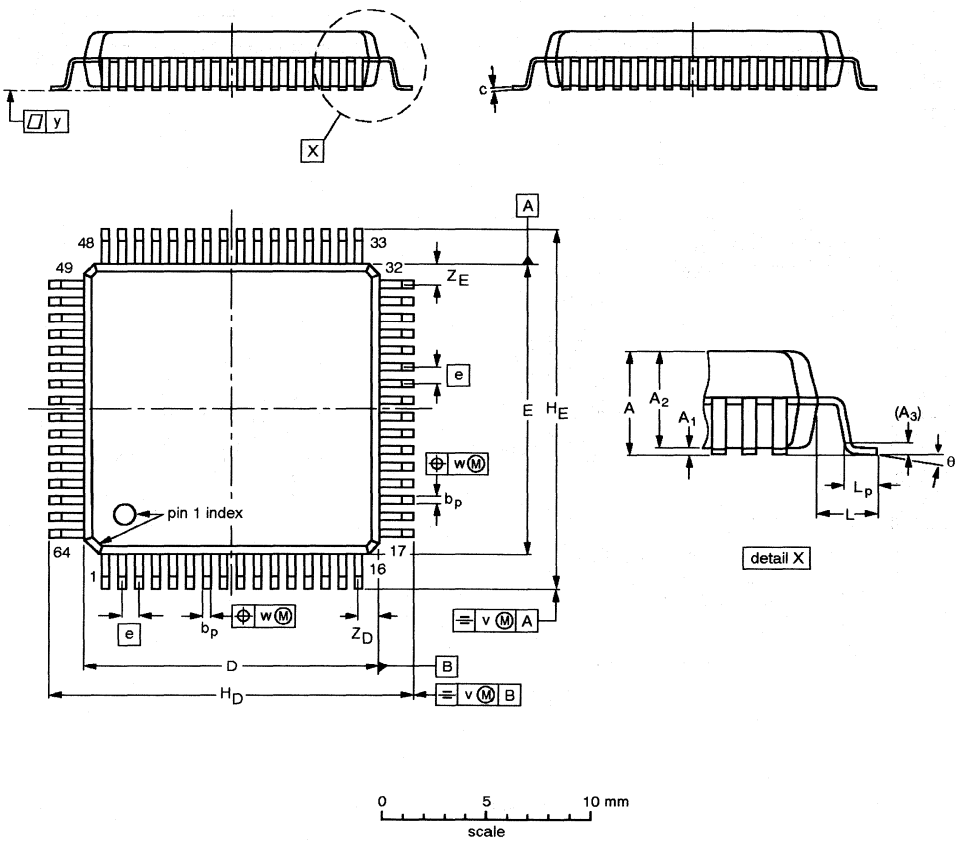
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT379-1		MO-108				~~95-02-04~~ 97-08-04

Package outlines

QFP64: plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 x 14 x 2.7 mm SOT393-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.00	0.25 0.10	2.75 2.55	0.25	0.45 0.30	0.23 0.13	14.1 13.9	14.1 13.9	0.8	17.45 16.95	17.45 16.95	1.60	1.03 0.73	0.16	0.16	0.10	1.2 0.8	1.2 0.8	7° 0°

Note

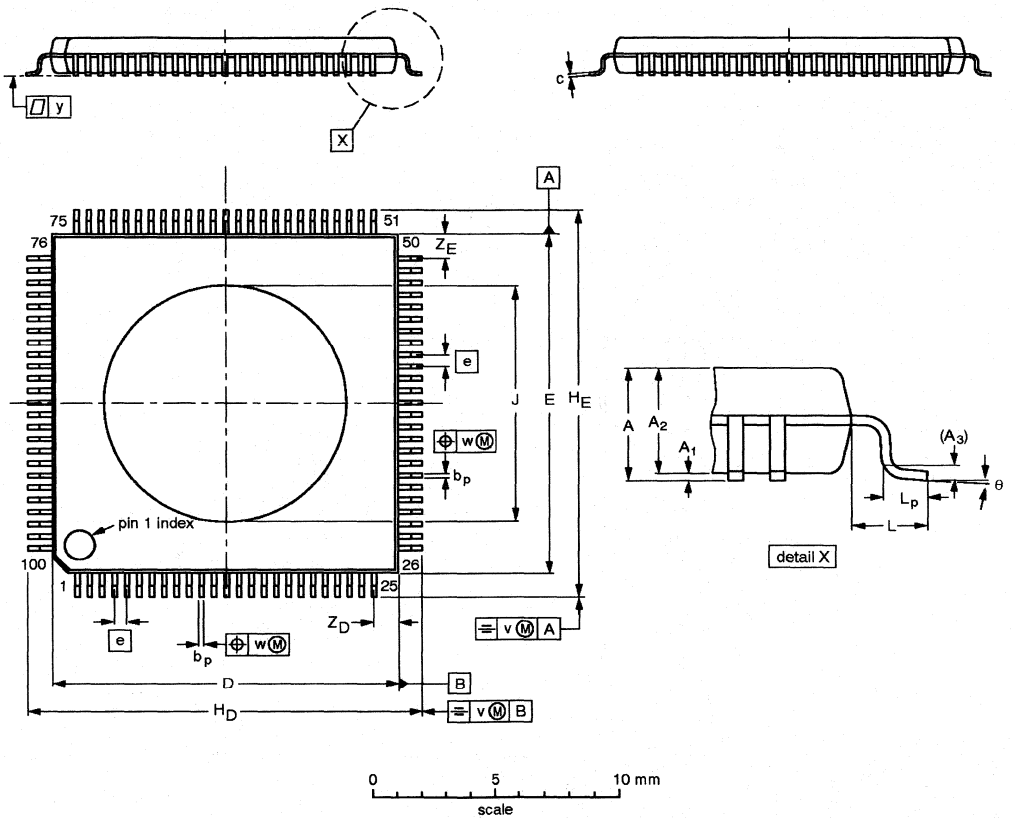
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT393-1		MS-022				~~96-05-21~~ 97-08-04

Package outlines

HLQFP100: plastic heat-dissipating low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm

SOT470-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	$J^{(2)}$	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.5 1.3	0.25	0.28 0.16	0.18 0.12	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	10.15 9.15	1.0	0.75 0.45	0.2	0.12	0.1	1.15 0.85	1.15 0.85	7^o 0^o

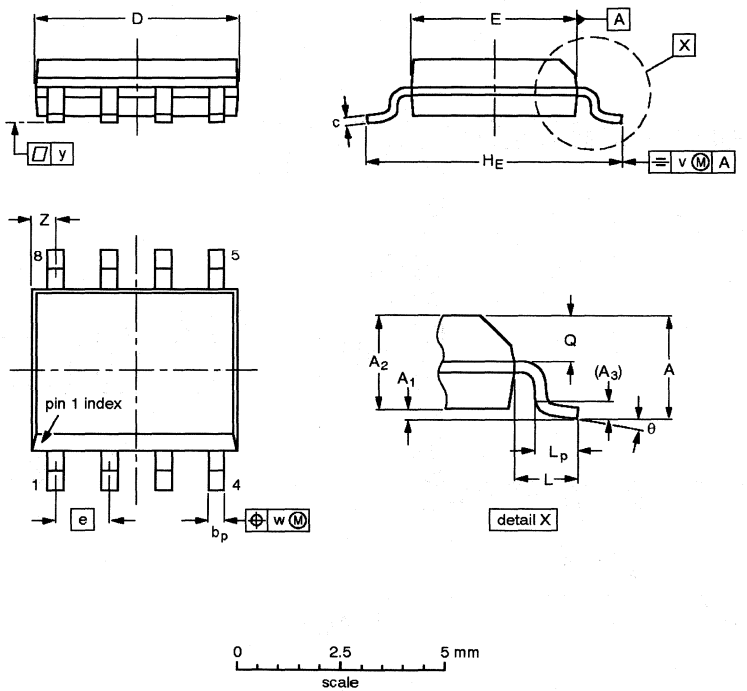
Notes

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.
2. Heatsink intrusion 0.0127 maximum.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT470-1						97-01-13

Package outlines

SO8: plastic small outline package; 8 leads; body width 3.9mm — SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

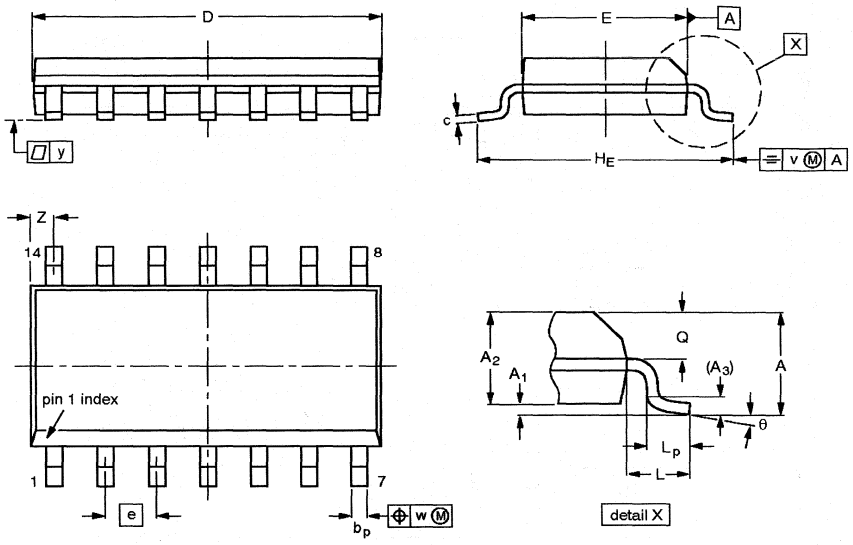
Notes

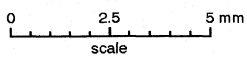
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

Package outlines

SO14: plastic small outline package; 14 leads; body width 3.9 mm — SOT108-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

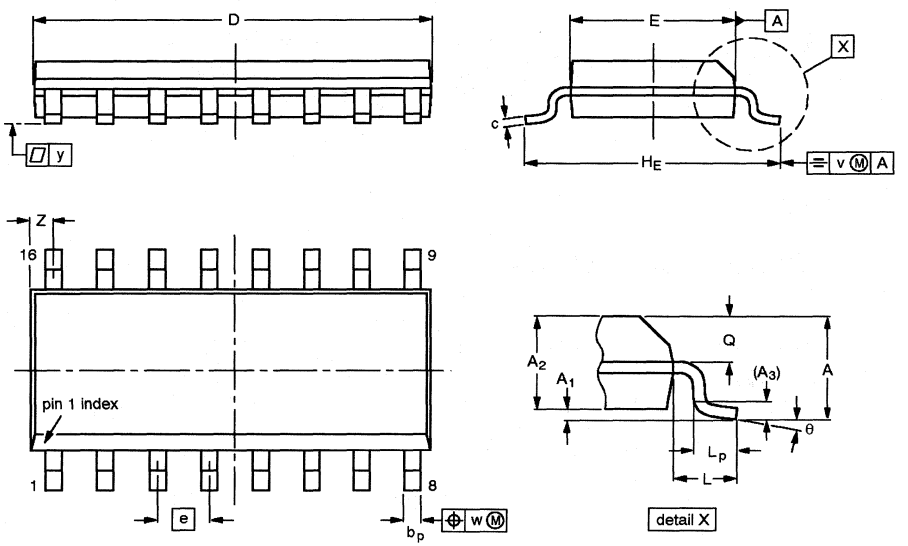
Note

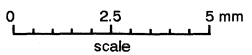
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~95-01-23~~ 97-05-22

Package outlines

SO16: plastic small outline package; 16 leads; body width 3.9 mm — SOT109-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

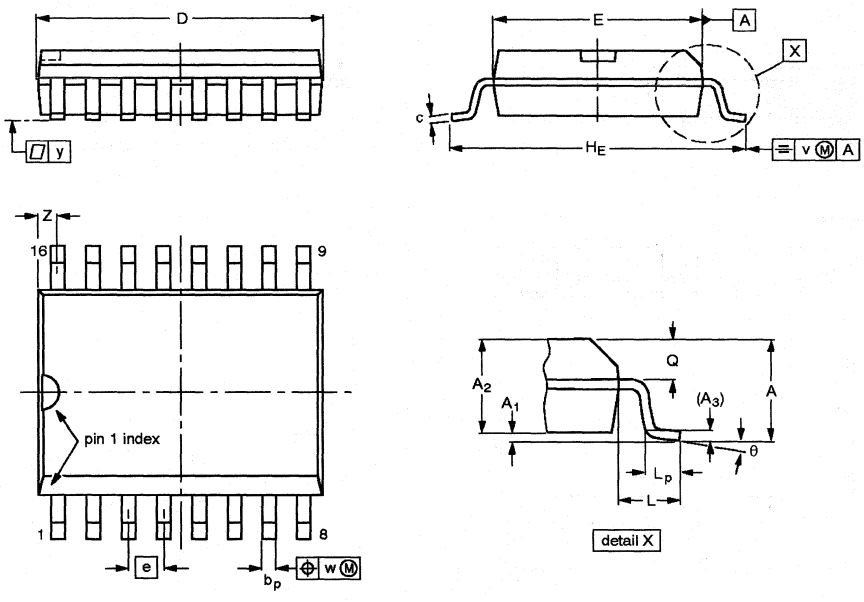
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

Package outlines

SO16: plastic small outline package; 16 leads; body width 7.5 mm — SOT162-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

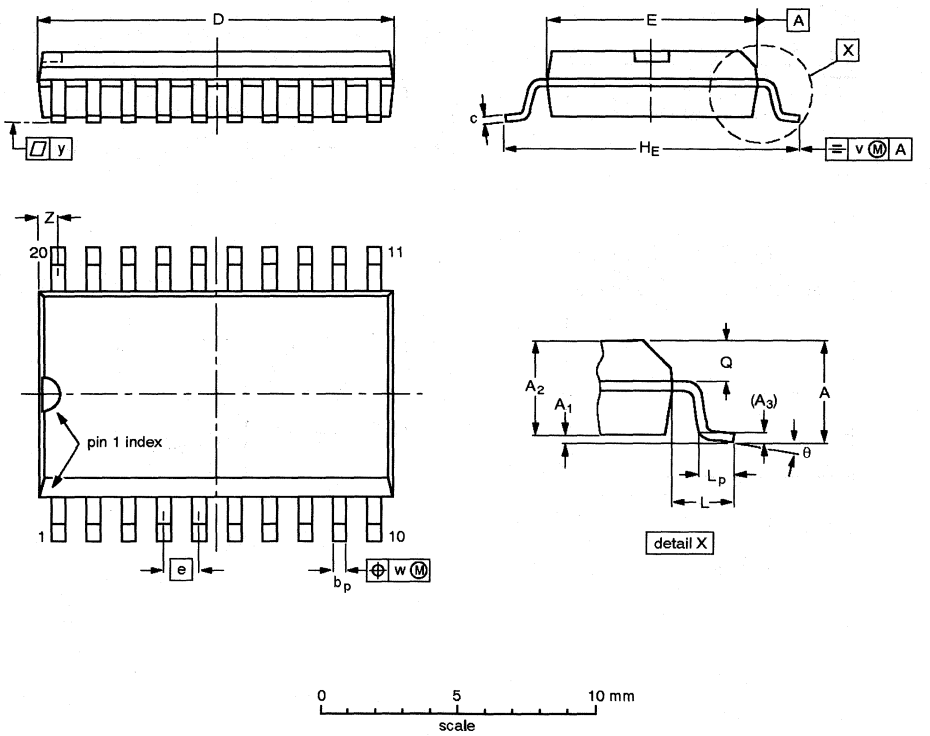
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~95-01-24~~ 97-05-22

Package outlines

SO20: plastic small outline package; 20 leads; body width 7.5 mm — SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

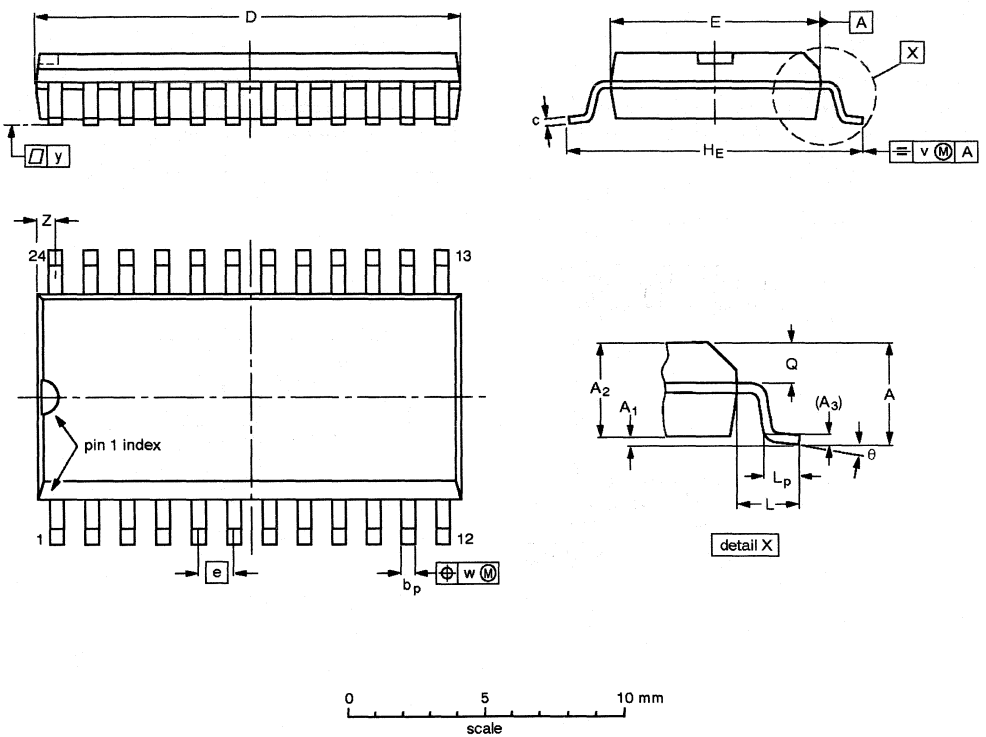
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

Package outlines

SO24: plastic small outline package; 24 leads; body width 7.5 mm — SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

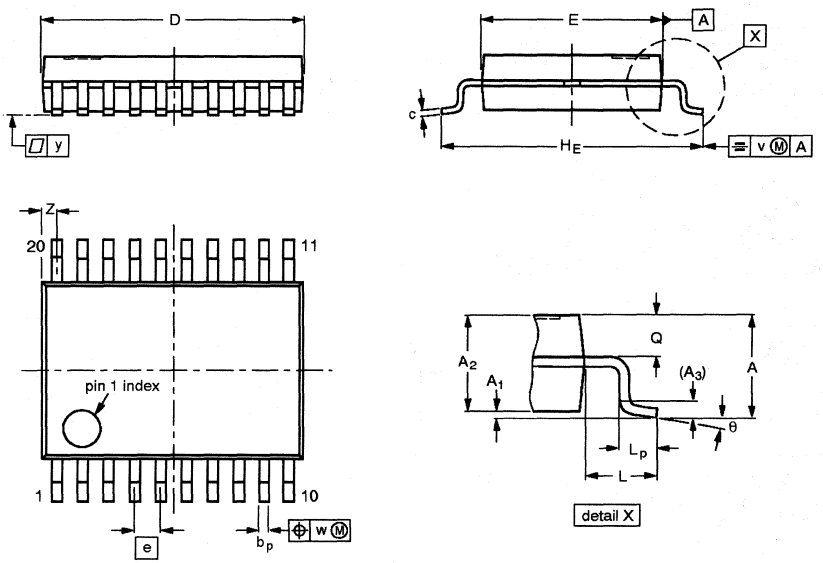
Note

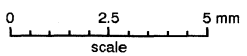
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

Package outlines

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm — SOT266-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

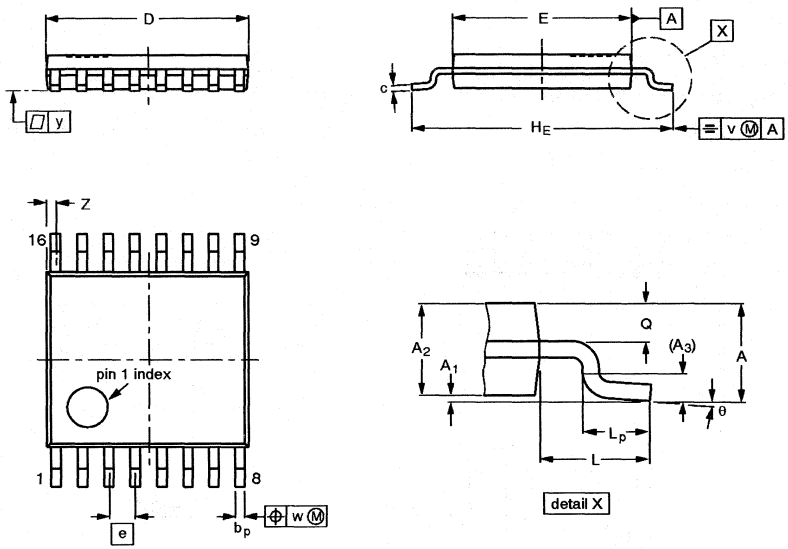
Note

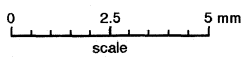
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

Package outlines

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm — SOT403-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

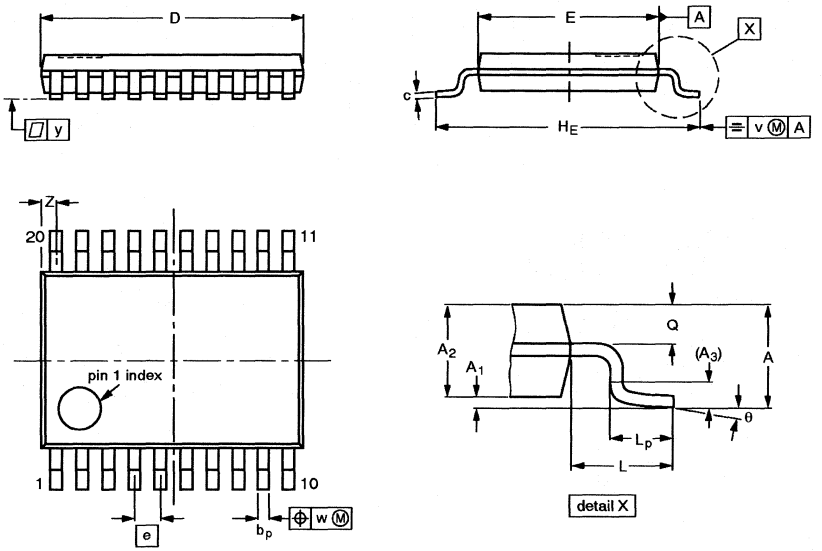
Notes

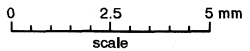
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

Package outlines

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm — SOT360-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

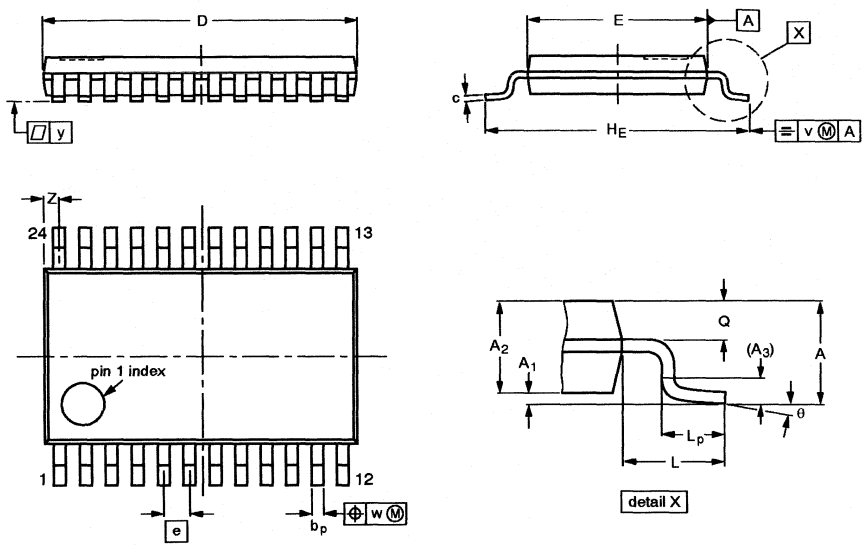
Notes

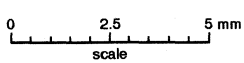
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				~~93-06-16~~ 95-02-04

Package outlines

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm — SOT355-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				~~93-06-16~~ 95-02-04

Appendix A
Data handbook system

Data handbook system 380

DATA HANDBOOK SYSTEM

Philips Semiconductors data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogs are available for selected product ranges (some catalogs are also on floppy discs).

Our data handbook titles are listed here.

Integrated Circuits

Book	*Title*
IC01	Semiconductors for Radio, Audio and CD/DVD Systems
IC02	Semiconductors for Television and Video Systems
IC03	Semiconductors for Wired Telecom Systems
IC04	HE4000B Logic Family CMOS
IC05	Advanced Low-power Schottky (ALS) Logic
IC06	High-speed CMOS Logic Family
IC11	General-purpose/Linear ICs
IC12	I^2C Peripherals
IC13	Programmable Logic Devices (PLD)
IC14	8048-based 8-bit Microcontrollers
IC15	FAST TTL Logic Series
IC16	CMOS ICs for Clocks, Watches and Real Time Clocks
IC17	Semiconductors for Wireless Communications
IC18	Semiconductors for In-Car Electronics
IC19	ICs for Data Communications
IC20	80C51-based 8-bit Microcontrollers
IC22	Multimedia ICs
IC23	BiCMOS Bus Interface Logic
IC24	Low Voltage CMOS & BiCMOS Logic
IC25	16-bit 80C51XA Microcontrollers (eXtended Architecture)
IC26	Integrated Circuit Packages
IC27	Complex Programmable Logic Devices

Discrete Semiconductors

Book	*Title*
SC01	Small-signal and Medium-power Diodes
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SC07	Small-signal Field-effect Transistors
SC13	Power MOS Transistors
SC14	RF Wideband Transistors
SC16	Wideband Hybrid Amplifier Modules for CATV
SC17	Semiconductor Sensors
SC18	Discrete Semiconductor Packages
SC19	RF & Microwave Power Transistors, RF Power Modules and Circulators/Isolators

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Our sister product division, Philips Components, also has a comprehensive data handbook system to support their products. Their data handbook titles are listed here.

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DC01	Colour Television Tubes
DC02	Monochrome Monitor Tubes and Deflection Units
DC03	Television Tuners, Coaxial Aerial Input Assemblies
DC04	Colour Monitor and Multimedia Tubes
DC05	Wire Wound Components

Magnetic Products

MA01	Soft Ferrites
MA03	Piezoelectric Ceramics Specialty Ferrites
MA04	Dry-reed Switches

Passive Components

PA01	Electrolytic Capacitors
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PA03	Potentiometers
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PA05	Film Capacitors
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PA06a	Surface Mounted Ceramic Multilayer Capacitors
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PA11	Quartz Oscillators

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